

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Add device type 05 to the drawing for vendor CAGE 34335. Add vendor CAGE 01295 for device type 04LX, 043X, and 04KX. Add footnote 9 to table I, subgroups 9, 10, and 11 testing. Changes to vendor similar part number for vendor CAGE 01295. Correction to table I, parameter I _{OS} . Editorial changes throughout.	91-05-01	M. A. Frye
E	Changes in accordance with NOR 5962-R298-97.	97-05-16	Raymond Monnin
F	Update drawing to current requirements. Editorial changes throughout. - gap	02-01-03	Raymond Monnin
G	Boilerplate update, part of 5 year review. ksr	06-05-22	Raymond Monnin
H	Update drawing in accordance with latest MIL-PRF-38535 requirements. - glg	14-07-10	Charles Saffle

This original first sheet of this drawing has been replaced.

CURRENT CAGE CODE 67268

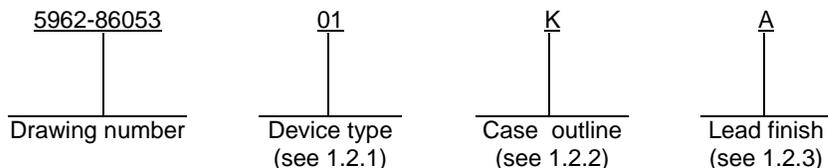
REV																				
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REV STATUS OF SHEETS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12							

PMIC N/A	PREPARED BY Greg A. Pitz	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p>																		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Dan DiCenzo																			
	APPROVED BY Robert P. Evans																			
	DRAWING APPROVAL DATE 86-07-10																			
	REVISION LEVEL H																			
	SIZE A	CAGE CODE 14933	5962-86053																	
	SHEET 1 OF 12																			

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	PAL22V10A	22-input 10-output registered AND-OR logic array
02	PAL22V10	22-input 10-output registered AND-OR logic array
03	PAL22VP10-25	22-input 10-output registered AND-OR logic array
04	PAL22V10-20	22-input 10-output registered AND-OR logic array
05	PAL22V10-12	22-input 10-output registered AND-OR logic array

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
K	GDFP2-F24 or CDFP3-F24	24	Flat package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Output voltage applied	-0.5 V dc to +7.0 V dc <u>2/</u>
Output sink current.....	+100 mA <u>2/</u>
Thermal resistance, junction-to-case (θ_{JC}):	
Cases K, L, and 3.....	See MIL-STD-1835
Maximum power dissipation (P_D) <u>3/</u>	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+260°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum

1/ All voltages referenced to V_{SS} .

2/ Except during programming.

3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS} .

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2. Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2. Terminal connections. The terminal connections shall be as specified on figure 1.

3.2. Truth tables.

3.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2. Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _I = -18 mA		1, 2, 3	All		-1.2	V
High level output voltage	V _{OH}	I _O = -2.0 mA, V _{CC} = 4.5 V, V _{IN} = 2.0 V or 0.8 V		1, 2, 3	All	2.4		V
Low level output voltage	V _{OL}	I _O = 12.0 mA, V _{CC} = 4.5 V, V _{IN} = 2.0 V or 0.8 V		1, 2, 3	All		0.5	V
High impedance output leakage current ^{2/}	I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V	1, 2, 3	All		100	μA
	I _{OZL}	V _{IN} = V _{IH} or V _{IL}				V _O = 0.4 V		
High level input current	I _{IH}	V _{IN} = 2.7 V, V _{CC} = 5.5 V		1, 2, 3	All		25	μA
		V _{IN} = 5.5 V, V _{CC} = 5.5 V		1, 2, 3	All		1.0	mA
Low level input current	I _{IL}	V _{IN} = 0.4 V, V _{CC} = 5.5 V		1, 2, 3	All		-250	μA
Supply current	I _{CC}	V _{CC} = 5.5 V		1, 2, 3	02		180	mA
					03		230	
					01, 04, 05		200	
Output short circuit current ^{3/}	I _{OS}	V _{CC} = 5.5 V, V _O = 0.5 V		1, 2, 3	01, 02, 03, 04	-30	-90	mA
					05	-30	-130	
Propagation delay output high impedance to output valid	t _{PZD}	V _{CC} = 5.0 V ±10%, C _L = 50 pF See figures 4 and 5 ^{4/}		9, 10, 11	01		30	ns
					02		40	
					03		25	
					04		20	
					05		15	
Propagation delay output valid to ^{5/} output high impedance	t _{PDZ}			9, 10, 11	01		30	ns
					02		40	
					03		25	
					04		20	
					05		12.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay <u>6/</u> data input to output	t _{PHL}	V _{CC} = 5.0 V ±10%, C _L = 50 pF See figures 4 and 5 <u>4/</u>	9, 10, 11	01		30	ns
				02		40	
				03		25	
				04		20	
				05		12	
Propagation delay <u>6/</u> data input to output	t _{PLH}		9, 10, 11	01		30	ns
				02		40	
				03		25	
				04		20	
				05		12	
Clock pulse width <u>7/</u>	t _{CL}		9, 10, 11	01,03	20		ns
				02	30		
				04	15		
				05	6		
Setup time <u>7/</u>	t _{SU}		9, 10, 11	01,03	25		ns
				02	35		
				04	17		
				05	10		
Hold time <u>7/</u>	t _H		9, 10, 11	All	0		ns
Maximum clock frequency <u>7/ 8/</u>	f _{MAX}		9, 10, 11	01		22	MHz
				02		16.5	
				03		25	
				04		33.3	
				05		50	
Asynchronous reset pulse width <u>7/ 9/</u>	t _{AW}		9, 10, 11	01,03	30		ns
				02	40		
				04	20		
				05	15		
Asynchronous reset recovery time <u>7/ 9/</u>	t _{AR}		9, 10, 11	01,03	30		ns
				02	40		
				04	20		
				05	10		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Asynchronous reset to registered output reset <u>7/</u>	t _{AP}	<u>4/</u>	9, 10, 11	01		35	ns
				02		45	
				03, 04		25	
				05		20	
Propagation delay clock to output <u>7/</u>	t _{CO}		9, 10, 11	01		20	ns
				02		25	
				03, 04		15	
				05		10	

1/ All voltages are referenced to ground.

2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.

3/ Only one output shorted at a time.

4/ Equivalent test loads may be used for testing when submitted to and approved by DLA Land and Maritime.

5/ C_L = 5 pF for t_{PDZ} test.

6/ Test applies only to non-registered (combinational logic) outputs.

7/ Test applies only to register outputs.

8/ f_{MAX} is derived by testing t_{SU} and t_{CO} and is not tested directly.

9/ Not tested directly, but guaranteed by testing of t_{AP} and t_{SU}.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8,
Group A test requirements (method 5005)	1*, 2, 3, 7*, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1*, 2, 3

1/ (*) indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall also verify that no fuses
are blown for unprogrammed devices or that the altered item drawing
pattern exists for programmed devices.

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Device types	01 through 05	
Case outlines	L and K	3
Terminal number	Terminal symbol	
1	CK/I	NC
2	I	CK/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V _{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V _{CC}

FIGURE 1. Terminal connections.

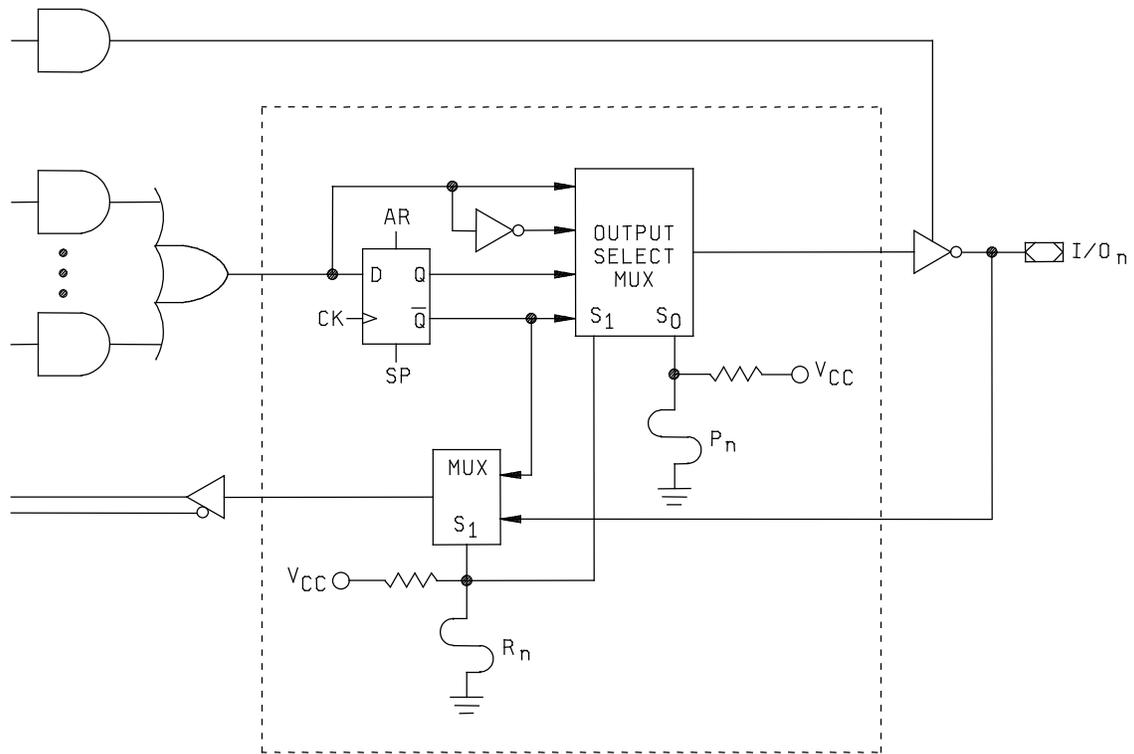
Truth table																					
Input pins											Output pins										
I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	
X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	

- NOTES:
 1. Z = Three-state
 2. X = Don't care

FIGURE 2. Truth table.

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OUTPUT LOGIC MACROCELL



S1	S0	Output configuration
0	0	Registered/active low
0	1	Registered/active high
1	0	Combinatorial/active low
1	1	Combinatorial/active high

0 = Unblown fuse
1 = Blown fuse

FIGURE 3. Logic diagram.

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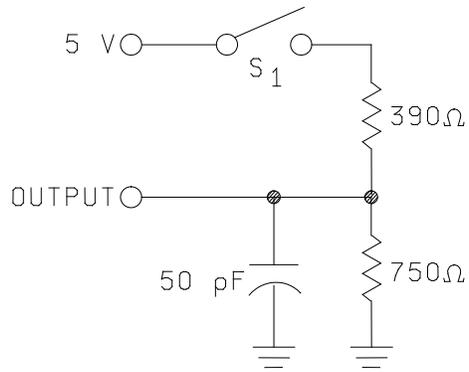
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NOTE: S_1 is open for high impedance to high tests and closed for high impedance to low test. Output disable times (t_{PDZ}) are tested with $C_L = 50$ pF. High to high impedance tests are made to output voltage of $V_{OH} - 0.5$ V with S_1 open; low to high impedance tests are made to $V_{OL} + 0.5$ V level with S_1 closed.

FIGURE 4. Output test circuit.

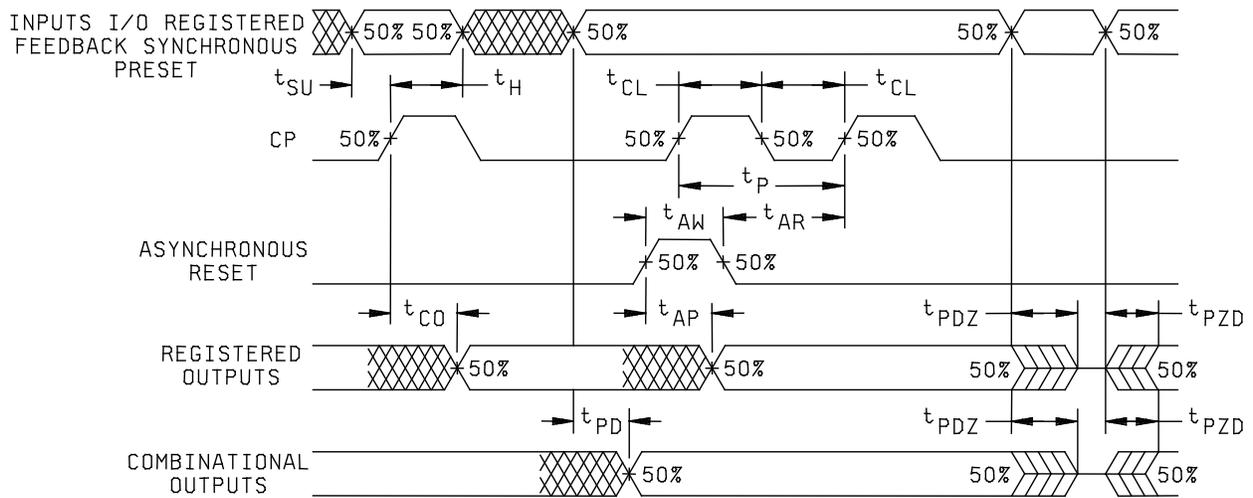


FIGURE 5. Switching waveforms.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:
 - (1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.
 - (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

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6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-07-10

Approved sources of supply for SMD 5962-86053 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8605301KA	01295	TIBPAL22V10AMWB
	<u>3/</u>	AMPAL22V10A/BKA
5962-8605301LA	01295	TIBPAL22V10AMJTB
	<u>3/</u>	AMPAL22V10A/BLA
5962-86053013A	01295	TIBPAL22V10AMFKB
	<u>3/</u>	AMPAL22V10A/B3C
5962-8605302KA	<u>3/</u>	AMPAL22V10/BKA
5962-8605302LA	<u>3/</u>	AMPAL22V10/BLA
5962-86053023A	<u>3/</u>	AMPAL22V10/B3A
5962-8605303KA	01295	TIBPAL22VP10-25MWB
5962-8605303LA	01295	TIBPAL22VP10-25MJTB
5962-86053033A	01295	TIBPAL22VP10-25MFKB
5962-8605304KA	01295	TIBPAL22V10-20MWB
	<u>3/</u>	PAL22V10-20/BKA
5962-8605304LA	01295	TIBPAL22V10-20MJTB
	<u>3/</u>	PAL22V10-20/BLA
5962-86053043A	01295	TIBPAL22V10-20MFKB
	<u>3/</u>	PAL22V10-20/B3A
5962-8605305KA	<u>3/</u>	PAL22V10-12/BKA
5962-8605305LA	<u>3/</u>	PAL22V10-12/BLA
5962-86053053A	<u>3/</u>	PAL22V10-12/B3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

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STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
P O Box 660199
Dallas, TX 75243

Point of contact:

U.S. Highway 75 South
P O Box 84, M/S 853
Sherman, TX 75090-9493

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