REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 27014 for 012X. Editorial changes throughout. Change drawing CAGE code from 14933 to 67268. - mbk	89-01-13	Michael A. Frye
B	Update boilerplate to MIL-PRF-38535 requirements. – jak	01-10-18	Thomas M. Hess
C	Update boilerplate to MIL-PRF-38535 requirements. - LTG	07-11-28	Thomas M. Hess
D	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-07-25	Thomas M. Hess

CURRENT CAGE CODE IS 67268

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A	PREPARED BY Jeffery Tunstall	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. A. DiCenzo	
	APPROVED BY Nelson A. Hauck	MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, DUAL J-K FLIP-FLOP WITH RESET, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 86-07-02	
	REVISION LEVEL D	SIZE A / CAGE CODE **14933** / **5962-85153**
		SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-85153	01	C	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC73	Dual J-K flip-flop with reset

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage ..... -0.5 V dc to V_{CC} +0.5 V dc
DC output voltage ..... -0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ± 20 mA
DC output current (per pin) ..... ± 25 mA
DC V_{CC} or GND current (per pin) ..... ± 50 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW 3/
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +2.0 V dc to +6.0 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall time:

V_{CC} = 2.0 V ..... 0 to 1000 ns
V_{CC} = 4.5 V ..... 0 to 500 ns
V_{CC} = 6.0 V ..... 0 to 400 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to ground.

3/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.

1.4 Recommended operating conditions – Continued.

Minimum setup time, J or K to clock (t_s):
T_C = +25°C
V_{CC} = 2.0 V ..... 100 ns
V_{CC} = 4.5 V ..... 20 ns
V_{CC} = 6.0 V ..... 17 ns
T_C = -55°C and +125°C
V_{CC} = 2.0 V ..... 150 ns
V_{CC} = 4.5 V ..... 30 ns
V_{CC} = 6.0 V ..... 26 ns

Minimum recovery time, reset to clock (t_{rec}):
T_C = +25°C
V_{CC} = 2.0 V ..... 100 ns
V_{CC} = 4.5 V ..... 20 ns
V_{CC} = 6.0 V ..... 17 ns
T_C = -55°C and +125°C
V_{CC} = 2.0 V ..... 150 ns
V_{CC} = 4.5 V ..... 30 ns
V_{CC} = 6.0 V ..... 26 ns

Minimum clock pulse width (t_{w1}):
T_C = +25°C
V_{CC} = 2.0 V ..... 90 ns
V_{CC} = 4.5 V ..... 18 ns
V_{CC} = 6.0 V ..... 15 ns
T_C = -55°C and +125°C
V_{CC} = 2.0 V ..... 135 ns
V_{CC} = 4.5 V ..... 27 ns
V_{CC} = 6.0 V ..... 23 ns

Minimum reset pulse width (t_{w2}):
T_C = +25°C
V_{CC} = 2.0 V ..... 100 ns
V_{CC} = 4.5 V ..... 20 ns
V_{CC} = 6.0 V ..... 17 ns
T_C = -55°C and +125°C
V_{CC} = 2.0 V ..... 150 ns
V_{CC} = 4.5 V ..... 30 ns
V_{CC} = 6.0 V ..... 26 ns

Minimum hold time, clock to J or K (t_H):
T_C = +25°C
V_{CC} = 2.0 V ..... 25 ns
V_{CC} = 4.5 V ..... 5 ns
V_{CC} = 6.0 V ..... 5 ns
T_C = -55°C and +125°C
V_{CC} = 2.0 V ..... 40 ns
V_{CC} = 4.5 V ..... 8 ns
V_{CC} = 6.0 V ..... 7 ns

Maximum frequency (f_{MAX}):
T_C = +25°C
V_{CC} = 2.0 V ..... 5.4 MHz
V_{CC} = 4.5 V ..... 27 MHz
V_{CC} = 6.0 V ..... 32 MHz
T_C = -55°C and +125°C
V_{CC} = 2.0 V ..... 3.6 MHz
V_{CC} = 4.5 V ..... 18 MHz
V_{CC} = 6.0 V ..... 21 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V	1, 2, 3	4.4		
			$V_{CC} = 6.0$ V	1, 2, 3	5.9		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4.0$ mA	$V_{CC} = 4.5$ V	1, 2, 3	3.7		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -5.2$ mA	$V_{CC} = 6.0$ V	1, 2, 3	5.2		
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = +20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V	1, 2, 3		0.1	
			$V_{CC} = 6.0$ V	1, 2, 3		0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = +4.0$ mA	$V_{CC} = 4.5$ V	1, 2, 3		0.4	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = +5.2$ mA	$V_{CC} = 6.0$ V	1, 2, 3		0.4	
High-level input voltage	V_{IH} 2/		$V_{CC} = 2.0$ V	1, 2, 3	1.5		V
			$V_{CC} = 4.5$ V		3.15		
			$V_{CC} = 6.0$ V		4.2		
Low-level input voltage	V_{IL} 2/		$V_{CC} = 2.0$ V	1, 2, 3		0.3	V
			$V_{CC} = 4.5$ V			0.9	
			$V_{CC} = 6.0$ V			1.2	
Input capacitance	C_{IN}	$V_{IN} = 0.0$ V, $T_C = +25°C$ See 4.3.1c		4		10	pF
Quiescent current	I_{CC}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 6.0$ V		1, 2, 3		80	μA
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 6.0$ V		1, 2, 3		±1.0	μA
Functional tests		See 4.3.1d		7			
Propagation delay, time, $\overline{mCP}$ to mQ or $\overline{mQ}$	t_{PLH1}, t_{PHL1} 3/	$C_L = 50$ pF See figure 4	$V_{CC} = 2.0$ V	9		170	ns
				10, 11		255	
			$V_{CC} = 4.5$ V	9		34	
				10, 11		51	
			$V_{CC} = 6.0$ V	9		29	
				10, 11		43	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay, time, $\overline{mR}$ to mQ or $\overline{mQ}$	t_{PLH2}, t_{PHL2} 3/	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		155	ns
				10, 11		235	
			V_{CC} = 4.5 V	9		31	
				10, 11		47	
			V_{CC} = 6.0 V	9		26	
				10, 11		40	
Transition time, output rise and fall	t_{THL}, t_{TLH} 4/	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		75	ns
				10, 11		110	
			V_{CC} = 4.5 V	9		15	
				10, 11		22	
			V_{CC} = 6.0 V	9		13	
				10, 11		19	

1/ For a power supply of 5.0 V ±10% the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designed with this supply. Worst case V_{IN} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. (The V_{IH} value at V_{CC} = 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 40 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f + I_{CC} V_{CC}$; and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

2/ V_{IH} and V_{IL} tests are not required if applied as a forcing function for V_{OH} or V_{OL}.

3/ Propagation delay times at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the limits specified in table I.

4/ Transition times (t_{TLH}, t_{THL}) shall be guaranteed, if not tested, to the limits specified in table I.

Device type	01	
Case outlines	C	2
Terminal number	Terminal symbol	
1	$\overline{1CP}$	NC
2	$\overline{1R}$	$\overline{1CP}$
3	1K	$\overline{1R}$
4	V_{CC}	1K
5	$\overline{2CP}$	NC
6	$\overline{2R}$	V_{CC}
7	2J	NC
8	$\overline{2Q}$	$\overline{2CP}$
9	2Q	$\overline{2R}$
10	2K	2J
11	GND	NC
12	1Q	$\overline{2Q}$
13	$\overline{1Q}$	2Q
14	1J	2K
15	- - -	NC
16	- - -	GND
17	- - -	NC
18	- - -	1Q
19	- - -	$\overline{1Q}$
20	- - -	1J

NC = No internal connection

FIGURE 1. Terminal connections.

Inputs				Output	
$\overline{mR}$	mCP	mJ	mK	mQ	$\overline{mQ}$
L	X	X	X	L	H
H	↓	L	L	No change	
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	H	H	Toggle	
H	L	X	X	No change	
H	H	X	X	No change	
H	↑	X	X	No change	

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high transition of the clock
↓ = High-to-low transition of the clock

FIGURE 2. Truth table.

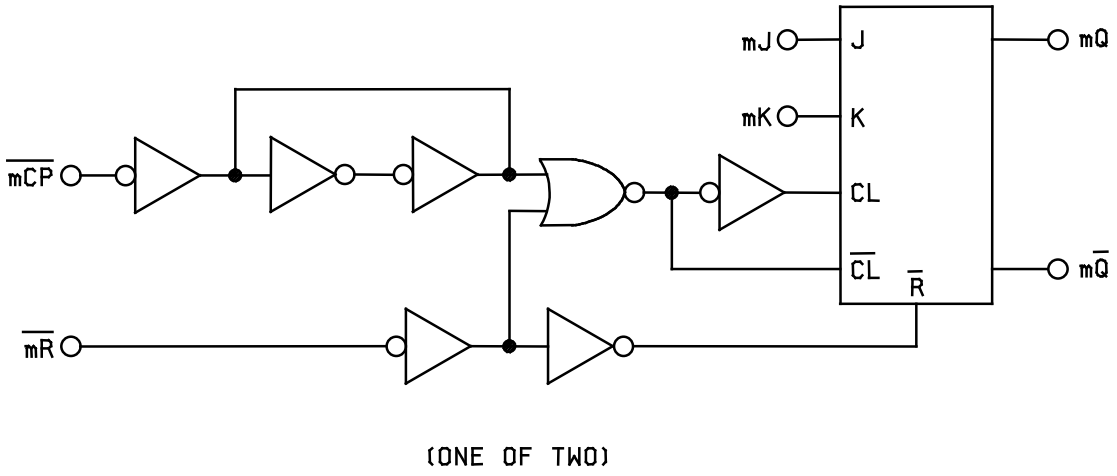
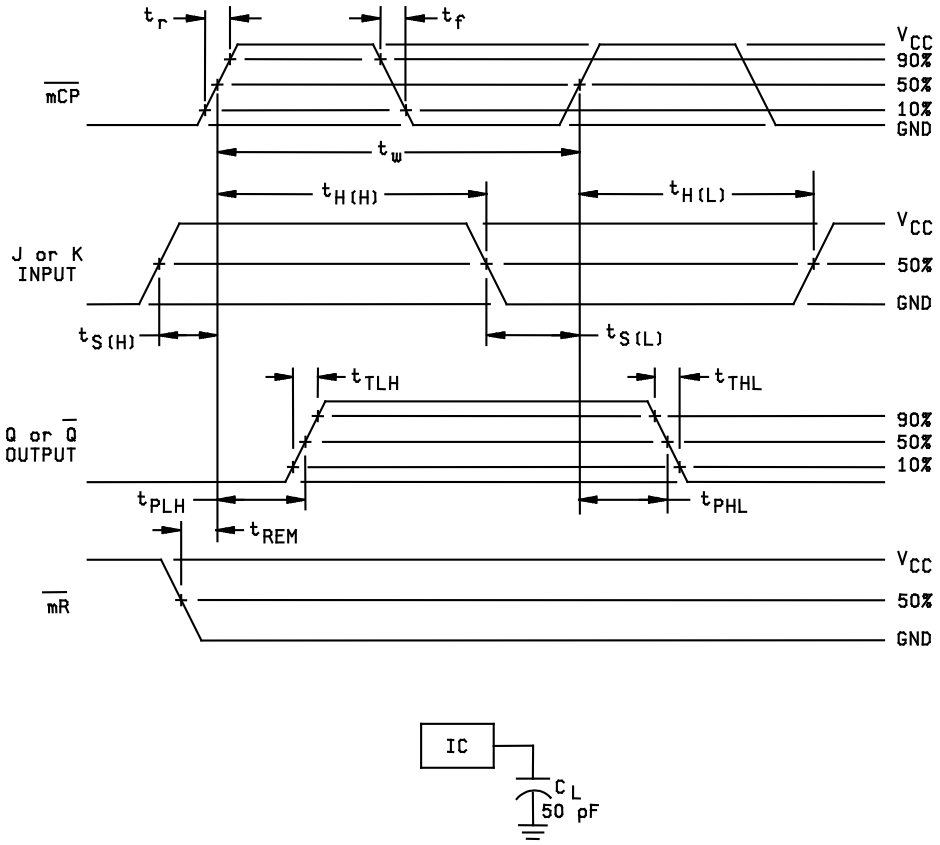


FIGURE 3. Logic diagram.



NOTES:

1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 1MHz; Z_O = 50Ω; t_r = 6.0 ns; t_f = 6.0 ns; t_r and t_f shall be measured from 0.1 V_{CC} to 0.9 V_{CC} and from 0.9 V_{CC} to 0.1 V_{CC}, respectively; duty cycle = 50 percent.
3. The outputs are measured one at a time with one transition per measurement.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	-----
Final electrical test parameters (method 5004)	1, 2, 9 1/
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10, 11 2/
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-07-25

Approved sources of supply for SMD 5962-85153 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8515301CA	01295	CD54HC73F3A
5962-85153012A	3/	MM54HC73E/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.