REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02, 03, and 04. Alter case outlines X and Y dimension tolerances. Change vendor CAGE code. Change drawing CAGE code to 67268. Editorial changes throughout.	89 MAY 05	M. A. Frye

CURRENT CAGE CODE 67268

REV	A	A	A	A	A	A	A	A	A	A	A	A	A					
SHEET	32	33	34	35	36	37	38	39	40	41	42	43	44					
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

REV STATUS OF SHEETS														
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
15 JUNE 1987

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, BIPOLAR, 16 BIT MICRO-PROCESSOR, MIL-STD-1750 INSTRUCTION SET ARCHITECTURE, I^3L, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	84169

SHEET 1 OF 44

* US GOVERNMENT PRINTING OFFICE: 1987--748-129/60912
5962-E1212

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

84169	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device type shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit
01	F9450	15.0 Mhz	16-bit microprocessor with MIL-STD-1750 instruction set architecture
02	F9450	18.0 Mhz	16-bit microprocessor with MIL-STD-1750 instruction set architecture
03	F9450	20.0 Mhz	16-bit microprocessor with MIL-STD-1750 instruction set architecture
04	F9450	15.0 Mhz	16-bit microprocessor with MIL-STD-1750 instruction set architecture

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	64- lead (1.650" x .583" x .180"), dual-in-line package (see figrue 1)
Y	64- lead (1.650" x .583" x .180"), gull wing package (see figrue 1)

1.3 Absolute maximum ratings.

Storage temperature ---------- -65°C to +150°C
V_{CC} pin potential to ground pin ---------- -0.5 V dc to +6.0 V dc
Input voltage range ---------- -0.5 V dc to +5.5 V dc
Input current range ---------- -20mA to +5 mA
Output voltage range (output high) ---------- -0.5 V dc to +5.5 V dc
Output current (output low) ---------- +20mA
Injector current (I_{INJ}) ---------- 1.8 A
Maximum power dissipation (P_D):
  Device type 01 ---------- 3.94 W
  Device type 02, 03, and 04 ---------- 4.26 W
Thermal resistance, junction-to-case (θ_{JC})---------- 2.5°C/W

1.4 Recommended operating conditions.

Supply voltage range ---------- 4.75 V dc minimum to +5.25 V dc maximum
Injector current range (I_{INJ}):
Device types 01 and 04 ---------- .98 A minimum to 1.22 A maximum
Device type 02 ---------- .98 A minimum to 1.28 A maximum
Device type 03 ---------- 1.04 A minimum to 1.28 A maximum
Case operating temperature range (T_C) ---------- -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1750 - Airborne Computer Instruction Set Architecture.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}C$ T_C instant on to $+125^{\circ}C$ T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input high level	V_{IH}	Guaranteed input high	All	1,2,3	2.0		V
Input high level (CPU CLK input only)					2.2		
Input low level	V_{IL}	Guaranteed input low	All	1,2,3		0.8	V
Positive-going threshold voltage USR_0 INT-USR_5 INT, $SYSFLT_0$, $SYSFLT_1$, PWRDN INT	V_{T+}	V_{CC} = 5.0 V I_{INJ} = 1.1 A	All	1,2,3	1.5	2.0	V
Negative-going threshold voltage USR_0 INT-USR_5 INT, $SYSFLT_0$, $SYSFLT_1$, PWRDN INT	V_{T-}	V_{CC} = 5.0 V I_{INJ} = 1.1 A	All	1,2,3	0.6	1.1	V
Input clamp voltage	V_{CD}	I_{IN} = -18 mA V_{CC} = 4.75 V I_{INJ} = 1.1 A	All	1,2,3		-1.5	V
Output high voltage	V_{OH}	I_{IN} = -0.4 mA V_{CC} = 4.75 V I_{INJ} = 1.1 A	All	1,2,3	2.4		V
Output low voltage	V_{OL}	I_{IN} = 8.0 mA V_{CC} = 4.75 V I_{INJ} = 1.1 A	All	1,2,3		0.5	V
Input high current IB_0-IB_{15}, BUS BUSY, BUS LOCK	I_{IH1}	V_{IN} = 2.7 V, V_{CC} = 5.25 V I_{INJ} = 1.1 A	All	1,2,3		40	μA
Input high current except IB_0-IB_{15}, BUS BUSY, BUS LOCK	I_{IH2}	V_{IN} = 2.7 V, V_{CC} = 5.25 V I_{INJ} = 1.1 A	All	1,2,3		100	μA
Input high current all inputs	I_{IH3}	V_{IN} = 5.25 V, V_{CC} = 5.25 V I_{INJ} = 1.1 A	All	1,2,3		1.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T_C instant on to +125°C T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Input low current	I_{IL}	V_{IN} = 0.4 V V_{CC} = 5.25 V I_{INJ} = 1.1 A		All	1,2,3		-400	µA
Output 3-state current IB_0-IB_{15}, BUS BUSY, BUS LOCK	I_{OZH1}	V_{OUT} = 2.4 V V_{CC} = 5.25 V	I_{INJ} = 1.1 A	01, 04	1,2,3		140	µA
			I_{INJ} = 1.16A	02, 03				
Output 3-state current AK_0-AK3, AS_0 AS3,R/W, M/IO, D/I STRBA, STRBD	I_{OZH2}	V_{OUT} = 2.4 V V_{CC} = 5.25 V	I_{INJ} = 1.1 A	01, 04	1,2,3		100	µA
			I_{INJ} = 1.16A	02, 03				
Output 3-state current IB_0-IB_{15}, BUS BUSY, BUS LOCK	I_{OZL1}	V_{OUT} = 0.5 V V_{CC} = 5.25 V	I_{INJ} = 1.1 A	01, 04	1,2,3		-500	µA
			I_{INJ} = 1.16A	02, 03				
Output 3-state current AK_0-AK3, AS_0 AS3,R/W, M/IO, D/I STRBA, STRBD	I_{OZL2}	V_{OUT} = 0.5 V V_{CC} = 5.25 V	I_{INJ} = 1.1 A	01, 04	1,2,3		-100	µA
			I_{INJ} = 1.16A	02, 03				
Output short circuit (not more than one output shorted at one time)	IOSH	V_{OUT} = 0 V V_{CC} = 5.25 V	I_{INJ} = 1.1 A	01, 04	1,2,3	-15	-125	mA
			I_{INJ} = 1.16A	02, 03				
Power supply current	I_{CC}	V_{CC} = 5.25 V T_C = -55°C	I_{INJ} = 1.1 A	01	1,2,3		390	mA
			I_{INJ} = 1.16A	02,03, 04			450	
		V_{CC} = 5.25 V T_C = +125°C	I_{INJ} = 1.1 A	01	1,2,3		260	
			I_{INJ} = 1.16A	02,03, 04			290	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T_C instant on to +125°C T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Injector voltage 1/	V_{INJ}	V_{CC} = 5.25 V 1/	I_{INJ} = 0.98 A	01,02,04	1,2,3	1.2	1.43	V
			I_{INJ} = 1.04 A	03				
		V_{CC} = 5.25 V 1/	I_{INJ} = 1.22 A	01, 04	1,2,3	1.34	1.55	
			I_{INJ} = 1.28 A	02, 03				
Propagation delay from clock								
M/IO, D/I, R/W, AS_0-AS_3, AK_0-AK_3 (STATUS)	$t_{c(M)}$	See figure 4 2/		01	9,10,11		60	ns
				02,03,04			55	
BUS REQ	$t_{c(BR)}$			01	9,10,11		45	
				02,03,04			40	
BUS BUSY	$t_{c(BB)}$			01	9,10,11		55	
				02,03,04			40	
BUS BUSY, three-state	$t_{c(BB)z}$			01	9,10,11		35	
				02,03,04			30	
BUS LOCK	$t_{c(BL)}$			01	9,10,11		50	
				02,03,04			35	
BUS LOCK, three-state	$t_{c(BL)z}$			01	9,10,11		40	
				02,03,04			35	
IB_0-IB_{15} address	$t_{c(IBA)v}$			01	9,10,11		65	
				02,03,04			55	
IB_0-IB_{15} address, three-state	$t_{c(IBA)z}$			01	9,10,11		75	
				02,03,04			60	
STRBA low	$t_{c(SA)l}$			01	9,10,11		25	
				02,03,04			20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T_C instant on to +125°C T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay from clock - continued							
STRBA high	$t_{c(SA)h}$	See figure 4 2/	All	9,10,11		35	ns
STRBA, three-state	$t_{c(SA)z}$		01	9,10,11		40	
			02,03,04			30	
IB_0-IB_{15} data	$t_{c(IBD)v}$		01	9,10,11		60	
			02,03,04			55	
IB_0-IB_{15} data, three-state	$t_{c(IBD)z}$		01	9,10,11		45	
			02,03,04			40	
STRBD low (read)	$t_{c(SDr)l}$		01	9,10,11		85	
			02,03,04			65	
STRBD high (read)	$t_{c(SDr)h}$		01	9,10,11		45	
			02,03,04			35	
STRBD low (write)	$t_{c(SDw)l}$		01	9,10,11		50	
			02,03,04			40	
STRBD high (write)	$t_{c(SDw)h}$		01	9,10,11		40	
			02,03,04			35	
STRBD three-state	$t_{c(SD)z}$		01	9,10,11		40	
			02,03,04			35	
SNEW	$t_{c(SNW)}$		01	9,10,11		75	
			02,03,04			65	
TRIGO RST	$t_{c(TGO)}$		01	9,10,11		70	
			02,03,04			60	
DMA EN	$t_{c(DME)}$		01	9,10,11		60	
			02,03,04			50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T_C instant on to +125°C T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay from clock - continued							
NML PWRUP	$t_{c(NPU)}$	See figure 4 2/	01	9,10,11		70	ns
			02,03,04			60	
MAJ ER, UNRCV ER	$t_{c(ER)}$		01	9,10,11		100	
			02,03,04			85	
Status three-state	$t_{c(M)z}$		All	9,10,11		40	
Other timing parameters							
STRBD pulse width, write cycle 3/	$t_{SDl(SD)h}$	See figure 4 2/	01	9,10,11	55		ns
			02		50		
			03		45		
			04		60		
DATA valid to STRBD high (write) 3/	$t_{BDv(SDw)h}$		01,04	9,10,11	90		
			02		80		
			03		70		
AD_DRES_S valid to STRBA low 3/	$t_{BAv(SA)l}$		01	9,10,11	10		
			02		5		
			03,04		5		
AD_DRES_S valid after STRBA hold time 3/	$t_{SAl(IBA)x}$		All	9,10,11	5		
Status valid to STRBA low 3/	$t_{Mv(SA)l}$		01	9,10,11	20		
			02,03,04		10		
STRBD high (write) to DATA invalid	$t_{SDwh(IBD)x}$		All	9,10,11	40		
DATA don't care to STRBD high (read)	$t_{IBDx(SDr)h}$		All	9,10,11	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T_C instant on to +125°C T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Other timing parameters - continued							
Memory or I/O system time 4/	t_{MEM}	See figure 4 2/	01, 04	9,10,11	135		ns
			02		105		
			03		90		
Pulse width, edge-sensitive Fault or Interrupt	$t_{F(F)}$, $t_{I(I)}$		All	9,10,11		30	
Setup time before clock (unless otherwise specified)							
RDYA	$t_{RAv(C)}$	See figure 4 2/	All	9,10,11		30	ns
RDYD	$t_{RDv(C)}$		All	9,10,11		30	
IBO_0-IB_{15} data in	$t_{IBDv(C)}$		01	9,10,11		0	
			02,03,04			5	
CON REQ	$t_{REQv(C)}$		All	9,10,11		0	
RESET	$t_{RSv(C)}$		01	9,10,11		10	
			02,03,04			20	
BUS LOCK	$t_{BLv(C)}$		All	9,10,11		25	
BUS GNT	$t_{BGv(C)}$		All	9,10,11		25	
PWRDN INT, USR INT (level-sense)	$t_{IRv(C)}$		All	9,10,11		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T_C instant on to +125°C T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Setup time before clock (unless otherwise specified) - continued							
Level-sensitive faults (before external BUS BUSY)	$t_{Fv(BB)h}$	See figure 4 2/	01	9,10,11		70	ns
			02,03,04			60	
Level-sensitive fault, MEM PRT ER, EXT ADR ER	$t_{Fv(C)}$		All	9,10,11		35	
IOL_1INT, IOL_2INT	$t_{IRLv(C)}$		All	9,10,11		0	
PAR ER load FT, generate UNRCV ER	$t_{PARv(C)}$		01	9,10,11		5	
			02,03,04			10	
PAR ER inhibit register load			01	9,10,11		20	
			02,03,04			10	
Hold time after clock (unless otherwise specified)							
RDYA	$t_{C(RA)}$	See figure 4 2/	All	9,10,11		0	ns
RDYD	$t_{C(RD)x}$		All	9,10,11		0	
IBO_0-IB_{15} data in	$t_{C(IBD)x}$		01	9,10,11		25	
			02,03,04			20	
CON REQ	$t_{C(REQ)x}$		01	9,10,11		40	
			02,03,04			35	
RESET	$t_{C(RS)x}$		01	9,10,11		15	
			02,03,04			20	
BUS LOCK	$t_{C(BL)x}$		All	9,10,11		0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

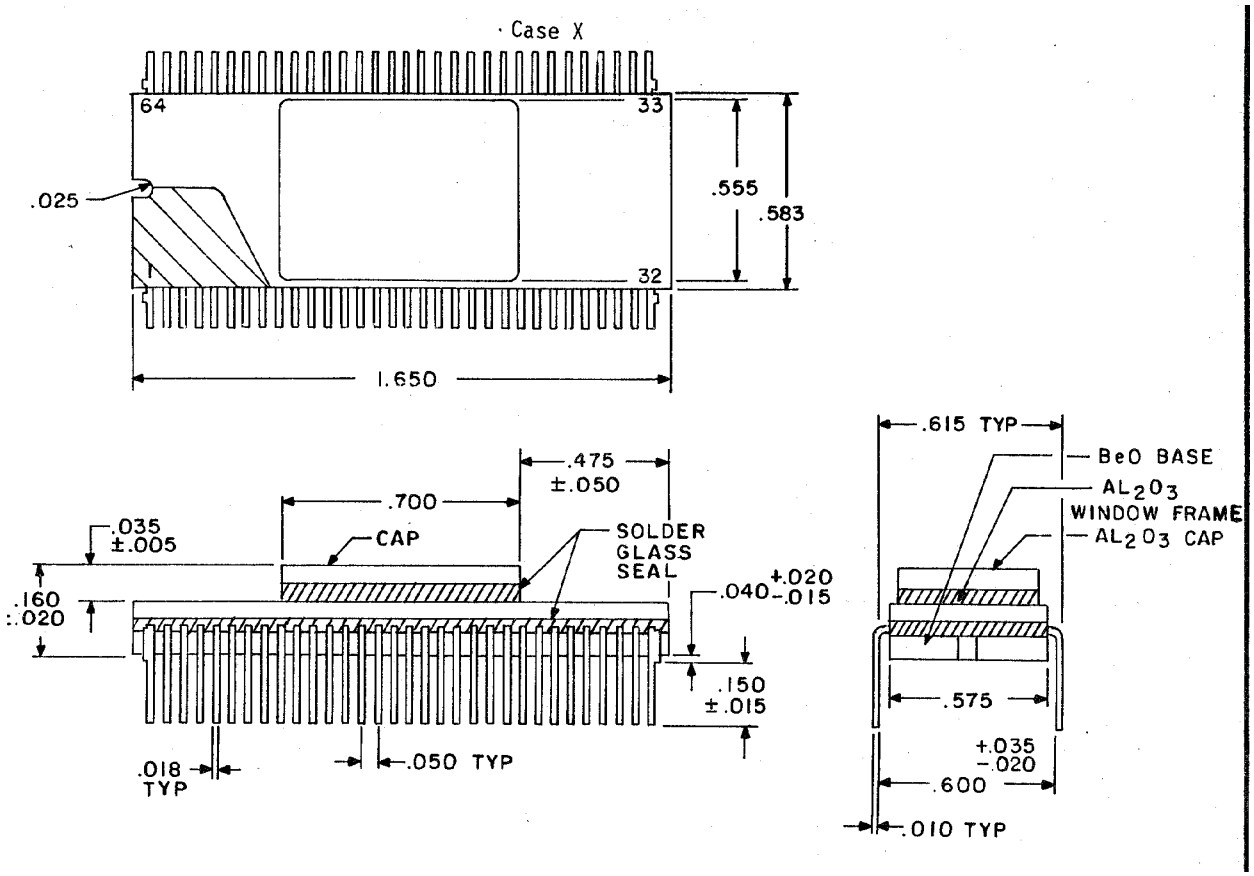
Test	Symbol	Conditions -55°C T_C instant on to +125°C T_C operating V_{CC} = 5.0 V ±5% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Hold time after clock (unless otherwise specified)							
BUS GNT	$t_{C(BG)x}$	See figure 4 2/	All	9,10,11		0	ns
PWRDN INT, USR INT (level-sense)	$t_{C(IR)x}$		01	9,10,11		40	
			02,03,04			35	
Level-sensitive faults (after BUS BUSY)	$t_{BBh(F)x}$		All	9,10,11		0	
IOL_1INT, IOL_2INT	$t_{C(IRL)x}$		01	9,10,11		40	
			02,03,04			35	

1/ The value specified for VINJ is a static value (CPU CLK = 0). The I^3L design of the F9450 requires a constant current source for I_{INJ}. Because the electrical grounds for both I^3L and TTL technologies are connected on the die, switching of the TTL output buffers may cause noise at IB bus frequency, approximately 450 mV above the specified value for V_{INJ}. This noise value should not be added to V_{INJ} for purposes of calculation of power supply requirements, as the 450 mV noise is caused by electrical ground rising within the F9450.

2/ See figure 4 switching time test circuits.
Input conditioning: Rise and fall time = 6 ns, amplitude = 0 to 3 volts.
Measurements taken at the 1.5 V level.
Clock period (CPRD) = 1/Fmax; Fmax = up to 15 MHz for device types 01 and 04.
18 MHz for device type 02.
20 Mhz for device type 03.
Clock pulse width (CPW) = 40 percent to 60 percent of CPRD.

3/ The parameters are CPRD dependent, values listed are at 15 Mhz (CP_{RD} of 65 ns) for device types 01 and 04; 18 Mhz (CPRD of 55 ns) for device type 02; 20 Mhz (CPRD of 50 ns) for device type 03.

4/ Memory or I/O system time is the elasped time from valid address to required valid data, during a read cycle, without additional wait states. If additonal time is required for either memory or I/O, it can be obtained through the addition of wait states in either the address or data time.

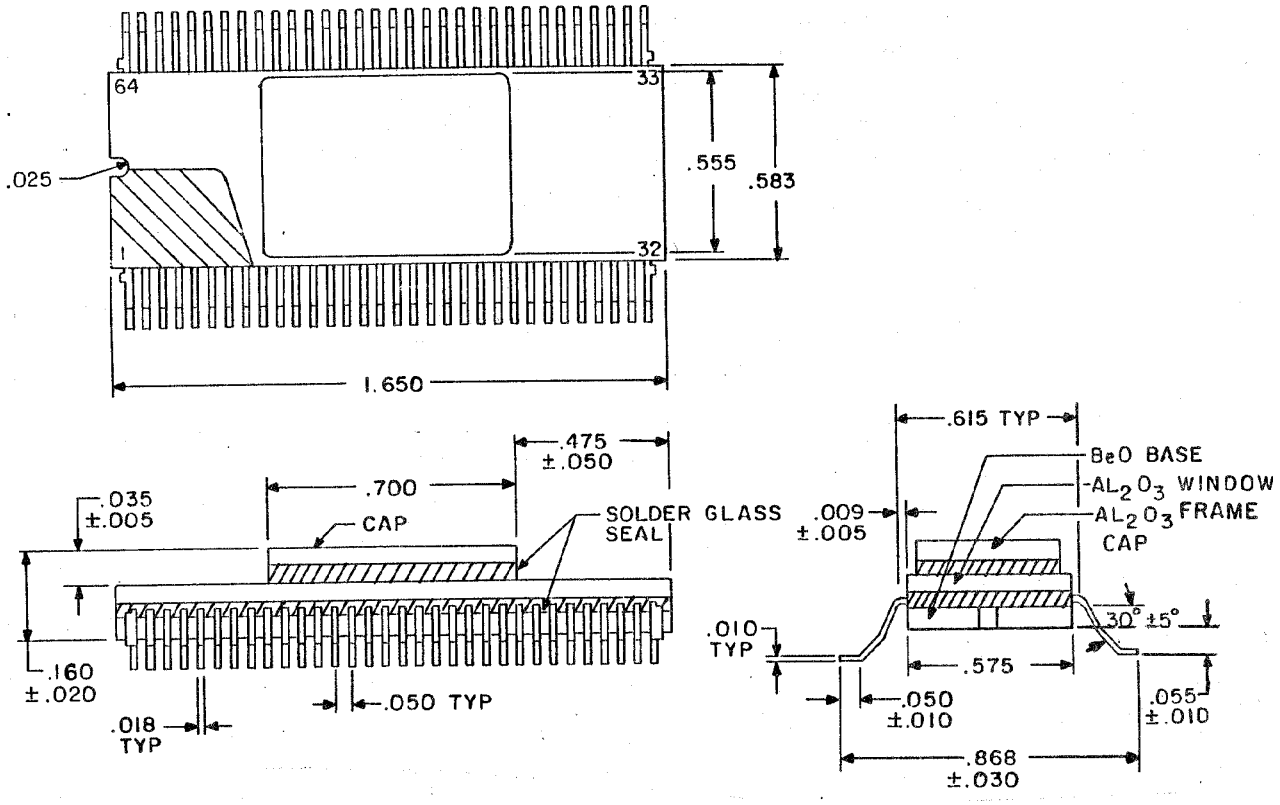


Notes:

1. All dimensions are in inches.
2. Lead finsh: Hot solder dip in accordance with MIL-M-38510.
3. Cap is ceramic.
4. Base is BeO.
5. Package weight is 8.5 grams.
6. A pin one identification mark shall be located adjacent to pin one and shall be located in the shaded area shown.
7. The letters "BeO" shall be located adjacent to pin 64.
8. Dimension tolerances ±.010 inch unless otherwise shown.

Inches	mm
.005	0.13
.010	0.25
.015	0.38
.018	0.46
.020	0.51
.025	0.64
.035	0.89
.040	1.02
.050	1.27
.150	3.81
.160	3.81
.475	3.81
.555	3.81
.575	3.81
.583	3.81
.600	3.81
.615	3.81
.700	3.81
1.650	3.81

FIGURE 1. Case outlines.



Notes:
1. All dimensions are in inches.
2. Lead finsh: Hot solder dip in accordance with MIL-M-38510.
3. Cap is ceramic.
4. Base is BeO.
5. Package weight is 8.5 grams.
6. Plane of lead "feet" parallel to bottom surface of BeO base ±5°.
7. A pin one identification mark shall be located adjacent to pin one and shall be located in the shaded area shown.
8. The letters "BeO" shall be located adjacent to pin 64.
9. Dimension tolerances ±.010 inch unless otherwise shown.

Inches	mm
.005	0.13
.009	0.23
.010	0.25
.018	0.46
.020	0.51
.025	0.64
.030	0.76
.035	0.89
.050	1.27
.055	1.40
.100	2.54
.475	12.08
.555	14.10
.575	14.61
.583	14.81
.615	15.62
.700	17.78
.868	22.05
1.650	41.91

FIGURE 1. Case outlines - Continued.

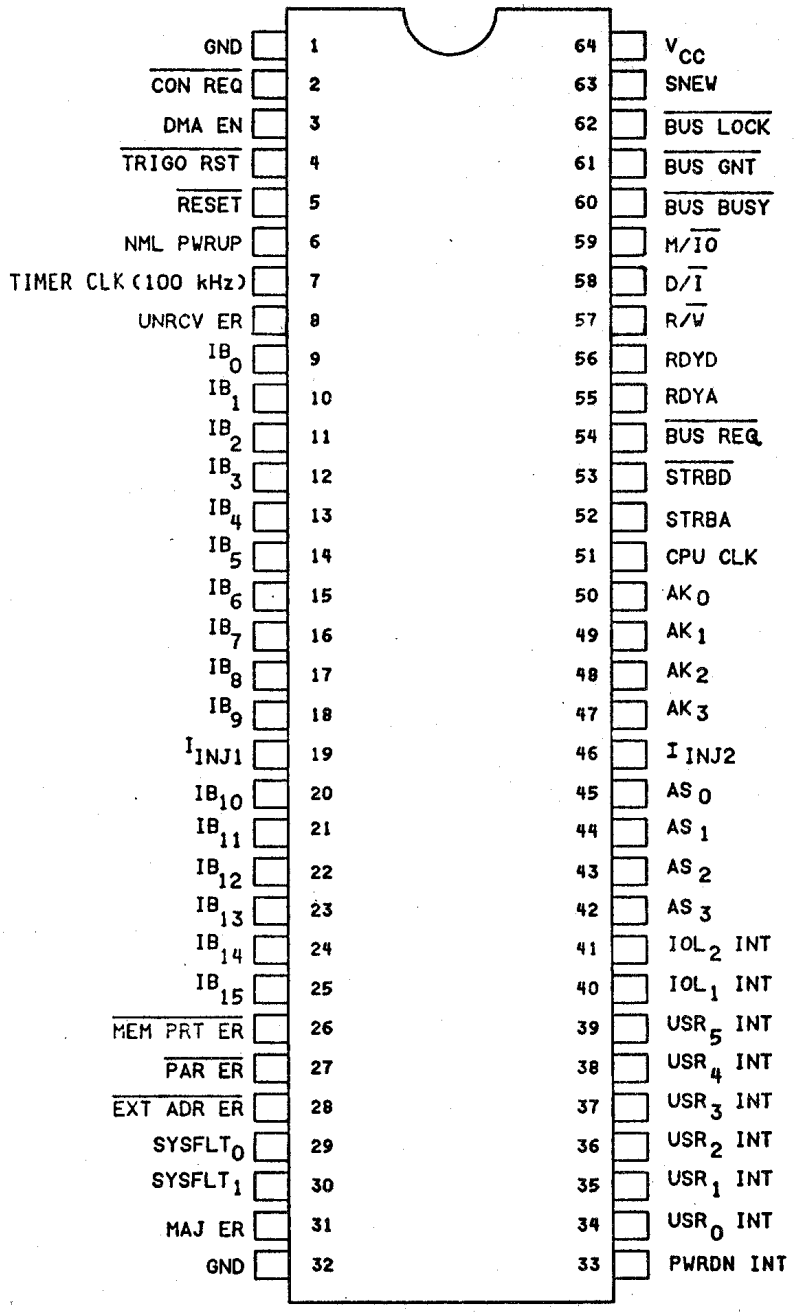


FIGURE 2. Terminal connections.

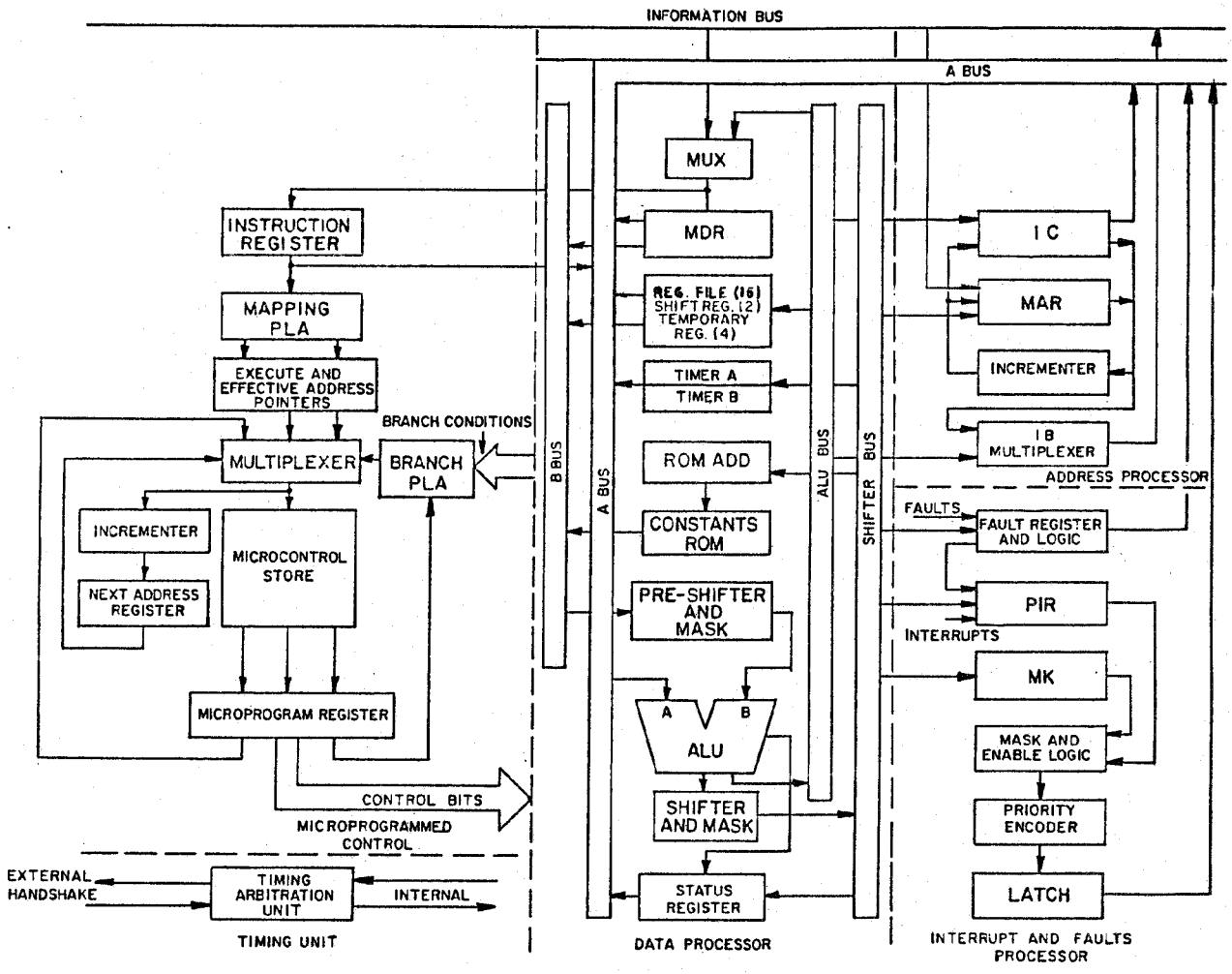


FIGURE 3. Functional block diagram.

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		REVISION LEVEL A	SHEET 15

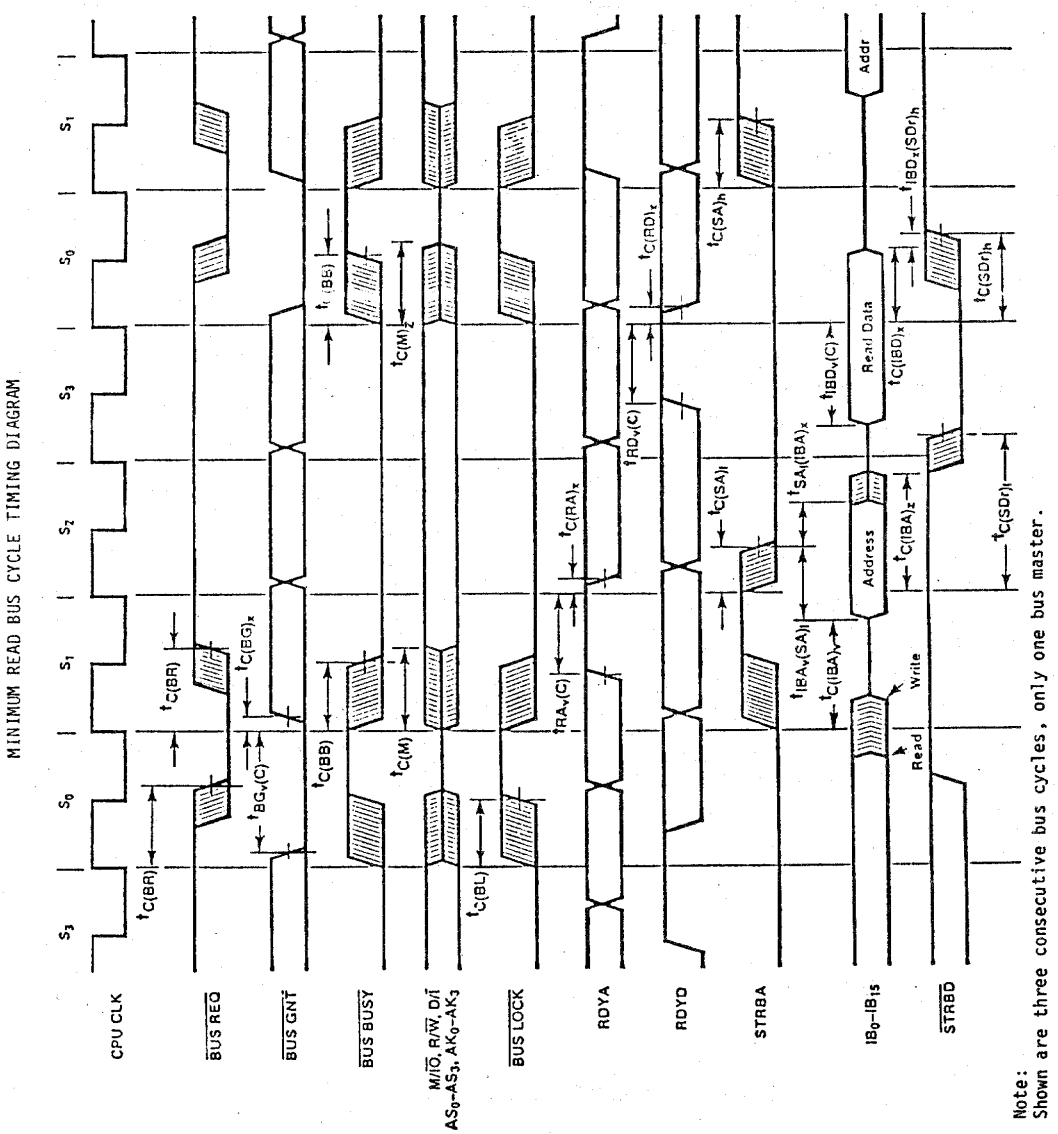
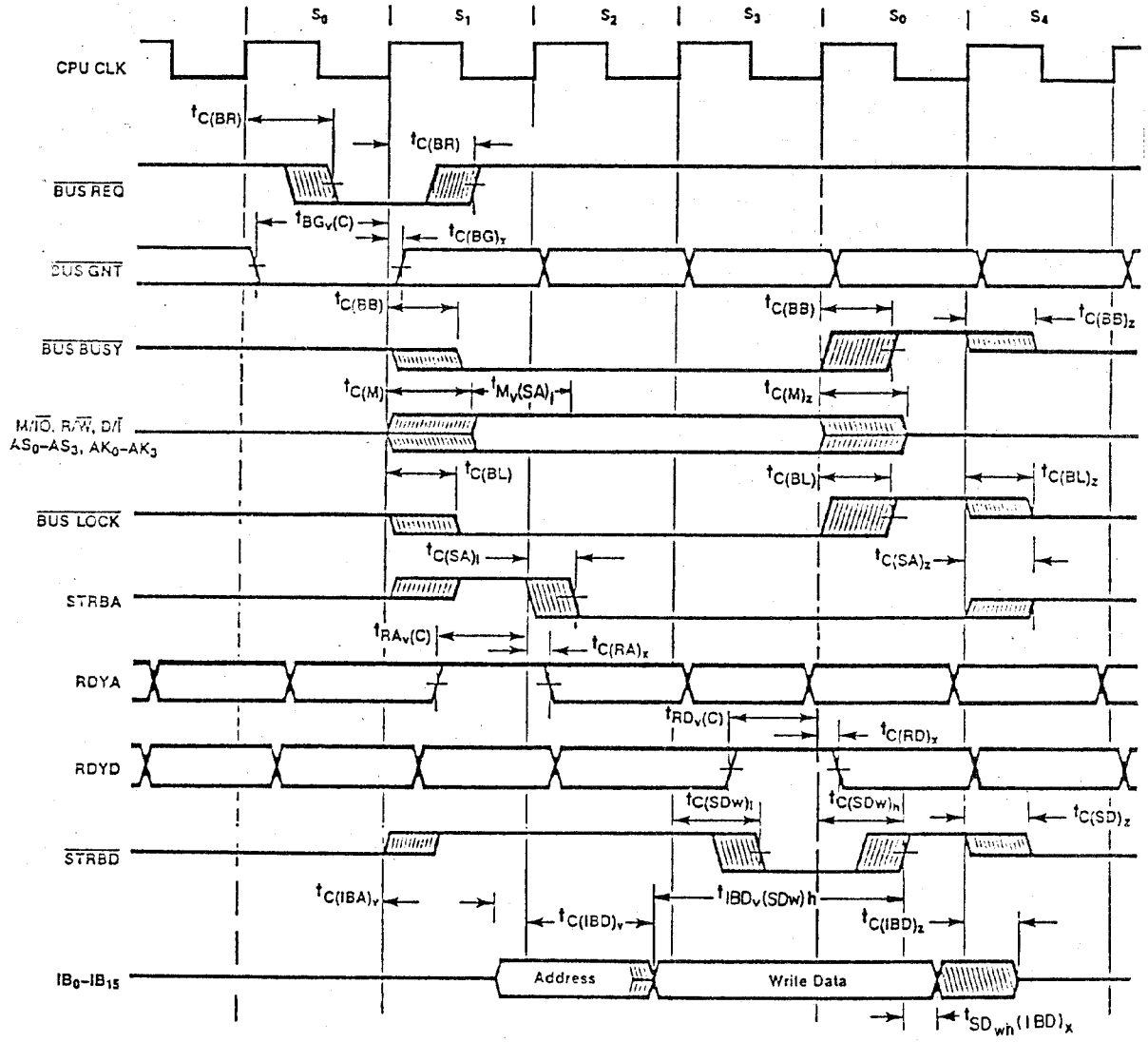


FIGURE 4. Timing waveforms

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84169
		REVISION LEVEL A	SHEET 16

MINIMUM WRITE BUS CYCLE TIMING DIAGRAM

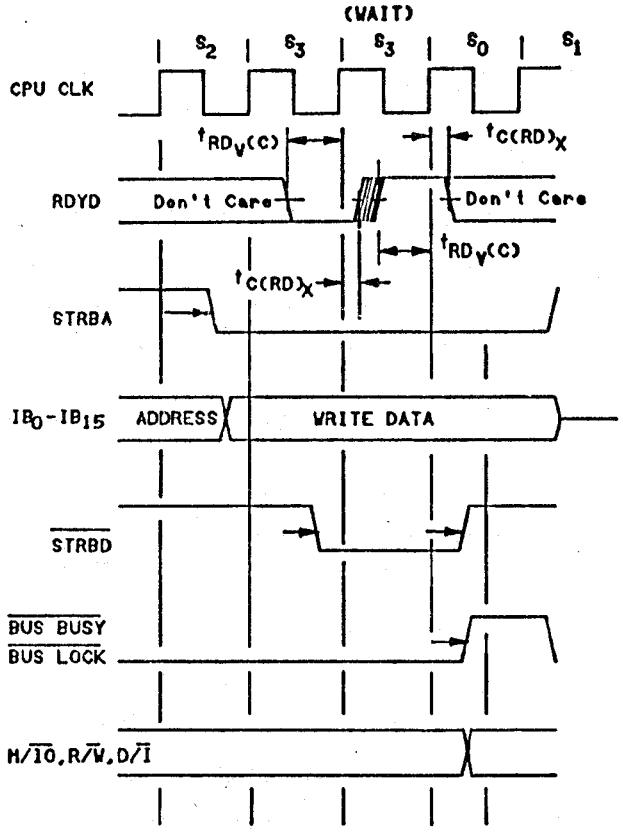


NOTES:

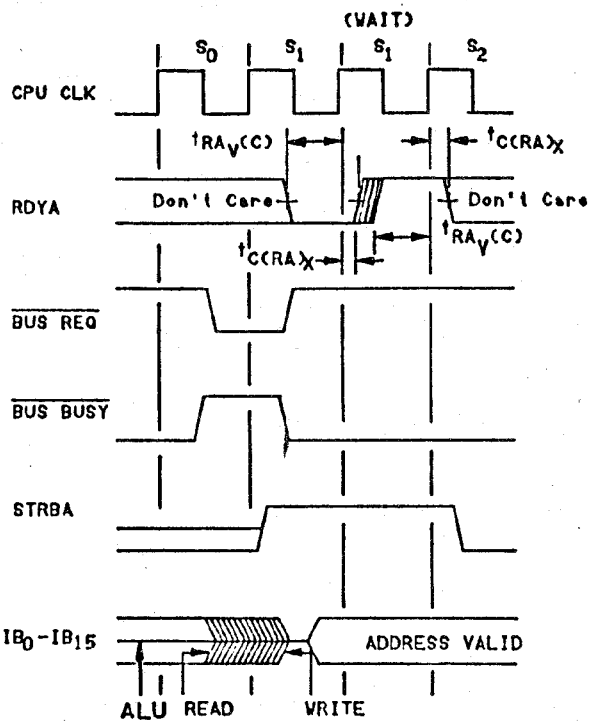
1. Shown is a single isolated bus cycle, only one bus master.
2. An intermediate level indicates that the CPU has placed this signal in a three-state condition.

FIGURE 4. Timing waveforms - Continued.

RDYD SIGNAL - WRITE BUS CYCLE TIMING DIAGRAM



RDYA SIGNAL TIMING DIAGRAM



RDYD SIGNAL - READ BUS CYCLE TIMING DIAGRAM

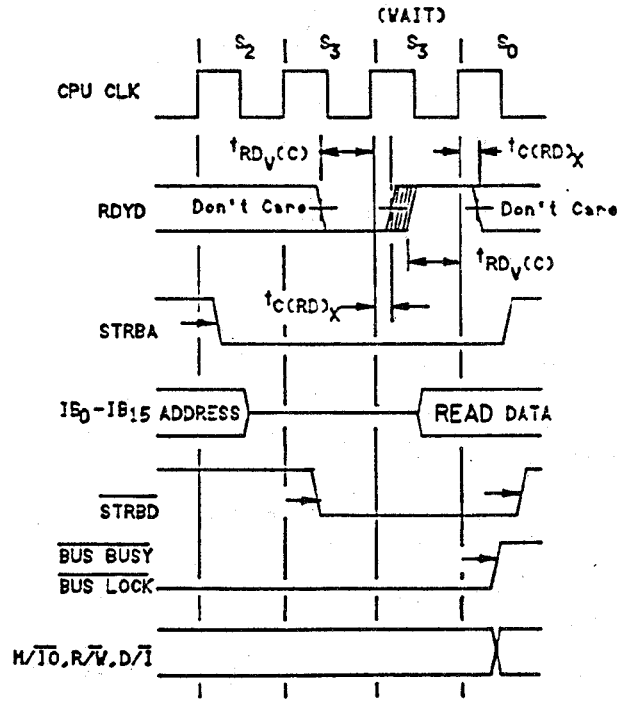
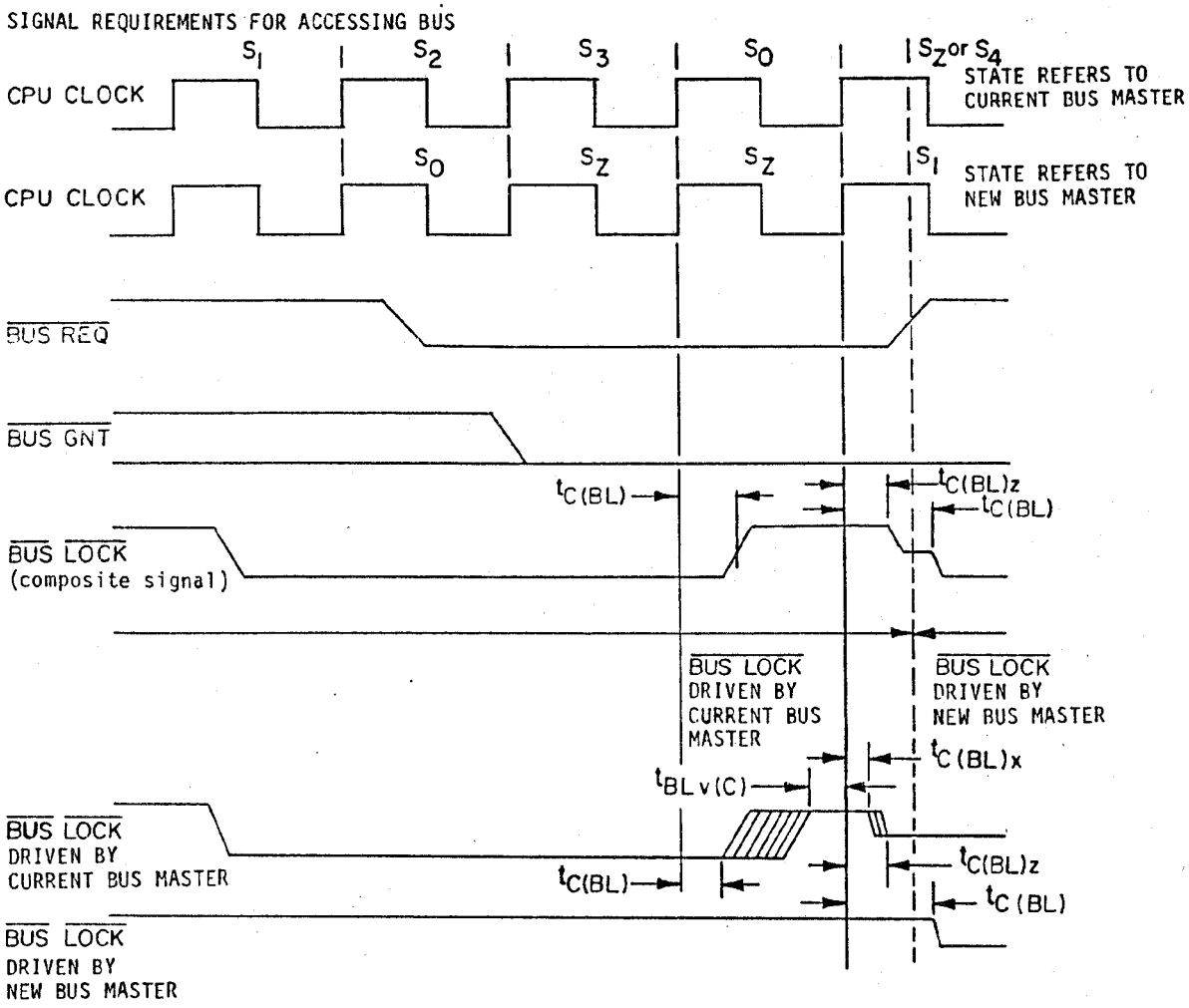


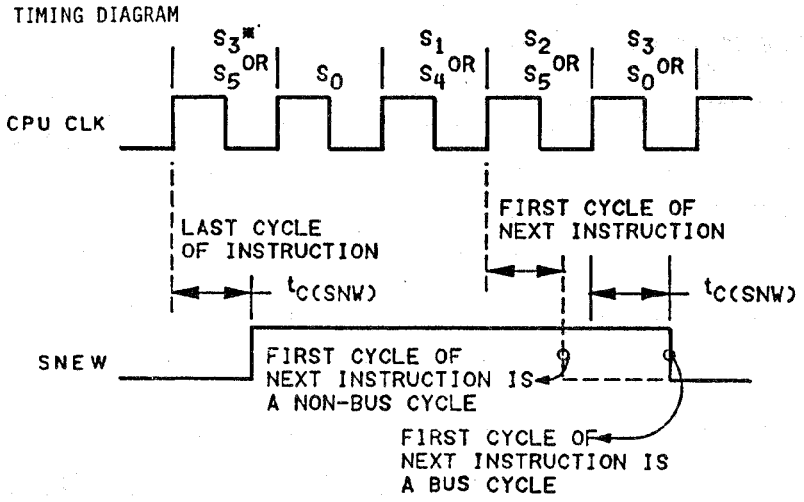
FIGURE 4. Timing waveforms - Continued.



NOTES:
1. Shown is device response to external control of the BUS LOCK signal. Note that current bus master must release active drive of BUS LOCK before new bus master begins driving.
2. All device masters are F9450 or F9450 bus-compatible devices.
3. Bus masters and external arbiter are operating on the same clock.
4. State Sz is the high-impedance state in which all new bus master drivers are in a three-state condition.
5. tBLv(C) and tC(BL)x are measured as inputs to new bus master.

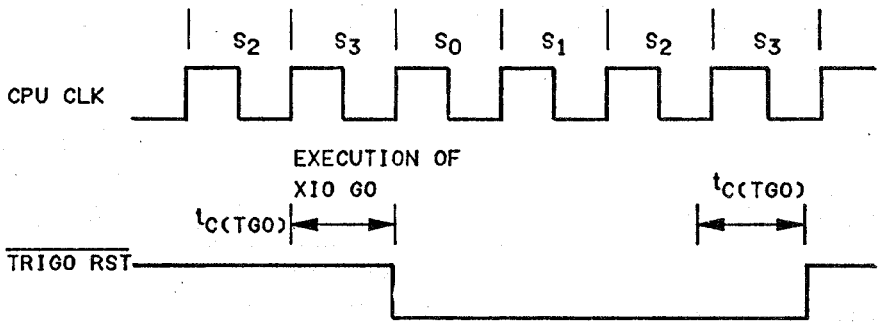
FIGURE 4. Timing waveforms - Continued.

SNEW DISCRETE TIMING DIAGRAM



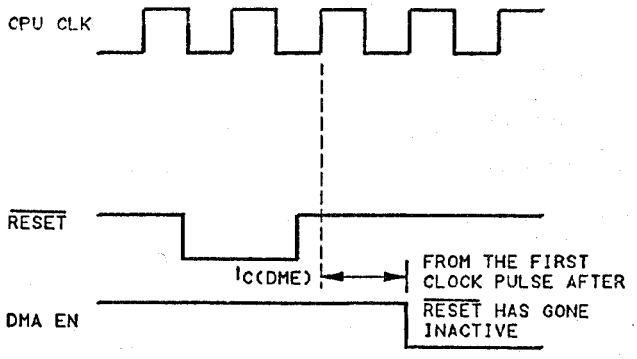
*If wait states are included in the data time of the previous cycle, this will be the first S3 state.

$\overline{\text{TRIGO RST}}$ DISCRETE TIMING DIAGRAM



DMA EN DISCRETE TIMING DIAGRAM

A) DURING RESET



B) XIO OPERATIONS

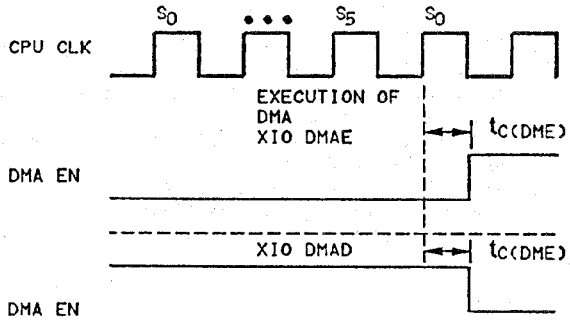


FIGURE 4. Timing waveforms - Continued.

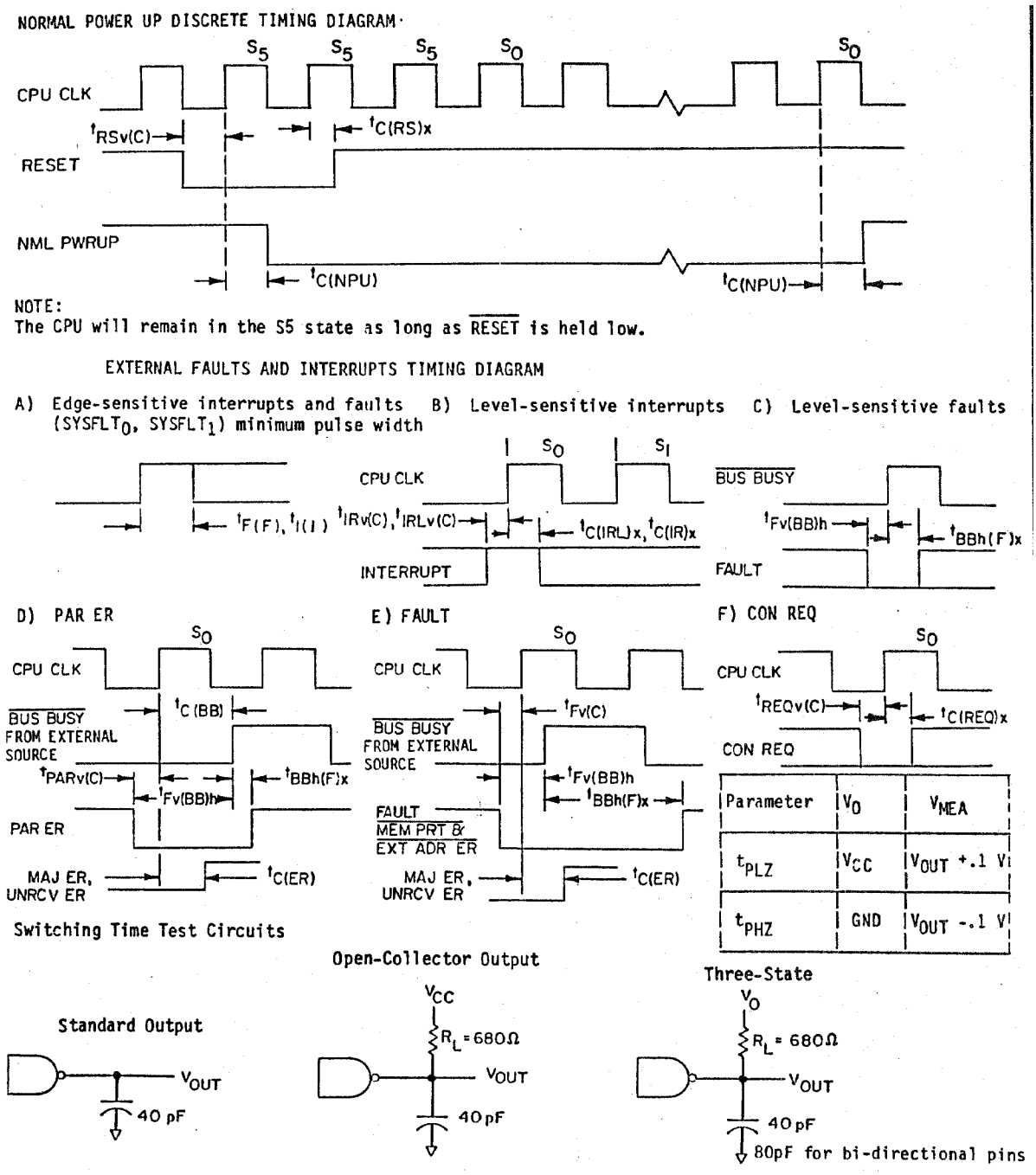


FIGURE 4. Timing waveforms - Continued.

3.7 Certification. Certification to MIL-STD-1750 verification software (VSW) test V 2.1 +2 shall be required and the manufacturer shall be listed on the Air Force VSW compliant computer list. For device types 02, 03 and 04, MIL-STD-1750 verification software (VSW) test V 2.1 +12 is applicable.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Instruction set and instruction-execution times for all device types.

3.10.1 Word key.

Instruction Set

The instruction set of the F9450 is optimized for real-time applications in accordance with the MIL-STD-1750A ISA. Table 1 shows addressing modes and related instruction word formats, Derived Address (DA), and Derived Operand (DO). Not all insructions use all the addressing modes; therefore, acceptable addressing modes should be confirmed for each instruction. Table 2 provides the instruction set with applicable addressing modes and table 3 gives the dedicatied I/O addresses.

Addressing Modes

There are ten addressing modes. The smallest addressable memory word is 16 bits. Therefore, the 16-bit address field allows direct addressing of 64K words. There is no restriction on the location of double-word operands in memory.

1. Register Direct (R)
   The instruction-specified register contains the required operand. With the exception of this mode, the DA denotes a memory address.

2. Memory Direct (D)
   In this mode, the instruction contains the memory address of the operand.

3. Memory Direct - Indexed (DX)
   The memory address of the required operand is specified by the sum of the contents of an index register and the instruction address field. Registers R1 through R15 may be specified for indexing.

4. Memory Indirect (I)
   The instruction-specified memory address contains the address of the required operand.

5. Memory Indirect with Pre-Indexing (IX)
   The sum of the contents of a specified index register and the instruction address field specify the address of a memory location containing the address of the required operand. Registers R1 through R15 may be specified for pre-indexing.

6. Immediate Long (IM)
   One method of Immediate Long addressing allows indexing and one does not. The indexable form of immediate addressing is shown in table 3. If the specified index register, RX, is $\neq 0$, the contents of RX is added to the immediate field to form the required operand; otherwise, the immediate field contains the required operand.

7. Immediate Short (IS)
   The required 4-bit operand is contained within the 16-bit instruction. One method of immediate Short addressing interprets the contents of the immediate field as positive data and another method interprets the contents of the immediate field as negative data.

   a. Immediate Short Positive (ISP)
      The immediate operand is treated as a positive integer between 1 and 16.

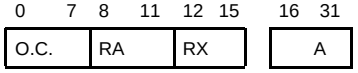
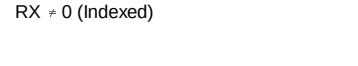
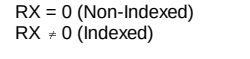
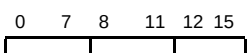
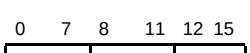
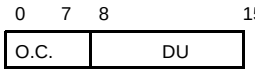
   b. Immediate Short Negative (ISN)
      The immediate operand is treated as a positive integer between 1 and 16. Its internal form is a twos-complement, sign-extended 16-bit number.

8. Instruction Counter Relative (ICR)
   This mode is used for 16-bit branch instructions. The contents of the instruction counter minus one (i.e., the address of the current instruction) are added to the sign-extended 8-bit displacement field of the instruction. The sum points to the memory address to which control may be transferred if a branch is executed. This mode allows addressing within a memory region of -128 to +127 words, relative to the address of the current instruction.

9. Base Relative (B)
   The contents of an instruction-specified base register are added to the 8-bit displacement field of the 16-bit instruction. The displacement field is taken to be a positive number between 0 and 255. The sum points to the memory address of the required operand. This mode allows addressing within a memory region of 256 words, beginning at the address pointed to by the base register.

10. Base Relative - Indexed (BX)
    The sum of the contents of a specified index register and a specified base register is the address of the required operand. Registers R1 through R15 may be specified for indexing.

3.10.2 Addressing modes and instruction formats.

Mode	Format	Derived Operand (DO) Single-Precision	Derived Operand (DO) Floating-Point and Double Precision	Derived Address (DA) Single-Precision	Derived Address (DA) Floating-Point and Double Precision
1. Register Direct "R"		(RB)	(RB, RB + 1)	RB	RB, RB + 1
2. Memory Direct "D" "DX"	 RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)	[A] [A + (RX)]	[A, A + 1] [A+ (RX),A + 1 + (RX)]]	A A + (RX)	A, A + 1 A + (RX), A + 1 + (RX)
3. Memory Indirect "I" "IX"	 RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)	[|A|] [|A+(RX)|]	[|A|, |A| + 1] [|A + (RX)|, |A + (RX)| + 1]	[A] [A + (RX)]	[A], [A] + 1 [A + (RX)], [A + (RX)] + 1
4. Immediate Long					
a. Not indexable "IM"		I			
b. Indexable "IM" "IMX"	 RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)	I I + (RX)			
5. Immediate Short					
a. Positive "ISP"		+ (I + 1)			
b. Negative "ISN"		- (I + 1)			
6. IC Relative (1) "ICR"				DU + (IC - 1)	
7. Base Relative (2)					
a. Not Indexable (3) "B"	 BR = BR + 12	[DU + (BR)]	[DU + (BR), DU + 1 + (BR)]	DU + (BR)	DU + (BR), DU + 1 + (BR)
b. Indexable "B" "BX"	 RX = 0 (Non-Indexed) RX ≠ 0 (Indexed)	[(BR)] [(BR)+(RX)]	[(BR), (BR) + 1] [(BR)+(RX), (BR) +1+(RX)]	(BR) (BR) + (RX)	(BR), (BR) + 1 (BR) + (RX),BR) + 1+(RX)

Notes:
1. -128 ≤ DU ≤ 127.
2. Base registers: BR = R12, R13, R14, and R15.
3. 0 ≤ DU ≤ 255.
4. Extended-precision floating-point instructions require addressing of three operands located at DA, DA + 1, and DA + 2.

3.10.3 Instruction execution times.

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
		INTEGER ARITHMETIC/LOGIC				
Single-Precision Add	A	R	1	0	5	Nf/N6
	A	B	1	1	12	Nf/N6
	A	BX	1	1	12	Nf/N6
	A	ISP	1	0	8	Nf/N6
	A	D	2	1	13	Nf/N6
	A	DX	2	1	13	Nf/N6
	A	IM	2	0	12	Nf/N6
Double-Precision Add	DA	R	1	0	18	
	DA	D	2	2	24	
	DA	DX	2	2	24	
Increment Memory by	INCM	D	2	2	17	Nf/N6 Bus Lock
Positive Integer	INCM	DX	2	2	17	Nf/N6 Bus Lock
Single-Presicion ABS	R	1	0	5	Nf/N6 , Pos.#	
Absolute Value	ABS	R	1	0	10	Nf/N6 , Neg.#
Double-Precision	DABS	R	1	0	13	Pos. #
Absolute Value	DABS	R	1	0	21	Neg. #
Single-Precision Subtract	S	R	1	0	5	Nf/N6
	S	B	1	1	12	Nf/N6
	S	BX	1	1	12	Nf/N6
	S	ISP	1	0	8	Nf/N6
	S	D	2	1	13	Nf/N6
	S	DX	2	1	13	Nf/N6
	S	IM	2	0	12	Nf/N6
Double-Precision Subtract	DS	R	1	0	18	
	DS	D	2	2	24	
	DS	DX	2	2	24	
Decrement Memory by	DECM	D	2	2	17	Nf/N6 Bus Lock
Positive Integer	DECM	DX	2	2	17	Nf/N6 Bus Lock

Nf: Number of Instruction Fetch Bus cycles.
No: Number of Operand Bus cycles (either memory or I/O). I/O cycles are indicated with a note in the comments column.
VIO instructions include only the execution of one operation.
Nc: Total number of clocks to execute the instruction with the given number of address and data wait states.
Nf/N6: An instruction Fetch cycle occurs during a 5 clock machine cycle. This allows the user to discount 1 data phase wait state.
Bus Lock: The Bus Lock signal is used during the execution of this instruction to hold the bus for use during 2 consecutive machine cycles.
Bus Lock (1): This instruction activates Bus Lock and keeps it active for 2 Bus cycles with 1 intervening ALU cycle.
Bus Lock (2): This instruction activates Bus Lock and keeps it active for a total of 4 machine cycles, including:
1 Memory Read Bus cycle
1 ALU cycle
1 Memory Read Bus cycle
1 Memory Write Bus cycle

NOTE: Calculation of some instruction execution times requires the addtition of more than one number, e.g. the time for an RPII/O command in a VIO chain requires the addition of the base time for the VIO instrruction, plus the incremental time for each VIO operation, plus the time for any unused bits preceding the RPI in the VIO Vector Select, plus the time for the RPI command.

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
Single-Precision Negate	NEG	R	1	0	5	Nf/N6
Double-Precision Negate	DNEG	R	1	0	18	
Single-Precision Multiply	MS	R	1	0	44	
16-Bit Product	MS	ISP	1	0	47	
	MS	ISN	1	0	47	
	MS	D	2	1	52	
	MS	DX	2	1	52	
	MS	IM	2	0	51	
			0	0	(30)	+ ZERO MULTIPLICAND
Single-Precision Multiply	M	R	1	0	42	
32-Bit Product	M	B	1	1	49	
	M	BX	1	1	49	
	M	D	2	1	50	
	M	DX	2	1	50	
	M	IM	2	0	49	
			0	0	5	+ ZERO MSW OFMULTIPLICAND
			0	0	(25)	+ ZERO MULTIPLICAND
Double-Precision Multiply	DM	R	1	0	130	
	DM	D	2	2	136	
	DM	DX	2	2	136	
Single-Precision Divide	DV	R	1	0	100	Nf/N6
16-Bit Dividend	DV	ISP	1	0	100	Nf/N6
	DV	ISN	1	0	100	Nf/N6
	DV	D	2	1	105	Nf/N6
	DV	DX	2	1	105	Nf/N6
	DV	IM	2	0	104	Nf/N6
			0	0	5	Add for dividend = 8000(H)
			0	0	6	Add for negative dividend
			0	0	3	Add for negative divisor
			0	0	3	Add for remainder correction
Single-Precision Divide	D	R	1	0	101	Nf/N6
32-Bit Dividend	D	B	1	1	105	Nf/N6
	D	BX	1	1	105	Nf/N6
	D	D	2	1	106	Nf/N6
	D	DX	2	1	106	Nf/N6
	D	IM	2	0	105	Nf/N6
			0	0	6	Add for RA $\geq$ divisor
Divisor						
			0	0	9	Add for negative dividend
			0	0	5	Add for negative divisor
			0	0	3	Add for remainder correction
Double-Precision Divide	DD	R	1	0	241	
	DD	D	2	2	247	
	DD	DX	2	2	247	
			0	0	6	Add for negative dividend
			0	0	6	Add for negative divisor
			0	0	7	Add for negative result
			0	0	5	Add for MSW of dividend = 8000(H)
			0	0	5	Add for dividend = 8000 0000(H)
			0	0	5	Add above + LSW of dividend = -1
Single-Precision Compare	C	R	1	0	8	Nf/N6
	C	B	1	1	15	Nf/N6
	C	BX	1	1	15	Nf/N6
	C	ISP	1	0	11	Nf/N6
	C	ISN	1	0	11	Nf/N6
	C	D	2	1	16	Nf/N6
	C	DX	2	1	16	Nf/N6

FUNCTION	INST	MODE	Nf	No	Nc		NOTES
	C	IM	2	0	15		Nf/N6
Compare Between Limits	CBL	D	2	2	30		Nf/N6 (RA<DO1)
			2	2	43		Nf/N6 (DO1≤RA≤DO2)
			2	2	40		Nf/N6 (RA>DO2)
	CBL	DX	2	2	30		Nf/N6 (RA<DO1)
			2	2	43		Nf/N6 (DO1≤RA≤DO2)
			2	2	40		Nf/N6 (RA>DO2)
Double-Precision Compare	DC	R	1	0	47		
	DC	D	2	2	27		
	DC	DX	2	2	27		
Inclusive-OR	OR	R	1	0	4		
	OR	B	1	1	11		
	OR	BX	1	1	11		
	OR	D	2	1	12		
	OR	DX	2	1	12		
	OR	IM	2	0	11		
AND	AND	R	1	0	4		
	AND	B	1	1	11		
	AND	BX	1	1	11		
	AND	D	2	1	12		
	AND	DX	2	1	12		
	AND	IM	2	0	11		
Exclusive-OR	XOR	R	1	0	4		
	XOR	D	2	1	12		
	XOR	DX	2	1	12		
	XOR	IM	2	0	11		
NAND	NAND	R	1	0	9		
	NAND	D	2	1	17		
	NAND	DX	2	1	17		
	NAND	IM	2	0	16		
FLOATING POINT							
Floating-Point Add	FA	R	1	0	91	2/	No shifts in
			1	0	70	3/	exponent adjust
	FA	B	1	2	96	2/	and in
			1	2	75	3/	normalization
	FA	BX	1	2	96	2/	
			1	2	75	3/	
	FA	D	2	2	97	2/	
			1	2	76	3/	
	FA	DX	2	2	97	2/	
			1	2	76	3/	
	FA	ALL	0	0	(15)		+RA=0
			0	0	(67)	2/	+DO=0
			0	0	(46)	3/	
			0	0	14		+ADDITION OVERFLOW
			0	0	8		+SCALE RA
			0	0	6		INCREMENTAL
			0	0	6		+ SCALE DO
			0	0	6		INCREMENTAL
			0	0	5		+ NORMALIZE
			0	0	13		INCREMENTAL
			0	0	5		UNNORMALIZED MANTISSA=0
			0	0	10		RESULT=0

FUNCTION	INST	MODE	Nf	No	Nc		NOTES
Extended-Precision	EFA	R	1	0	106	2/	
Floating-Point Add			1	0	85	3/	
	EFA	D	2	3	113	2/	
			2	3	92	3/	
	EFA	DX	2	3	113	2/	
			2	3	92	3/	
	EFA	ALL	0	0	(15)		+RA=0
			0	0	(76)	2/	+DO=0
			0	0	(55)	3/	
			0	0	17		+ADDITION OVERFLOW
			0	0	8		+SCALE RA
			0	0	9		INCREMENTAL
			0	0	6		+SCALE DO
			0	0	9		INCREMENTAL
			0	0	8		+NORMALIZE
			0	0	16		INCREMENTAL
			0	0	2		MSH OF MANTISSA=0
			0	0	7		UNNORMALIZED MANTISSA=0
			0	0	20		RESULT=0
Floating-Point	FABS	R	1	0	16		Pos.#
Absolute Value	FABS	R	1	0	71		Neg.#
Floating-Point Subtract	FS	R	1	0	91	2/	
			1	0	70	3/	
	FS	B	1	2	96	2/	
			1	2	75	3/	
	FS	BX	1	2	96	2/	
			1	2	75	3/	
	FS	D	2	2	97	2/	
			2	2	76	3/	
	FS	DX	2	2	97	2/	
			2	2	76	3/	
	FS	ALL	0	0	(15)		+RA=0
			0	0	(67)	3/	+DO=0
			0	0	(46)	3/	
			0	0	14	2/	+ ADDITION OVERFLOW
			0	0	17	3/	
			0	0	8		+SCALE RA
			0	0	6		INCREMENTAL
			0	0	6		+SCALE DO
			0	0	6		INCREMENTAL
			0	0	5		+NORMALIZE
			0	0	13		INCREMENTAL
			0	0	5		UNNORMALIZED MANTISSA=0
			0	0	10		RESULT=0
Extended-Precision	EFS	R	1	0	106	2/	
Floating-Point Subtract			1	0	85	3/	
	EFS	D	2	3	113	2/	
			2	3	92	3/	
	EFS	DX	2	3	113	2/	
			2	3	92	3/	

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
	EFS	ALL	0	0	(15)	+ RA=0
			0	0	(76)	+DO=0
			0	0	5	
			0	0	17	+ADDITION OVERFLOW
			0	0	8	+SCALE RA
			0	0	9	INCREMENTAL
			0	0	6	+SCALE DO
			0	0	9	INCREMENTAL
			0	0	8	+NORMALIZE
			0	0	16	INCREMENTAL
			0	0	2	MSH OF MANTISSA=0
			0	0	7	UNNORMALIZED MANTISSA=0
			0	0	20	RESULT=0
Floating-Point Negate	FNEG	R	1	0	61	Pos.#
			1	0	65	Neg.#
Floating-Point Multiply	FM	R	1	0	120	
	FM	B	1	2	125	
	FM	BX	1	2	125	
	FM	D	2	2	126	
	FM	DX	2	2	126	
			0	0	18	+NORMALIZE
			0	0	6	+8000 00XX* 8000 00XX
Extended-Precision	EFM	R	1	0	243	
Floating-Point Multiply	EFM	D	2	3	250	
	EFM	DX	2	3	250	
			0	0	24	+NORMALIZE
			0	0	6	+8000 00XX 0000*8000 00XX 0000
Floating-Point Divide	FD	R	1	0	120	
	FD	B	1	2	125	
	FD	BX	1	2	125	
	FD	D	2	2	126	
	FD	DX	2	2	126	
	FD	ALL	0	0	18	+NORMALIZE
			0	0	14	+MAN(RA) > MAN(DO)
			0	0	9	+ MAN(RA) = MAN(DO)
			0	0	(181)	+ DIVISOR = 0
			0	0	(195)	+DIVIDEND = 0
			0	0	6	+ CORRECTION REQUIRED
Extended-Precision	EFD	R	1	0	462	
Floating-Point Divide	EFD	D	2	3	469	
	EFD	DX	2	3	469	
			0	0	24	+NORMALIZE
			0	0	17	+MAN(RA) > MAN(DO)
			0	0	12	+ MAN(RA) = MAN(DO)
			0	0	(412)	+ DIVISOR = 0
			0	0	(435)	+DIVIDEND = 0
			0	0	3	+ CORRECTION REQUIRED
Floating-Point Divide	FC	R	1	0	52	Nf/N6; RA< DO; RA > DO, A1 <> 0
	FC	B	1	2	57	Nf/N6; RA< DO; RA > DO, A1 <> 0
	FC	BX	1	2	57	Nf/N6; RA< DO; RA > DO, A1 <> 0
	FC	D	2	2	58	Nf/N6; RA< DO; RA > DO, A1 <> 0

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
	FC	DX	2	2	58	Nf/N6; RA< DO; RA > DO, A1 <> 0
			0	0	(15)	+ RA=0
			0	0	(28)	+DO=0
			0	0	14	+ADDITION OVERFLOW
			0	0	8	+SCALE RA
			0	0	6	INCREMENTAL
			0	0	3	+SCALE DO
			0	0	6	INCREMENTAL
			0	0	10	+RA = DO; RA > DO, A1 = 0, A2 > 0
			0	0	13	+ RA > DO, A1 = 0, A2 < 0
Extended-Precision	EFC	R	1	0	55	Nf/N6; RA< DO; RA > DO, A1 <> 0
Floating-Point Compare	EFC	D	2	3	68	Nf/N6; RA< DO; RA > DO, A1 <> 0
	EFC	DX	2	3	68	Nf/N6; RA< DO; RA > DO, A1 <> 0
	EFC	ALL	0	0	(15)	+ RA = DO
			0	0	(31)	+ DO = 0
			0	0	9	+ADDITION OVERFLOW
			0	0	8	+SCALE RA
			0	0	9	INCREMENTAL
			0	0	3	+SCALE DO
			0	0	9	INCREMENTAL
			0	0	15	+ RA = DO
			0	0	8	+ RA > DO, A1 = 0, A2 > 0
			0	0	13	+ RA > DO, A1 = 0, A2 < 0
			0	0	15	+ RA > DO, A1 = 0, A2 = 0, Q1 > 0
			0	0	18	+ RA > DO, A1 = 0, A2 = 0, Q1 < 0
Floating-Point Multiply	FIX	R	1	0	28	Nf/N6, 0<EXP(RB)<15
to 16-Bit Integer			0	0	3	INCREMENTAL (14-EXP(RB) TIMES)
			1	0	10	Nf/N6, RB = 0
			1	0	25	Nf/N6, EXP(RB) = 150
			0	0	8	+ RB < 0, RB + 1 = 0
			0	0	10	+ RB < 0, RB + 1 <> 0
			1	0	13	Nf/N6, EXP(RB) < 0
			1	0	26	Nf/N6, EXP(RB) > 15
Convert 16-Bit Integer	FLT	R	1	0	16	Nf/N6
to Floating Point			1	0	8	Nf/N6, DO = 0
			0	0	5	+NORMALIZATION
			0	0	13	INCREMENTAL
Convert Extended-Precision	EFIX	R	1	0	44	0<EXP(DO)<31
Floating Point to			0	0	6	INCREMENTAL (30-EXP(DO)TIMES)
32-Bit Integer			1	0	21	RB = 0
			1	0	36	EXP(DO) = 31
			0	0	8	+ RB < 0, RB + 2 = 0
			0	0	15	+ RB < 0, RB + 2 <>0
			1	0	24	EXP(DO)<0
			1	0	39	EXP(DO)>31
Convert 32-Bit Integer	EFLT	R	1	0	31	Nf/N6, RA <>0
to Extended-Precision			0	0	8	+NORMALIZATION
Floating Point			0	0	16	+NORMALIZATION, INCREMENTAL
			0	0	2	+ RA=0, RA<>0
			1	0	22	Nf/N6, RA =0, RA+1=0
	BIT OPERATIONS					
Set Bit	SB	R	1	0	7	
	SB	D	2	2	16	Bus Lock
	SB	DX	2	2	16	Bus Lock
	SB	I	2	3	20	Bus Lock
	SB	IX	2	3	20	Bus Lock

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
Reset Bit	RB	R	2	0	7	
	RB	D	2	2	16	Bus Lock
	RB	DX	2	2	16	Bus Lock
	RB	I	2	3	20	Bus Lock
	RB	IX	2	3	20	Bus Lock
Test Bit	TB	R	2	0	7	
	TB	D	2	1	15	
	TB	DX	2	1	15	
	TB	I	2	2	19	
	TB	IX	2	2	19	
Test and Set Bit	TSB	D	2	3	23	Bus Lock(2)
	TSB	DX	2	3	23	Bus Lock(2)
Set Variable Bit in Register	SVBR	R	1	0	7	
Reset Variable Bit in Register	RVBR	R	1	0	7	
Test Variable Bit in Register	TVBR	R	1	0	7	
	SHIFT					
Shift Left Logical	SLL	R	1	0	7	One Shift
			0	0	3	Incremental
Shift Right Logical	SRL	R	1	0	7	One Shift
			0	0	3	Incremental
Shift Right Arithmetic	SRA	R	1	0	7	One Shift
			0	0	3	Incremental
Shift Left Cyclic	SLC	R	1	0	7	One Shift
			0	0	3	Incremental
Double Shift Left Logical	DSLL	R	1	0	16	One Shift
			0	0	6	Incremental
Double Shift Right Logical	DSRL	R	1	0	16	One Shift
			0	0	6	Incremental
Double Shift Right Arithmetic	DSRA	R	1	0	16	One Shift
			0	0	6	Incremental
Double Shift Left Cyclic	DSLC	R	1	0	19	One Shift
			0	0	9	Incremental
Shift Logical,	SLR	R	1	0	8	Nf/N6, no shift
Count in Register			1	0	21	Nf/N6, right
			0	0	3	Incremental
	SLR	R	1	0	38	Nf/N6, left
			0	0	5	Incremental
Shift Arithmetic,	SAR	R	1	0	8	Nf/N6, no shift
Count in Register			1	0	21	Nf/N6, right
			0	0	3	Incremental
	SAR	R	1	0	29	Nf/N6, left
			0	0	5	Incremental
Shift Cyclic,	SCR	R	1	0	8	Nf/N6, no shift
Count in Register			1	0	21	Nf/N6, right
			0	0	3	Incremental
	SCR	R	1	0	24	Nf/N6, left
			0	0	3	Incremental
Double Shift Logical,	DSLR	R	1	0	11	Nf/N6, no shift
Count in Register			1	0	30	Nf/N6, right
			0	0	6	Incremental
	DSLR	R	1	0	44	Nf/N6, left
			0	0	8	Incremental
Double Shift Arithmetic,	DSAR	R	1	0	11	Nf/N6, no shift
Count in Register			1	0	30	Nf/N6, right
			0	0	6	Incremental

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
	DSAR	R	1	0	35	Nf/N6, left
			0	0	8	Incremental
Double Shift Cyclic,	DSCR	R	1	0	11	Nf/N6, no shift
Count in Register			1	0	33	Nf/N6, right
			0	0	9	Incremental
	DSCR	R	1	0	33	Nf/N6, left
			0	0	9	Incremental
	LOAD/STORE/EXCHANGE					
Single-Precision Load	L	R	1	0	4	
	L	B	1	1	11	
	L	BX	1	1	11	
	L	ISP	1	0	7	
	L	ISN	1	0	7	
	L	D	2	1	12	
	L	DX	2	1	12	
	L	IM	2	0	11	
	L	IMX	2	0	14	
	L	I	2	2	16	
	L	IX	2	2	16	
Double-Precision Load	DL	R	1	0	16	
	DL	B	1	2	21	
	DL	BX	1	2	21	
	DL	D	2	2	22	
	DL	DX	2	2	22	
	DL	I	2	3	26	
	DL	IX	2	3	26	
Extended-Precision	EFL	D	2	3	26	
Floating-Point Load	EFL	DX	2	3	26	
Load from Upper Byte	LUB	D	2	1	15	
	LUB	DX	2	1	15	
	LUB	I	2	2	19	
	LUB	IX	2	2	19	
Load from Lower Byte	LLB	D	2	1	12	
	LLB	DX	2	1	12	
	LLB	I	2	2	16	
	LLB	IX	2	2	16	
Single-Precision Store	ST	B	1	1	11	
	ST	BX	1	1	11	
	ST	D	2	1	12	
	ST	DX	2	1	12	
	ST	I	2	2	16	
	ST	IX	2	2	16	
Store a Non-Negative Constant	STC	D	2	1	12	
	STC	DX	2	1	12	
	STC	I	2	2	16	
	STC	IX	2	2	16	
Double-Precision Store	DST	B	1	2	15	
	DST	BX	1	2	15	
	DST	D	2	2	16	
	DST	DX	2	2	16	
	DST	I	2	3	20	
	DST	IX	2	3	20	
Store Register through Mask	SRM	D	2	3	20	Bus Lock(1)
	SRM	DX	2	3	20	Bus Lock(1)
Extended-Precision	EFST	D	2	3	20	
Floating-Point Store	EFST	DX	2	3	20	
Store into Upper Byte	STUB	D	2	2	16	Bus Lock

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
	STUB	DX	2	2	16	Bus Lock
	STUB	I	2	3	20	Bus Lock
	STUB	IX	2	3	20	Bus Lock
Store into Lower Byte	STLB	D	2	2	16	Bus Lock
	STLB	DX	2	2	16	Bus Lock
	STLB	I	2	3	20	Bus Lock
	STLB	IX	2	3	20	Bus Lock
Exchange Bytes in Register	XBR	S	1	0	7	
Exchange Words in Register	XWR	R	1	0	10	
	MULTIPLE LOAD/STORE					
Push Multiple Registers	PSHM	S	1	1	16	One operation
onto the Stack			0	1	12	Incremental
Pop Multiple Registers	POPM	S	1	1	20	Nf/N6
off the Stack			0	1	16	Incremental
Load Multiple Registers	LM	D	2	1	16	
			0	1	8	Incremental
	LM	DX	2	1	16	
			0	1	8	Incremental
Store Multiple Registers	STM	D	2	1	17	
			0	1	9	Incremental
	STM	DX	2	1	17	
			0	1	9	Incremental
Move Multiple Words,	MOV	S	1	0	9	no move
Memory-to-Memory			1	2	37	one move
			0	2	13	Incremental
	PROGRAM CONTROL					
Jump on Condition	JC	D	2	0	9	Nf/N6, No Jump
	JC	D	3	0	17	Nf/N6, Jump
	JC	DX	2	0	9	Nf/N6, No Jump
	JC	DX	3	0	17	Nf/N6, Jump
	JC	I	2	1	13	Nf/N6, No Jump
	JC	I	3	1	21	Nf/N6, Jump
	JC	IX	2	1	13	Nf/N6, No Jump
	JC	IX	3	1	21	Nf/N6, Jump
Jump to Subroutine	JS	D	3	0	12	
	JS	DX	3	0	12	
Subtract One and Jump	SOJ	D	2	0	13	No Jump
	SOJ	D	3	0	17	Jump
	SOJ	DX	2	0	13	No Jump
	SOJ	DX	3	0	17	Jump
Branch Unconditionally	BR	ICR	2	0	14	
Branch if Equal to (Zero)	BEZ	ICR	1	0	4	No Branch
	BEZ	ICR	3	0	15	Branch
Branch if Less Than (Zero)	BLT	ICR	1	0	4	No Branch
	BLT	ICR	3	0	15	Branch
Branch if Less Than or	BLE	ICR	1	0	4	No Branch
Equal to (Zero)	BLE	ICR	3	0	15	Branch
Branch if Greater than (Zero)	BGT	ICR	1	0	4	No Branch
	BGT	ICR	3	0	15	Branch
Branch if Not Equal to (Zero)	BNZ	ICR	1	0	4	No Branch
	BNZ	ICR	3	0	15	Branch
Branch if Greater Than or	BGE	ICR	1	0	4	No Branch
Equal to (Zero)	BGE	ICR	3	0	15	Branch
Branch Executive	BEX	S	2	8	92	No MMU
			2	8	87	MMU

FUNCTION	INST	MODE	Nf	No	Nc	NOTES
Load Status 1/	LST	D	3	3	42	MMU Attached
			3	3	47	No MMU Attached
	LST	DX	3	3	42	MMU Attached
			3	3	47	No MMU Attached
	LST	I	3	4	46	MMU Attached
			3	4	51	No MMU Attached
	LST	IX	3	4	46	MMU Attached
			3	4	51	No MMU Attached
Stack IC and Jump	SJS	D	3	1	22	
to Subroutine	SJS	DX	3	1	22	
Unstack IC and Return from Subroutine	URS	S	3	1	15	
No-Operation	NOP	S	1	0	9	
Breakpoint	BPT	S	1	1	23	No Console (I/O)
Built-In-Function (to Utilize	BIF	D	3	2	34	(I/O)
External Co-Processors	BIF	DX	3	2	34	(I/O)
	BIF	I	3	3	38	(2 I/O)
	BIF	IX	3	3	38	(2 I/O)
	PROGRAMMED INPUT/OUTPUT					
Execute Input/Output 1/	XIO	IM	2	0	27	Overhead - PI
	XIO	IMX	2	0	30	Overhead - PI
	XIO	IM	2	0	21	Overhead - PO
	XIO	IMX	2	0	24	Overhead - PO
Vectored Input/Output 1/	VIO	D	2	2	35	Overhead
	VIO	DX	2	2	38	Overhead
	VIO		0	1	33	PI Case - Incremental
	VIO		0	1	30	PO Case - Incremental
	VIO		0	0	18	Incremental - Unused Bits
Programmed Input	PI		0	1	4	(I/O in)
Programmed Output	PO		0	1	5	(I/O out)
	TIMER CONTROL					
Timer A Start	TAS		0	1	5	(I/O out)
Timer A Halt	TAH		0	1	5	(I/O out)
Output Timer A	OTA		0	1	7	(I/O out)
Input Timer A	ITA		0	1	7	(I/O in)
Timer B Start	TBS		0	1	5	(I/O out)
Timer B Halt	TBH		0	1	5	(I/O out)
Output Timer B	OTB		0	1	7	(I/O out)
Input Timer B	ITB		0	1	7	(I/O in)
	INTERRUPTION/DMA/FAULT CONTROL					
Set Interrupt Mask	SMK		0	1	4	(I/O out)
Clear Interrupt Request	CLIR		0	1	7	(I/O out)
Enable Interrupts	ENBL		0	1	5	(I/O out)
Disable Interrupts	DSBL		0	1	5	(I/O out)
Reset Pending Interrupt	RPI		0	1	18	(I/O out)
Set Pending Interrupts	SPI		0	1	4	(I/O out)
Read Interrupt Mask	RMK		0	1	4	(I/O out)
Read Pending Interrupt Register	PIR		0	1	3	(I/O in)
Read and Clear Fault Register	RCFR		0	1	7	(I/O in)
Enable DMA	DMAE		0	1	5	(I/O out)
Disable DMA	DMAD		0	1	5	(I/O out)

FUNCTION	INST MODE	Nf	No	Nc	NOTES
	MMU CONTROL				
Write Instruction Page Register	WIPR	0	1	5	(I/O out)
Write Operand Page Register	WOPR	0	1	5	(I/O out)
Read Instruction Page Register	RIPR	0	1	4	(I/O in)
Read Operand Page Register	ROPR	0	1	4	(I/O in)
	BPU CONTROL				
Load Memory Protect RAM	LMP	0	1	5	(I/O out)
Read Memory Protect RAM	RMP	0	1	4	(I/O in)
Memory Protect Enable	MPEN	0	1	5	(I/O out)
	MISC				
Write Status Word	WSW	0	1	12	(I/O out) MMU
	WSW	0	1	17	(I/O out) no MMU
Read Status Word	RSW	0	1	4	(I/O in)
Write Instruction Page Register	RNS	0	1	5	(I/O out)
Write Operand Page Register	GO	1	1	5	(I/O out)
	Console Operations				
Disable	74	0	0	19	Repeat Till Interrupt or CONREQ
Examine Register	60	0	2	20	
Deposit Register	61	0	2	20	
Examine & Clear Fault Register	62	0	2	20	
Deposit Status Word	63	0	2	22	
Examine Memory	66	0	4	28	
Deposit Memory	67	0	3	21	
Examine Next Memory	6A	0	3	27	
Deposit Next Memory	6B	0	3	24	
Continue	75	2	1	24	
Examine XIO	6C	0	4	31	
Deposit XIO	6D	0	3	24	
Examine Next XIO	6E	0	3	27	
Deposit Next XIO	6F	0	3	27	
	Interrupt Response				
Interrupt Acknowledge		2	9	96	No MMU
		2	9	91	MMU

1/ Privileged instruction.
2/ Device type 01 only.
3/ Device types 02, 03, and 04 only.

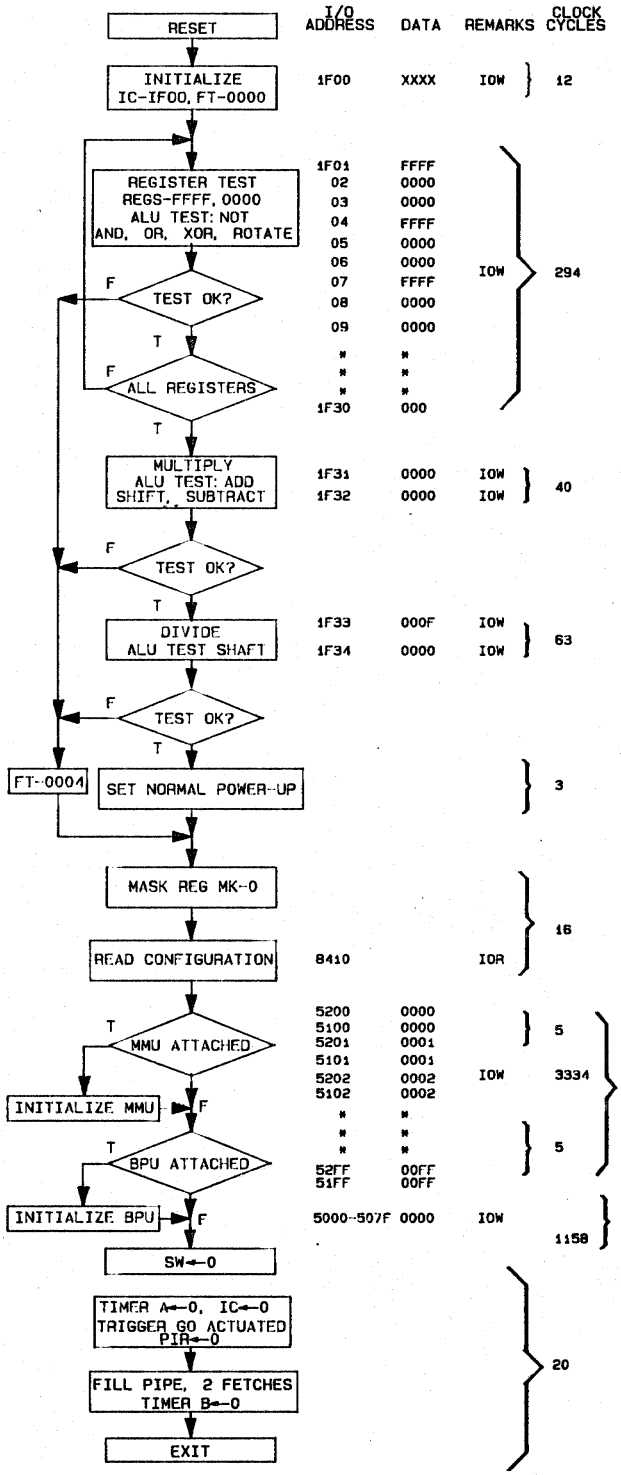
3.10.4 MIL-STD-1750 defined I/O command.

Mnemonic	Function	I/O Command Field (Hex)	
Timer Control			
TAS	Timer A Start	4008	
TAH	Timer A Halt	4009	
OTA	Output Timer A	400A	
ITA	Input Timer A	C00A	
TBS	Timer B Start	400C	
TBH	Timer B Halt	400D	
OTB	Output Timer B	400E	
ITB	Input Timer B	C00E	
Interrupt/ DMA/ Fault Control			
SMK	Set Interrupt Mask	2000	
CLIR	Clear Interrupt Request	2001	
ENBL	Enable Interrupts	2002	
DSBL	Disable Interrupts	2003	
RPI	Reset Pending Interrupt	2004	The F9450 implements these I/O commands on chip.
SPI	Set Pending Interrupt Register	2005	
RMK	Read Interrupt Mask	A000	
RPIR	Read Pending Interrupt Register	A004	
RCFR	Read and Clear Fault Register	A00F	
DMAE	DMA Enable	4006	
DMAD	DMA Disable	4007	
MISC			
WSW	Write Status Word	200E	
RSW	Read Status Word	A00E	
RNS	Reset Normal Power-Up Discrete	200A	
GO	Pulse TR I GO RST Output	400B	
MMU Control			
WIPR	Write Instruction Page Register	51XY	
WOPR	Write Operand Page Register	52XY	
RIPR	Read Instruction Page Register	D1XY	
ROPR	Read Operand Page Register	D2XY	
BPU Control			These commands are implemented within the F9452. The F9450 performs no special operation during the execution of these I/O commands. The F9450 treats these as any external I/O.
LMP	Load Memory Protect RAM	50XX	
RMP	Read Memory Protect RAM	D0XX	
MPEN	Memory Protect Enable	4003	

Mnemonic	Function	I/O Command Field (Hex)	
Miscellaneous			
PO	Programmed Output	0YXX	
PI	Programmed Input	8YXX	
OD	Output Discretes	2008	
CO	Console Output	4000	
CLC	Clear Console	4001	
ESUR	Enable Start Up ROM	4004	
DSUR	Disable Start Up ROM	4005	
RIC1	Read I/O Interrupt Code, Level 1	A001	The F9450 is totally transparent to these codes. No special operation results in the F9450 from execution of these I/O commands. The F9450 treats these operations as any external I/O. Please refer to XIO and VIO instructions for execution time.
RIC2	Read I/O Interrupt Code, Level 2	A002	
RDOR	Read Discrete Output Register	A008	
RDI	Read Discrete Input	A009	
TPIO	Test Programmed Output	A00B	
RMFS	Read Memory Fault Status	A00D	
CI	Console Input	C000	
RCS	Read Console Status	C001	

3.10.5 F9450 dedicated I/O addresses.

I/O Address/Command	Input/Output	Function
8400	Input	Read console command
8401	Input	Read console data
0400	Output	Write result into console
8410	Input	Read system configuration (see the "System Configuration Register (SCR)" section).
0800, 0900, 0A01, 0B01	Output	Write derived address to coprocessor no. 1, 2, 3, or 4, respectively (used to implement the Built-In Function).
0801, 0901, 0A01, 0B01	Output	Write op-code into coprocessor no. 1, 2, 3, or 4, respectively.
1000	Output	Indicate and interrupt acknowledge cycle. Used by external devices to reset their level-generated interrupts.
1F00 - 1F34	Output	If these I/O addresses are used within the system, they should be protected during F9450 self-test.



NOTE: The purpose of the I/O Write (IOW) addresses is to inform the user of the presently executed instruction in the self-test program. The user must furnish bus control signals to the CPU to enable it to continue the self-test sequence.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). In addition, a device shall be submitted once every 12 months of production to WPAFB (SEAFAC) for verification to MIL-STD-1750 VSW test V 2.1 + 2 (see 3.7). For device types 02, 03, and 04, MIL-STD-1750 VSW test V 2.1 + 12 is applicable. The result of such testing shall be reported to DESC-ECS.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Subgroup 12 shall be added and shall consist of the MIL-STD-1750 VSW test at V 2.1 + 2 deterministic portion only, at room ambient (see 3.7). For device types 02, 03, and 04, MIL-STD-1750 VSW test V 2.1 + 12 is applicable.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 functional testing shall include verification of instruction set.

d. Subgroup 13 shall be added and shall consist of the MIL-STD-1750 VSW test at V 2.1 + 2 deterministic portion only, at -55°C instant on and +125°C T_C (see 3.7). For device types 02, 03, and 04, MIL-STD-1750 VSW test V 2.1 + 12 is applicable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein. Devices which have passed subgroups 1, 2, and 3 in table I and the device functional built-in test and operate at greater than or equal to 12MHz may be used for destructive quality conformance inspection testing (QCI) provided subject parts are identified as NONSHIPPABLE parts and the noncompliant electricals from subgroups 9, 10, and 11 are identified through the remainder of testing. Group D inspection electrical test end points shall be subgroups 1, 2, and 3 and the device built-in test. (The devices defined herein shall be for group D end points only.)

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. Subgroup 13 shall be added and will be as defined in 4.3.1d.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10**, 11**, 12
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**, 13
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	7,8,9,10**, 11**,13

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbred device specified in this drawing will be replaced by the microcircuit identified as part number M38510/550XXXXX.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Definitions.

Mnemonic	Pin no.	Name	Description
Clocks			
CPU CLK	51	CPU clock	Single-phase input clock signal (15 Mhz, 40 percent to 60 percent duty cycle).
TIMER CLK	7	Timer clock	A 100 kHz input that, after synchronization with CPU, CLK, provides the clock for Timer A and Timer B. If timers are used, the CPU CLK signal frequency must be > 500kHz (40 percent to 60 percent duty cycle).
External Requests			
RESET	5	Reset	An active-low input that initializes the device. The processor must be RESET after input power ($V_{CC,}$ I_{INJ}) is within specification and stable to insure proper operation.
CONREQ	2	Console request	An active-low input that initiates console operations after the current instruction.
Interrupts			
PWRDN INT	33	Power down interrupt	An input interrupt request than cannot be masked or disabled. This signal is active on the positive-going edge or the high level, according to the interrupt mode bit in the configuration register. This input has hysteresis circuitry for noise immunity.
USR_0 INT- USR_5 INT	34-39	User interrupt	Input signals that are active on the positive-going edge or high level, according to the interrupt mode bit in the configuration register. These inputs have hysteresis circuitry for noise immunity.
IOL1 INT IOL2 INT	40,41	I/O level interrupts	Active-high inputs that can be used to expand number of user interrupts.
Faults			
MEM PRT ER	26	Memory protect error	An active-low input generated by the MMU or BPU, or both, and sampled by the BUS BUSY signal into the fault register (bit 0 if CPU bus cycle, bit 1 if non-CPU bus cycle).
PAR ER	27	Parity error	An active-low input sampled by the BUS BUSY signal into bit 2 of the fault register.
EXT ADR ER	28	External address error	An active-low input sampled by the BUS BUSY signal into the fault register (bit 5 or 8), depending on the cycle (memory or I/O).

Mnemonic	Pin no.	Name	Description
$SYSFLT_0$ $SYSFLT_1$	29,30	System fault 0 System fault 1	Asynchronous, positive-edge-sensitive inputs to the device that set bit 7 ($SYSFLT_0$) or bits 13 and 15 ($SYSFLT_1$) in the fault register. These inputs are protected from system noise through hysteresis circuitry.
Information bus			
IB_0-IB_{15}	9-18 20-25	Information bus	An active-high bidirectional time-multiplexed address/data bus that is 3-state during bus cycles not assigned to this CPU; IB_0 is the most significant bit.
Status bus			
AK_0-AK_3	47-50	Access key	Active-high outputs used to match the access lock in the MMU for memory accesses (a mismatch is one of several possible situations that cause the MMU to pull the MEM PRT ER signal low. These signals are 3-state during bus cycles not assigned to this CPU.
AS_0-AS_3	42-45	Address state	Active-high outputs that select the page register group in the MMU; 3-state bus during bus cycles not assigned to this CPU. These outputs together with D/I can be used to expand the device's direct addressing range to 2M words.
Error control			
UNRCV ER	8	Unrecoverable error	An active-high output that indicates the occurrence of an error classified as unrecoverable.
MAJ ER	31	Major error	An active-high output indicating the occurrence of an error classified as major.
Discrete control			
DMA EN	3	Direct memory access enable	An active-high output that indicates the DMA is enabled. It is disabled when the CPU is initalized (reset) and is enabled under program control.
NML PWRUP	6	Normal power up	An active-high output that is set when the CPU has successfully completed the built-in test in the initallization sequence.
SNEW	63	Start new	An active-high output that indicates a new instruction will start executing in the next cycle; useful for instruction tracing function. Signal valid at frequencies up to 1/2 F_{max}.

Mnemonic	Pin no.	Name	Description
Discrete control - continued			
TR I GO RST	4	Trigger go reset initialization.	An active-low discrete output. This signal can be pulsed low under program control I/O address 400B (He_x) and is automatically pulsed once during processor
Bus control			
D/T	58	Data or instruction	An output signal that indicates whether the current bus cycle access is for data (high) or instruction (low); 3-state during bus cycles not assigned to this CPU. This line can be used as an additional memory address bit for systems that require separate data and program memory.
R/W	57	Read or write	An output signal that indicates direction of data flow with respect to the current bus master: a high indicates a read or input operation and a low indicates a write or output operation. The signal is 3-state during bus cycles not assigned to this CPU.
M/ I O	59	Memory or I/O	Output signal that indicates whether the current bus cycle is memory (high) or I/O (low). This signal is 3-state during bus cycles not assigned to this CPU.
STRBA	52	Address strobe	An active-high output that can be used to externally latch the memory or I/O address at the high-to-low transition of the strobe. The signal is 3-state during bus cycles not assigned to this CPU.
RDYA	55	Address ready	An active-high input that can be used to extend the address phase of a bus cycle. When RDYA is not active, wait states are inserted by the device's timing unit to accomadate slower memory or I/0 devices.
STRBD	53	Data strobe	An active-low output that can be used to strobe data in memory and XIO cycles. The signal is 3-state during bus cycles not assigned to this CPU.
RDYD	56	Data ready	An active-high input that extends the data phase of a bus cycle. When RDYD is not active, wait states are inserted by the device's timing unit to accomadate slower memory or I/O devices.
Bus arbitration			
BUS REQ	54	Bus request	An active-low output that indicates the CPU requires the bus; becomes inactive when the CPU has acquired the bus and started the bus cycle.

Mnemonic	Pin no.	Name	Description
Bus arbitration - continued.			
BUS GNT	61	Bus grant	An active-low input from an external arbiter that indicates the CPU currently has the highest priority bus request. If the bus is not locked, the CPU may begin a bus cycle commencing with the next CPU clock.
BUS BUSY	60	Bus busy	An active-low bidirectional signal used to establish the beginning and end of a bus cycle. The trailing edge (low-to-high transition) is used for sampling bits into the fault register. It is 3-state in bus cycles not assigned to this CPU; however, the CPU monitors the BUS BUSY line for latching non-CPU bus-cycle faults into the fault register.
BUS LOCK	62	Bus-lock	An active-low bidirectional signal used to lock the bus for successive bus cycles. During non-locked bus cycles, the BUS LOCK signal mimics the BUS BUSY signal. It is 3-state during bus cycles not assigned to this CPU. The following instructions will lock the bus: INCM, DECM, SB, RB, TSB, SRM, STUB, STLB.
Power			
V_{CC}	64	Power supply	+5 V, 270 mA typical power supply.
GND	1, 32	Ground	0 V reference. These pins should be tied together as close to the chip as possible.
$IINJ_1$, $IINJ_2$	19 46	Injector current	Current source to provide bias for the injection logic. These pins should be tied together as close to the chip as possible.

Timing characteristics.

The abbreviated symbol convention used for timing parameters in this drawing is tAb(C)d, where:

Timing symbols all begin with the letter "t".

The mnemonic in the position represented by "A" indicates the signal node beginning the interval.

The mnemonic in the position represented by "b" defines the direction of signal transition at the beginning node, if such definition is necessary; the new state of the signal may be low (1), high (h), 3-state (z), don't care (x), or valid (v).

The mnemonic in the position represented by "(C)", which always appears in the parentheses, indicates the signal node ending the interval.

The mnemonic in the position represented by "d" is the same as "b", but refers to the state of the signal at the node indicated by mnemonic in position "(C)".

The mnemonics in the positions represented by "b" and "d" are not used for reference to the CPU CLK signal, as it is assumed to be active on the rising edge.

For example, $t_{F(BB)}$ is setup time from a valid fault (EXT ADR ER, MEM PRT ER, PAR ER) input to BUS BUSY.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8414901XX	27014	F9450-15DMQB	M38510/550XXBXX
8414901YX	27014	F9450-15GMQB	M38510/550XXBXX
8414902XX	27014	F9450-18DMQB	M38510/550XXBXX
8414902YX	27014	F9450-18GMQB	M38510/550XXBXX
8414903XX	27014	F9450-20DMQB	M38510/550XXBXX
8414903YX	27014	F9450-20GMQB	M38510/550XXBXX
8414904XX	27014	F9450-15DMQB	M38510/550XXBXX
8414904YX	27014	F9450-15GMQB	M38510/550XXBXX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, CA 95052-8090