

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change $t_{PHZ}$ maximum limits to 29/41 ns and $t_{PLZ}$ maximum limits to 18/26 ns. Convert to military drawing format. Delete minimum limits from $I_{IL}$ . Make corrections to table I $V_{OH1}$ .	87-01-28	N. A. Hauck
B	Change $I_{OL}$ maximum limit to 12 mA. Change $t_{PHZ}$ and $t_{PLZ}$ maximum limits to 33/46/22/30 ns. Add note to table I. Omit inversion circles from Fig. 1. Change code itent no. to 67268. Editorial changes.	87-10-15	R. R. Evans
C	Changes in accordance with NOR 5962-R124-92. - tvn.	92-02-05	Monica L. Poelking
D	Update to reflect latest changes in format and requirements. Editorial changes throughout. - les	02-08-20	Raymond Monnin
E	Change 3.5 marking paragraph to remove "5962-". Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-08-17	Thomas M. Hess
F	Update drawing to current MIL-PRF-38535 requirements. - jt	17-08-18	Charles Saffle

**CURRENT CAGE CODE 67268**

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.



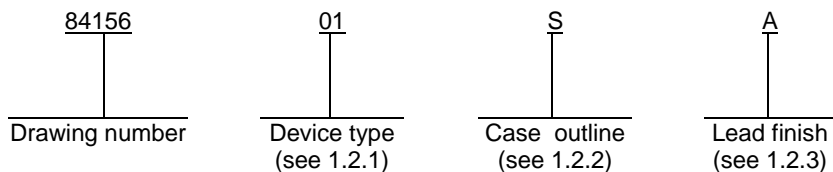
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PMIC N/A	PREPARED BY Joseph A. Kerby	<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY D. A. DiGenzo																		
	APPROVED BY N. A. Hauck	<p align="center">MICROCIRCUIT, DIGITAL, LOW-POWER SCHOTTKY, TTL, BUFFER, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 85-07-01																		
	REVISION LEVEL F	SIZE A	CAGE CODE <b>14933</b>	<b>84156</b>															
		SHEET		1 OF 10															

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54LS541	Inverting octal buffer gate (inverting control inputs) with three-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
S	GDFF2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage .....	-0.5 V dc +7.0 V dc
Input voltage range .....	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range .....	-65°C to +150°C
Maximum power dissipation ( $P_D$ ) <sup>1/</sup> .....	302 mW
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Junction temperature ( $T_J$ ) .....	+175°C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) .....	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V dc
Maximum low level input voltage ( $V_{IL}$ ):	
At -55°C and +25°C .....	0.7 V dc
At +125°C .....	0.6 V dc
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C

<sup>1/</sup> Maximum power dissipation is defined as  $V_{CC} \times I_{CC}$ , and must withstand the added  $P_D$  due to short-circuit test; e.g.,  $I_{OS}$ .

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

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3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
High level output voltage	V <sub>OH1</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IH</sub> = 2.0 v, I <sub>OH</sub> = -3 mA, V <sub>IL</sub> = 0.7 V at +25°C and -55°C V <sub>IL</sub> = 0.6 V at +125°C	1, 2, 3	All	2.4		V	
	V <sub>OH2</sub>	V <sub>CC</sub> = 4.5 V, V <sub>IH</sub> = 2.0 v, V <sub>IL</sub> = 0.5 V, I <sub>OH</sub> = -12 mA	1, 2, 3	All	2.0		V	
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA, V <sub>IH</sub> = 2.0 v, V <sub>IL</sub> = 0.7 V at +25°C and -55°C V <sub>IL</sub> = 0.6 V at +125°C	1, 2, 3	All		0.4	V	
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA T <sub>C</sub> = +25°C	1	All		-1.5	V	
High level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V,	1, 2, 3	All		20	μA	
	I <sub>IH2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 7.0 V,				100		
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V	1, 2, 3	All		-200	μA	
Short circuit output current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V, <u>1</u> / V <sub>OUT</sub> = 0.0 V	1, 2, 3	All	-40	-225	mA	
Supply current,	I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V	1, 2, 3	All		32	mA	
	I <sub>CCL</sub>							Outputs high
	I <sub>CCZ</sub>							Outputs low
			1, 2, 3	All		55		
			1, 2, 3	All				
High level output current'	I <sub>OH</sub>		1, 2, 3	All		-12	mA	
Low level output current	I <sub>OL</sub>		1, 2, 3	All		12	mA	
Hysteresis <u>2</u> /	V <sub>T+</sub> , V <sub>T-</sub>	V <sub>CC</sub> = 4.5 V	1, 2, 3	All	0.2		V	
Off-state (high-impedance) output current	I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.0 v, V <sub>OH</sub> = 2.7 V, V <sub>IL</sub> = 0.7 V at +25°C and -55°C V <sub>IL</sub> = 0.6 V at +125°C	1, 2, 3	All		20	μA	
	I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.0 v, V <sub>OL</sub> = 0.4 V, V <sub>IL</sub> = 0.7 V at +25°C and -55°C V <sub>IL</sub> = 0.6 V at +125°C	1, 2, 3	All		-20		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time data to output	t <sub>PLH</sub>	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF ±10%, R <sub>L</sub> = 110Ω ±5% <u>3/</u>	9	All		15	ns
			10, 11	All		21	
	t <sub>PHL</sub>		9	All		18	ns
			10, 11	All		26	
Output enable time to high level	t <sub>PZH</sub>		9	All		32	ns
			10, 11	All		45	
Output enable time to low level	t <sub>PZL</sub>		9	All		38	ns
			10, 11	All		54	
Output disable time from high level	t <sub>PHZ</sub>		9	All		33	ns
			10, 11	All		46	
Output disable time from low level	t <sub>PLZ</sub>		9	All		22	ns
			10, 11	All		30	

- 1/ Not more than one output should be shorted at a time, and duration of the short circuit condition should not exceed one second.
- 2/ Guaranteed but not tested.
- 3/ Frequency testing may be performed using either C<sub>L</sub> = 5 pF, C<sub>L</sub> = 45 pF or C<sub>L</sub> = 50pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50 pF load.

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Device type	01
Case outlines	S, 2
Terminal number	Terminal symbol
1	$\overline{1G}$
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	A8
10	GND
11	Y8
12	Y7
13	Y6
14	Y5
15	Y4
16	Y3
17	Y2
18	Y1
19	$\overline{2G}$
20	V <sub>CC</sub>

FIGURE 1. Terminal connections.

INPUTS			OUTPUTS
$\overline{1G}$	$\overline{2G}$	A	Y
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = High voltage level  
L = Low voltage level  
X = Irrelevant  
Z = High impedance

FIGURE 2. Truth table.

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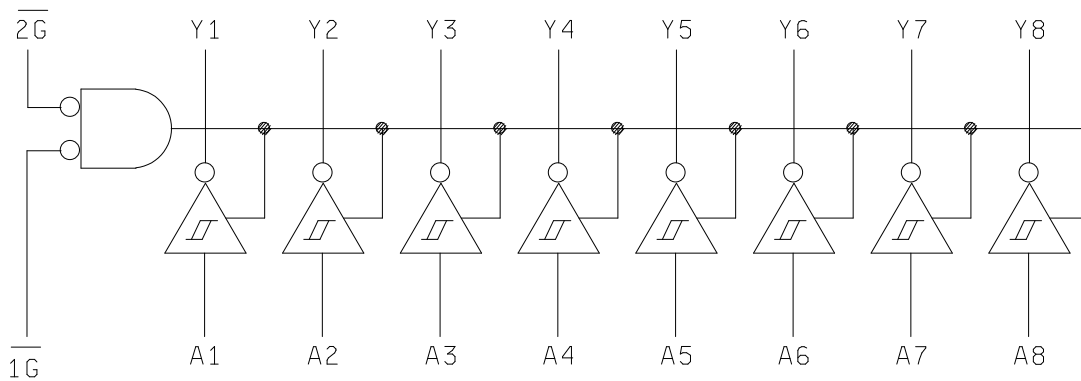


FIGURE 3. Logic diagram.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T<sub>A</sub> = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10**, 11**
Group C end-point electrical parameters (method 5005)	1, 2, 3
Group D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1.

\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-08-18

Approved sources of supply for SMD 84156 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification part number <u>1/</u>
8415601SA	01295 58625	SNJ54LS541W SL54LS541/BSA	M38510/32405BSA
84156012A	01295 58625	SNJ54LS541FK SL54LS541/B2A	M38510/32405B2A
84156012C	58625	SL54LS541/B2C	M38510/32405B2C

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

Vendor name  
and address

01295

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

58625

Lansdale Semiconductor Inc.  
5245 S. 39th St.  
Phoenix, AZ 85040-9008

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