REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Add vendor CAGE F8859. Add device class V criteria. Correct data limits in paragraph 1.3. Add case outline X. Update boilerplate. Add table III, delta limits. Editorial changes throughout. - jak	00-06-21	Monica L. Poelking
E	Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - jak	09-03-25	Thomas M. Hess
F	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	15-04-27	Muhammad A. Akbar
G	Remove class M requirements throughout. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. – TTM	21-06-22	Muhammad A. Akbar

Current CAGE Code is 67268

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Donald R. Osborne

CHECKED BY
Robert P. Evans

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
84-10-01

REVISION LEVEL
G

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, HEX INVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**84098**

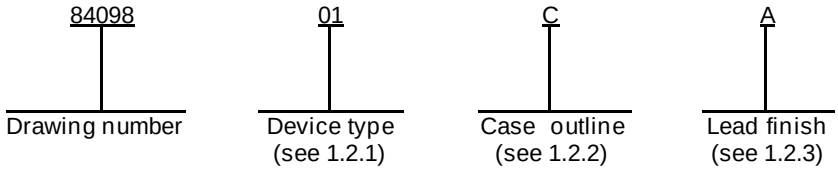
SHEET 1 OF 12

1. SCOPE

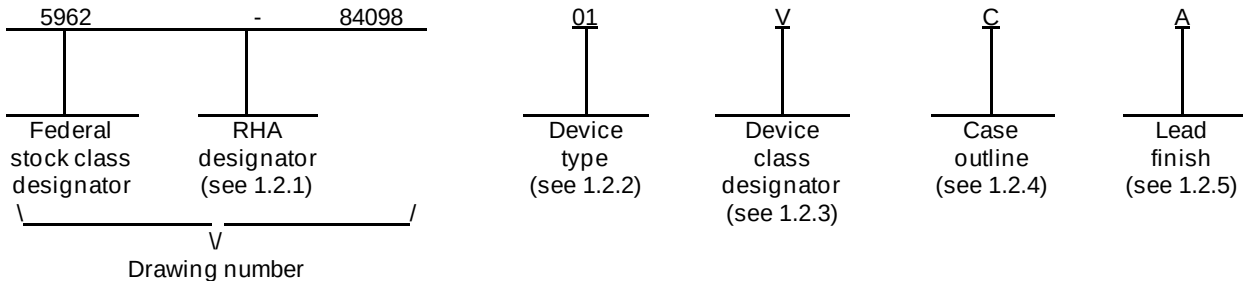
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device class Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC04	Hex inverter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
B	GDFP4-F14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
X	CDFP3-F14	14	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} +0.5 V dc
Input clamp current (I_{IK}) (V_{IN} < 0.0 V to V_{IN} > V_{CC})	±20 mA
Output clamp current (I_{OK}) (V_{OUT} < 0.0 V to V_{OUT} > V_{CC})	±20 mA
Continuous output current (I_{OUT}) (V_{OUT} = 0.0 V to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW 4/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time (t_r , t_f):	
V_{CC} = 2.0 V	0 to 1000 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 5.0 V ±0.5 V	0 to 400 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device, Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.

5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD7 - Standard for Description of 54/74HCXXXXX and 54/74HCTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at https://www.jedec.org/.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -20$ µA	2.0 V	1, 2, 3	1.9		V
			4.5 V		4.4		
			6.0 V		5.9		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -4.0$ mA	4.5 V	1	3.98		
				2, 3	3.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -5.2$ mA	6.0 V	1	5.48		
				2, 3	5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = +20$ µA	2.0 V	1, 2, 3		0.1	V
			4.5 V			0.1	
			6.0 V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = +4.0$ mA	4.5 V	1		0.26	
				2, 3		0.40	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = +5.2$ mA	6.0 V	1		0.26	
				2, 3		0.40	
High level input voltage	V_{IH} 2/		2.0 V	1, 2, 3	1.5		V
			4.5 V	1, 2, 3	3.15		
			6.0 V	1, 2, 3	4.2		
Low level input voltage	V_{IL} 2/		2.0 V	1, 2, 3		0.3	V
			4.5 V	1, 2, 3		0.9	
			6.0 V	1, 2, 3		1.2	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0.0$ A	6.0 V	1		2.0	µA
				2, 3		40.0	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0 V	1		±0.10	µA
				2, 3		±1.0	
Input capacitance	C_{IN}	$T_C = +25°C$ $V_{IN} = 0.0$ V, See 4.4.1c	2.0 V to 6.0 V	4		10.0	pF
Power dissipation capacitance	C_{PD}	$V_{IN} = 0.0$ V $T_C = +25°C$, See 4.4.1c	6.0 V	4		20.0	pF
Functional tests		See 4.4.1b		7, 8	L	H	
Propagation delay time, mA to mY	t_{PLH}, t_{PHL} 3/	$T_C = 25°C$ $C_L = 50$ pF minimum See figure 4	2.0 V	9		95.0	ns
			4.5 V	9		19.0	ns
			6.0 V	9		16.0	ns
		$T_C = -55°C$ and $+125°C$ $C_L = 50$ pF minimum See figure 4	2.0 V	10, 11		145.0	ns
			4.5 V	10, 11		29.0	ns
			6.0 V	10, 11		25.0	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
Transition time, high to low, low to high	t_{TLH}, t_{THL} 4/	T_C = 25°C C_L = 50 pF minimum See figure 4	2.0 V	9		75.0	ns
			4.5 V	9		15.0	ns
			6.0 V	9		13.0	ns
		T_C = -55°C and +125°C C_L = 50 pF minimum See figure 4	2.0 V	10, 11		110.0	ns
			4.5 V	10, 11		22.0	ns
			6.0 V	10, 11		19.0	ns

1/ For a power supply of 5.0 V ±10%, the worst case output voltages (V_{OH} and V_{OL}) occur for high-speed CMOS at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case leakage currents (I_{IN} and I_{CC}) occur for CMOS at the higher voltage, so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 20 pF per latch, determines the no load dynamic power consumption, $P_D = C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption.

2/ Tests shall be guaranteed if applied as a forcing function for V_{OH} and V_{OL}.

3/ For propagation delay times V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed to the specified limits in table I.

4/ Transition time (t_{TLH}, t_{THL}), if not tested, shall be guaranteed to the specified limits in table I.

Device type	01	
Case outlines	B, C, D and X	2
Terminal number	Terminal symbol	Terminal symbol
1	1A	NC
2	1Y	1A
3	2A	1Y
4	2Y	2A
5	3A	NC
6	3Y	2Y
7	GND	NC
8	4Y	3A
9	4A	3Y
10	5Y	GND
11	5A	NC
12	6Y	4Y
13	6A	4A
14	V_{CC}	5Y
15		NC
16		5A
17		NC
18		6Y
19		6A
20		V_{CC}

NC = No internal connection

FIGURE 1. Terminal connections.

(Each inverter)

Input	Output
A	Y
H	L
L	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

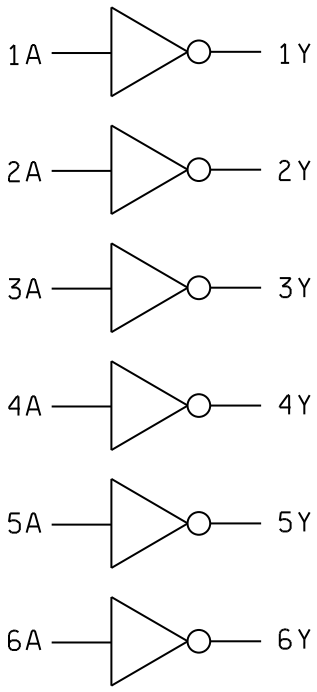
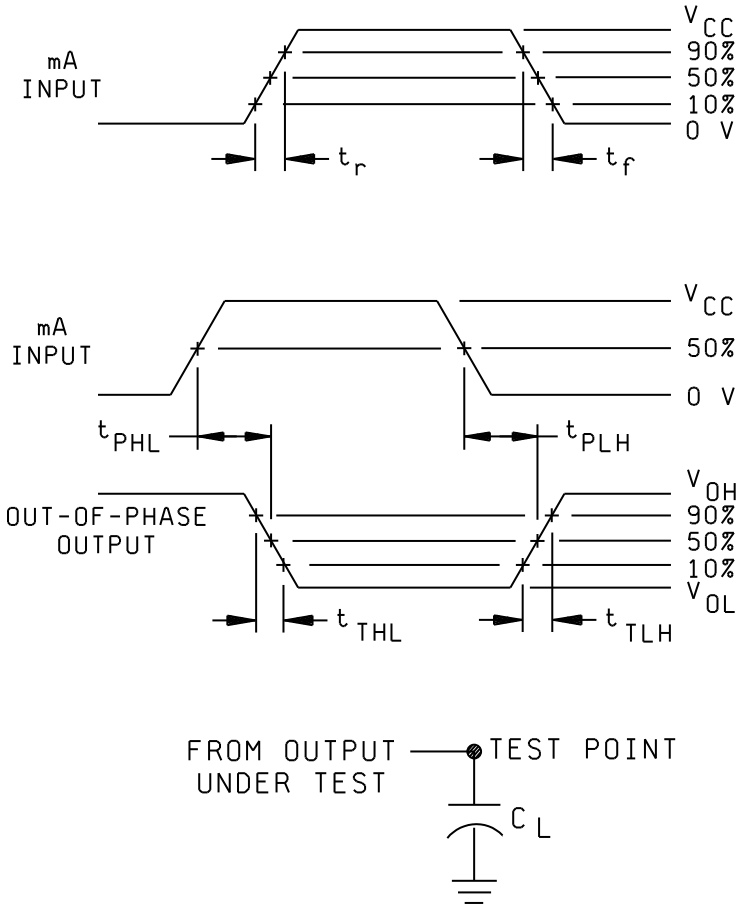


FIGURE 3. Logic diagram.



NOTES:

1. C_L = 50 pF minimum (includes test jig and probe capacitance).
2. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50Ω, t_r = 6.0 ns, t_f = 6.0 ns.
3. The outputs are measured one at a time with one input transition per measurement.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7,	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	3/1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table III shall be required where specified and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test delta parameters (+25°C).

Parameter	Symbol	Delta limits
Quiescent current	I_{CC}	±30 nA
Input current low level	I_{IL}	±20 nA
Input current high level	I_{IH}	±20 nA
Output voltage low level (I_{OL} = +4 mA, V_{CC} = 4.5 V)	V_{OL}	±0.026 V
Output voltage high level (I_{OH} = -4 mA, V_{CC} = 4.5 V)	V_{OH}	±0.20 V

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering micro electronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-06-22

Approved sources of supply for SMD 5962-84098 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8409801VCA	01295	SNV54HC04J
5962-8409801VDA	01295	SNV54HC04W
5962-8409801VXA	3/	54HC04
5962-8409801VXC	3/	54HC04
84098012A	01295	SNJ54HC04FK
8409801BA	3/	54HC04
8409801CA	01295	SNJ54HC04J
8409801DA	01295	SNJ54HC04W
8409801XA	3/	54HC04
8409801XC	3/	54HC04

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243