REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add LCC package (outline letter Z).	85 OCT 17	M.A. Frye
B	Convert to standardized military drawing format. Add source of supply, CAGE code 60991. Upgrade operating temperature range, alter electrical test requirements. Add switching test waveforms. Editorial changes throughout.	89 JUN 09	M.A. Frye

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	B																							
SHEET	22																							
REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A	PREPARED BY Todd D Cole	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARDIZED MILITARY DRAWING	CHECKED BY Ray Monnin	MICROCIRCUITS, DIGITAL, N-CHANNEL, SIGNAL PROCESSOR, MONOLITHIC SILICON
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY M.A. Frye	SIZE A / CAGE CODE 14933 / 84053
	DRAWING APPROVAL DATE 6 SEPTEMBER 1984	
AMSC N/A	REVISION LEVEL B	SHEET 1 OF 22

DESC FORM 193-1
SEP 87

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5962-E1067

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

84053	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	32010	Digital signal processor

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
Z	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (V_{CC}) 1/	-0.3 V dc to 7 V dc
Input voltage	-0.3 V dc to 15 V dc
Output voltage	-0.3 V dc to 15 V dc
Maximum power dissipation	1.5 W
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	175°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Q and Z	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Supply voltage (V_{SS})	0.0 V dc
High level input voltage (V_{IH})	
All inputs except CLKIN	2 V dc minimum
CLKIN	2.8 V dc minimum
Low level input voltage (V_{IL})	
X2/CLKIN and data	0.8 V dc maximum
$\overline{BIO}$, $\overline{INT}$, MC/$\overline{MP}$, $\overline{RS}$	0.7 V dc maximum
High level output current (I_{OH}), (all outputs)	-300 μA maximum
Low level output current (I_{OL}), (all outputs)	2 mA maximum
Case operating temperature range (T_C)	-55°C to +110°C

1/ All voltage values are with respect to V_{SS}.

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Master clock cycle time, $t_c(MC)$ - - - - - - - - - - - - - - -	50 ns minimum to 150 ns maximum
Rise time master clock input, $t_r(MC)$ - - - - - - - - - - - - -	10 ns maximum
Fall time master clock input, $t_f(MC)$ - - - - - - - - - - - - -	10 ns maximum
Pulse duration master clock low, $t_w(MC)$, ($t_c(MC)$ = 50 ns)	20 ns minimum
Pulse duration master clock high, $t_w(MC)$, ($t_c(MC)$ = 50 ns)	20 ns minimum
Hold time $\overline{BIO}$ ↑↓ after CLKOUT↓$t_{h(IO)}$ - - - - - - - - - - - - -	50 ns minimum
Hold time $\overline{INT}$ ↑↓ after CLKOUT↓$t_{h(INT)}$ - - - - - - - - - - - - -	50 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +110°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = max	All outputs except data	1,2,3	2.4		V dc
		I_{OH} = max	Data		2.2		V dc
Low level output voltage	V_{OL}	I_{OL} = max		1,2,3		0.5	V dc
Off-stage output current	I_{OZ}	V_{CC} = max V_{CC} = max	V_O = 2.4 V V_O = 0.4 V	1,2,3		20 -20	µA
Input current	I_I	$V_I = V_{SS}$ to V_{CC}		1,2,3		±50	µA
Supply current	I_{CC}	V_{CC} = max		1,2		275	mA
				3		300	
Input capacitance	C_I	F = 1 MHz, See 4.3.1c T_C = +25°C		4		25	pF
Output capacitance	C_O			4		20	pF
Bidirectional capacitance	$C_{I/O}$			4		35	pF
Clock capacitance 1/	C_1, C_2			4		20	pF
Crystal frequency 1/ 2/	F_X			7,8	6.7	20 3/	MHz
Functional tests		See 4.3.1d		7,8			
CLKOUT cycle time	$t_{c(C)}$	R_L = 870Ω ±10% C_L = 100 pF See figure 3		9,10,11	200		ns
Delay time CLKOUT ↓ to address bus valid 3/ 4/	t_{d1}			9,10,11	10	60	ns
Delay time CLKOUT ↓ to $\overline{MEN}$ ↓ 3/	t_{d2}			9,10,11	$1/4T_{C(C)}-10$	$1/4T_{C(C)}+15$	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C < T_C < +110^{\circ}C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Delay time CLKOUT ↓ to $\overline{MEN}$ ↑ 3/	t_{d3}	$R_L = 870\Omega \pm 10\%$ $C_L = 100$ pF See figure 3	9,10,11	-15	15	ns
Delay time CLKOUT ↓ to $\overline{DEN}$ ↓ 3/	t_{d4}		9,10,11	$1/4T_C$ (C)-10	$1/4T_C$ (C)+15	ns
Delay time CLKOUT ↓ to $\overline{DEN}$ ↑ 3/	t_{d5}		9,10,11	-15	15	ns
Delay time CLKOUT ↓ to $\overline{WE}$ ↓ 3/	t_{d6}		9,10,11	$1/2T_C$ (C)-10	$1/2T_C$ (C)+15	ns
Delay time CLKOUT ↓ to $\overline{WE}$ ↑ 3/	t_{d7}		9,10,11	-10	15	ns
Delay time CLKOUT ↓ to data bus out valid	t_{d8}		9,10,11		$1/4T_C$ (C)+65	ns
Time after CLKOUT ↓ that data bus starts to be driven 3/	t_{d9}		9,10,11	$1/4T_C$ (C)-10		ns
Time after CLKOUT ↓ that data bus stops being driven 3/	t_{d10}		9,10,11		$1/4T_C$ (C)+35	ns
Data bus out valid after CLKOUT ↓	t_v		9,10,11	$1/4T_C$ (C)-10		ns
Setup time data bus valid prior to CLKOUT ↓ 5/	$t_{su(D)}$		9,10,11	50		ns
Hold time data bus held valid after CLKOUT ↓ 5/	$t_{H(D)}$		9,10,11	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +110^{\circ}C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Delay time CLKIN to CLKOUT 3/	$t_{d(MCC)}$	$R_L = 870\Omega \pm 10\%$ $C_L = 100$ pF See figure 3	9,10,11	10	60	ns
$\overline{RS}$ pulse duration	$t_{w(R)}$		9,10,11	$5T_C$ (C)		ns
Reset ($\overline{RS}$) setup time prior to CLKOUT	$t_{su(R)}$		9,10,11	50		ns
Delay time $\overline{DEN}$ ↑, $\overline{WE}$ ↑, and $\overline{MEN}$ ↑ from $\overline{RS}$	t_{d11}		9,10,11		$1/2T_C$ (C)+125	ns
Data bus disable time after $\overline{RS}$ 6/	$t_{DIS(R)}$		9,10,11		$1/4T_C$ (C)+50	ns
Fall time $\overline{INT}$	$t_{f(INT)}$		9,10,11		15	ns
Pulse duration $\overline{INT}$	$t_{w(INT)}$		9,10,11	T_C(C)		ns
Setup time $\overline{INT}$ ↓ before CLKOUT ↓	$t_{su(INT)}$		9,10,11	50		ns
Fall time $\overline{BIO}$ 7/	$t_{f(IO)}$		9,10,11		15	ns
Pulse duration $\overline{BIO}$ 7/	$t_{w(IO)}$		9,10,11	T_C(C)		ns
Setup time $\overline{BIO}$ ↓ before CLKOUT ↓ 7/	$t_{su(IO)}$		9,10,11	50		ns

See footnotes on next page.

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1/ The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT is one-fourth the crystal fundamental frequency.
2/ An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed under the recommended operating conditions.
3/ This limit is guaranteed to the limit specified herein, if not tested.
4/ Address bus will be valid upon $\overline{WE}$ ↑, $\overline{DEN}$ ↑, or $\overline{MEN}$ ↑.
Address bus will be valid upon $\overline{MEN}$ ↓, $\overline{DEN}$ ↓.
5/ Data may be removed from the data bus upon $\overline{MEN}$ ↑ or $\overline{DEN}$ ↑ preceding CLKOUT ↓.
6/ $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.
7/ $\overline{BIO}$ is an asynchronous input. It can occur anytime within a clock cycle but should be maintained for a minimum of one clock cycle to ensure synchronization and correct execution (see figure 3).

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Initial and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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Case Q
Device type 01

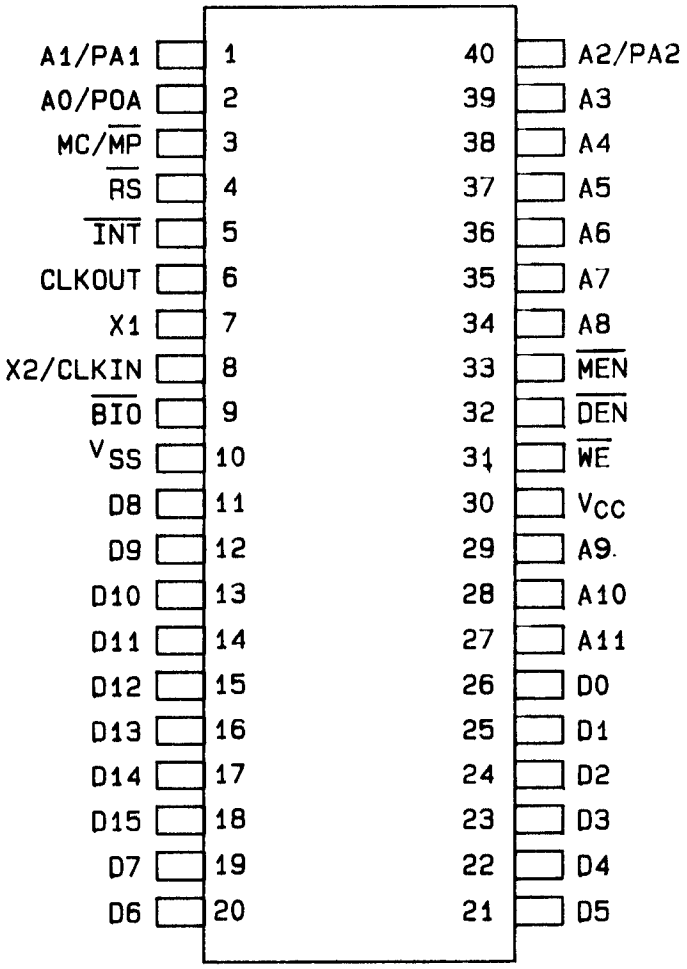

FIGURE 1. Terminal connections.

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Case Z
Device type 01

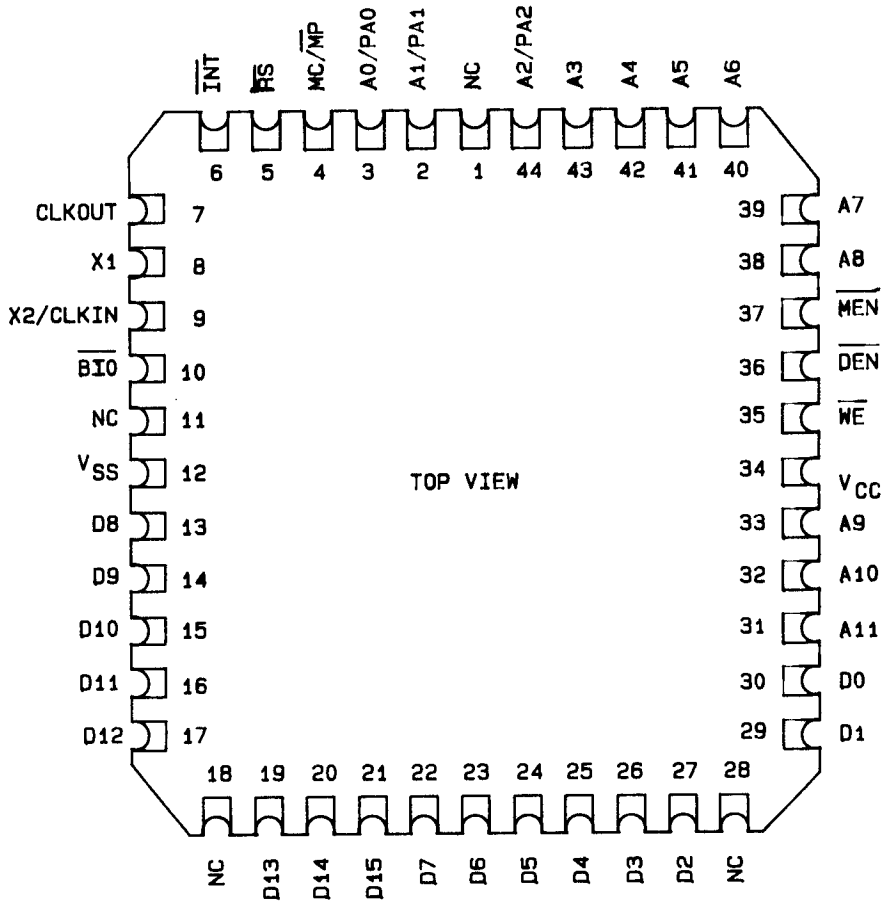

FIGURE 1. Terminal connections - Continued.

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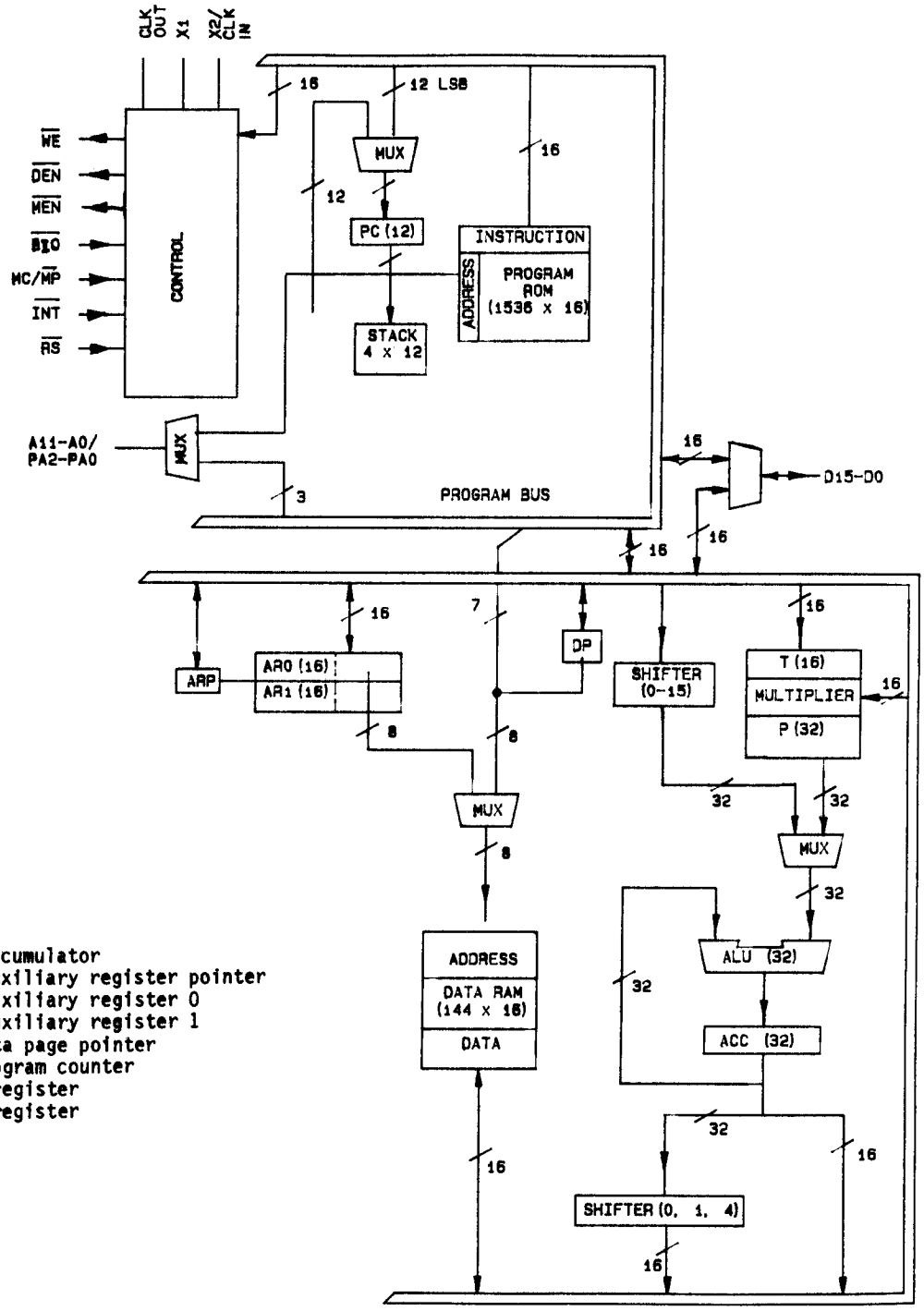

NOTE:
ACC = Accumulator
ARP = Auxiliary register pointer
AR0 = Auxiliary register 0
AR1 = Auxiliary register 1
DP = Data page pointer
PC = Program counter
P = P register
T = T register

FIGURE 2. Functional block diagram.

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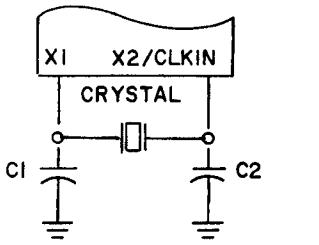
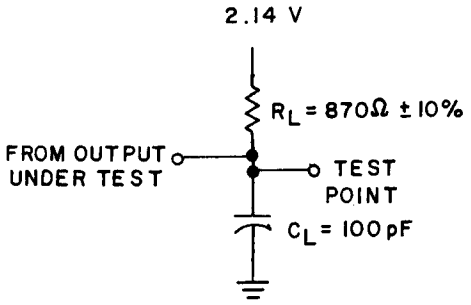
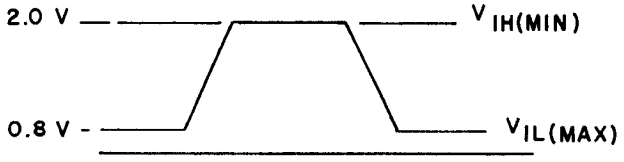


INTERNAL CLOCK OPTION



NOTE: Equivalent TTL load may be used.



INPUT VOLTAGE REFERENCE WAVEFORM

FIGURE 3. AC loading circuits and switching waveforms.

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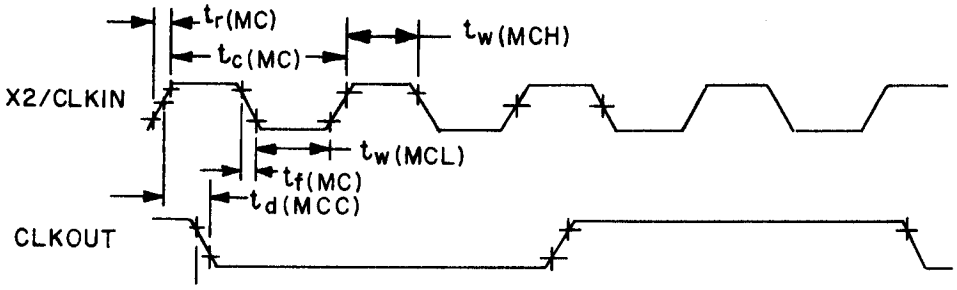
Clock Timing



NOTES:
1. t_d (MCC) referenced to an intermediate level of 1.5 volts on the CLKIN waveform.
2. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

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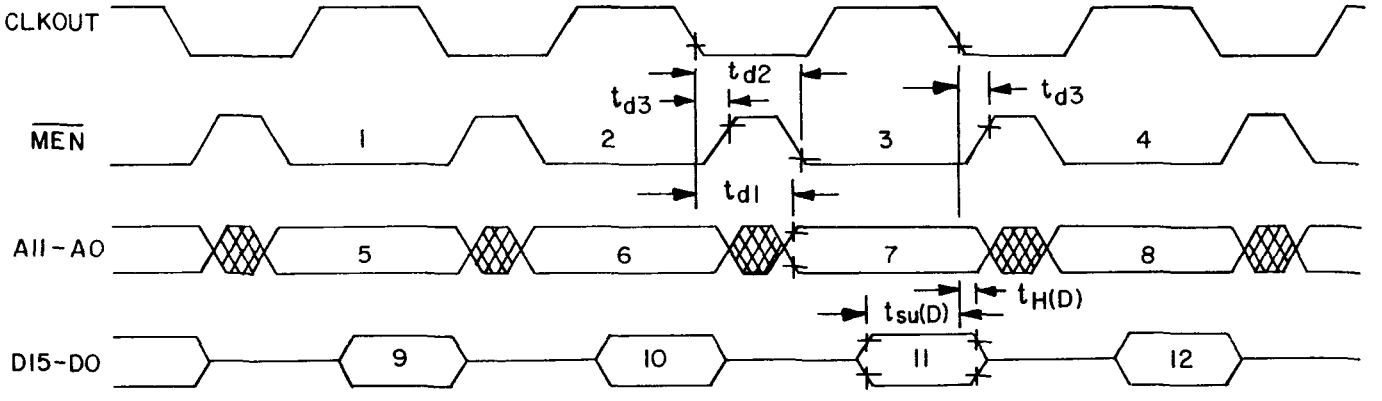
TBLR INSTRUCTION TIMING



LEGEND

1. TBLR INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. DATA FETCH
4. NEXT INSTRUCTION PREFETCH
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. ADDRESS BUS VALID
9. INSTRUCTION IN VALID
10. INSTRUCTION IN VALID
11. DATA IN VALID
12. INSTRUCTION IN VALID

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

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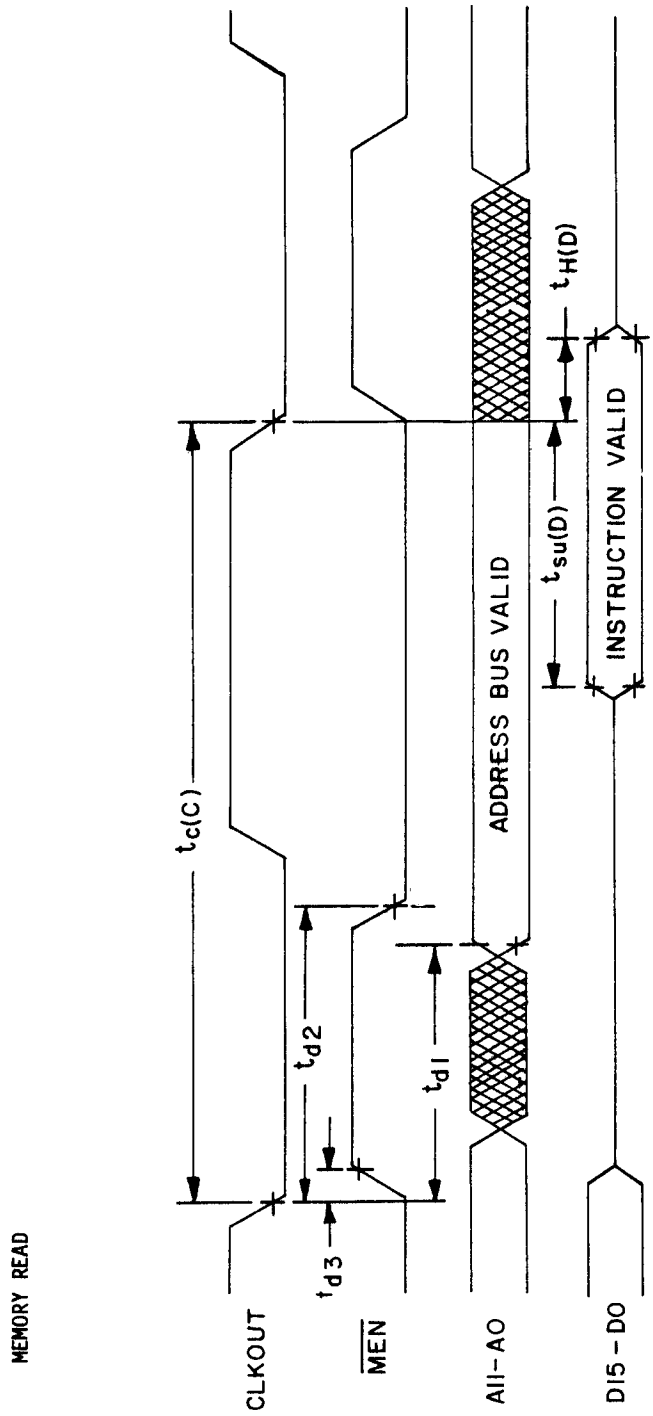

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

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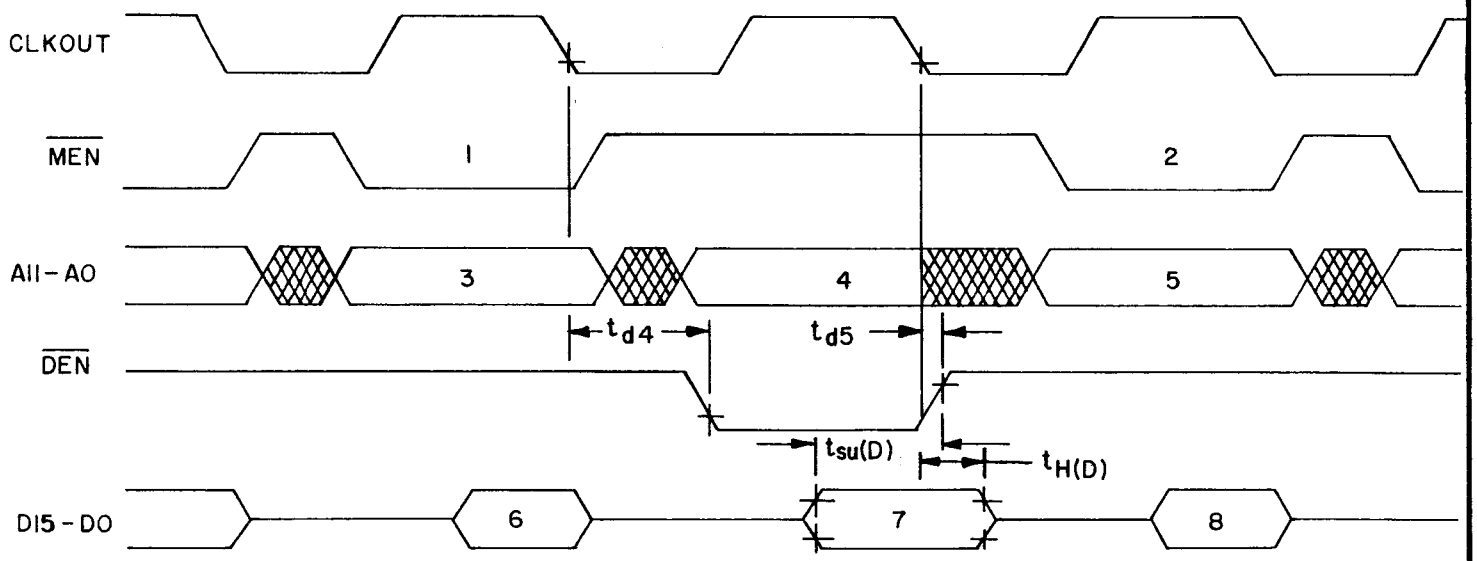
IN INSTRUCTION TIMING



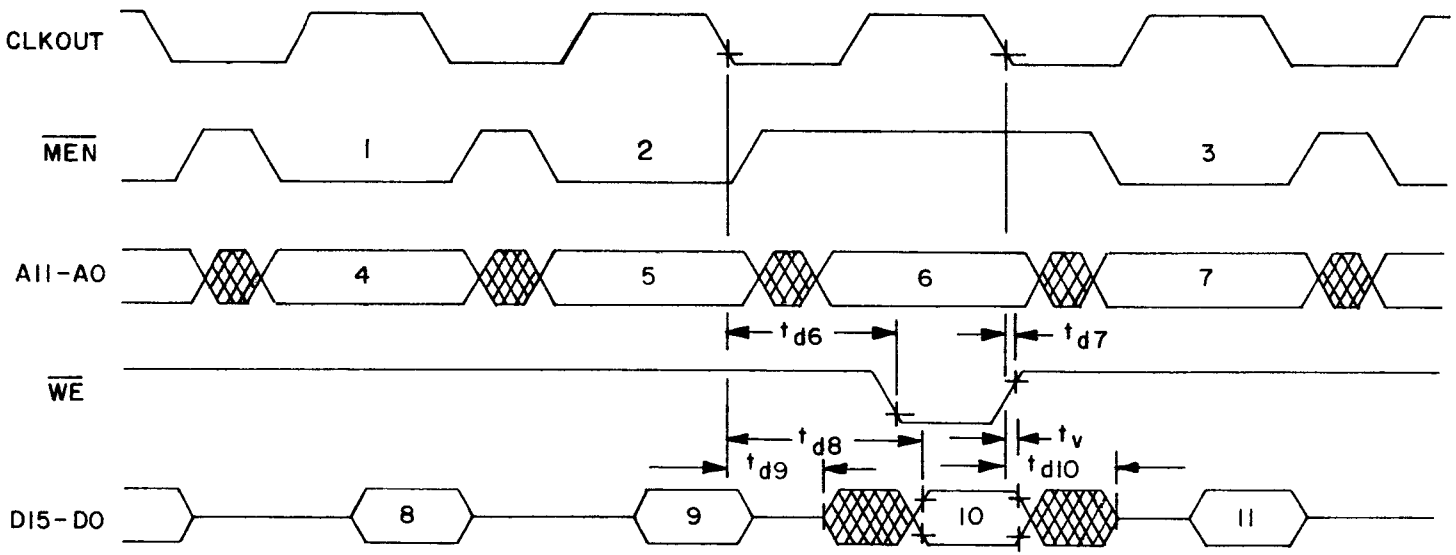
LEGEND

1. IN INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION IN VALID
7. DATA IN VALID
8. INSTRUCTION IN VALID

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

TBLW INSTRUCTION TIMING



LEGEND
1. TBLW INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. NEXT INSTRUCTION PREFETCH
4. ADDRESS BUS VALID
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. INSTRUCTION IN VALID
9. INSTRUCTION IN VALID
10. DATA OUT VALID
11. INSTRUCTION IN VALID

NOTE: Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

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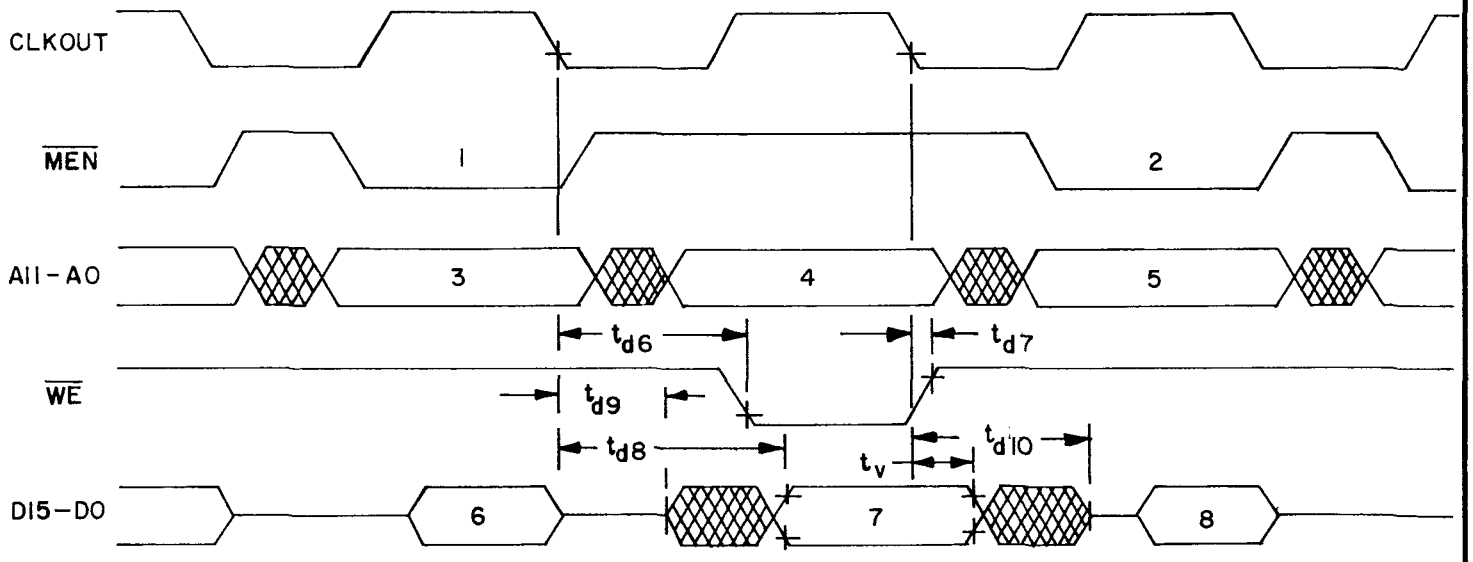
OUT INSTRUCTION TIMING



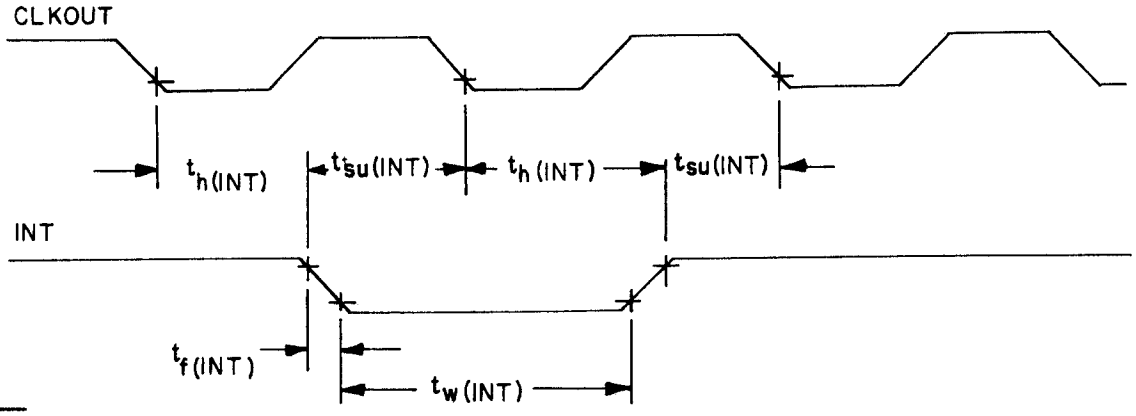
LEGEND

1. OUT INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION IN VALID
7. DATA OUT VALID
8. INSTRUCTION IN VALID

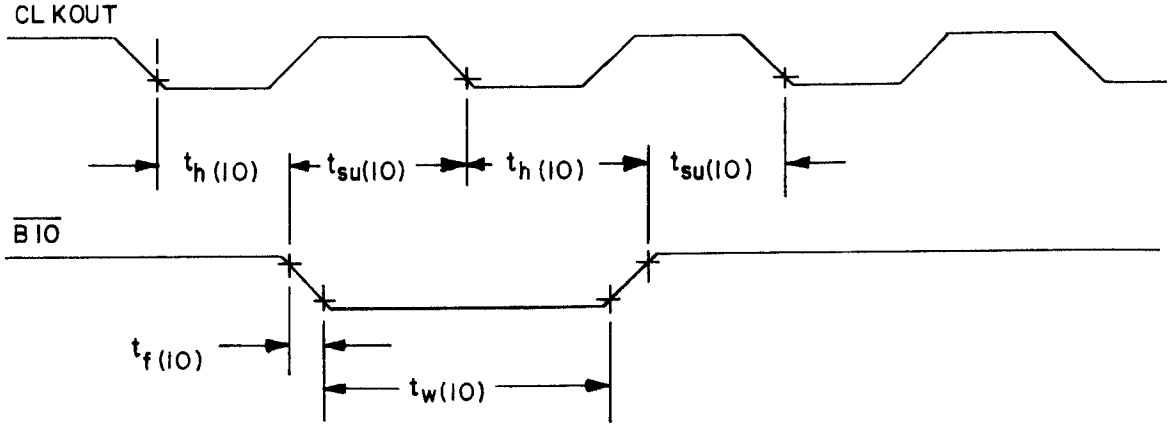
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

INTERRUPT TIMING



$\overline{BIO}$ TIMING



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

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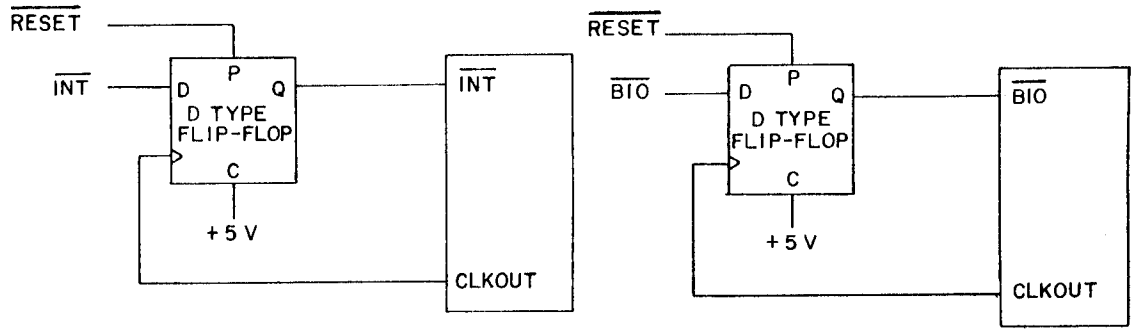
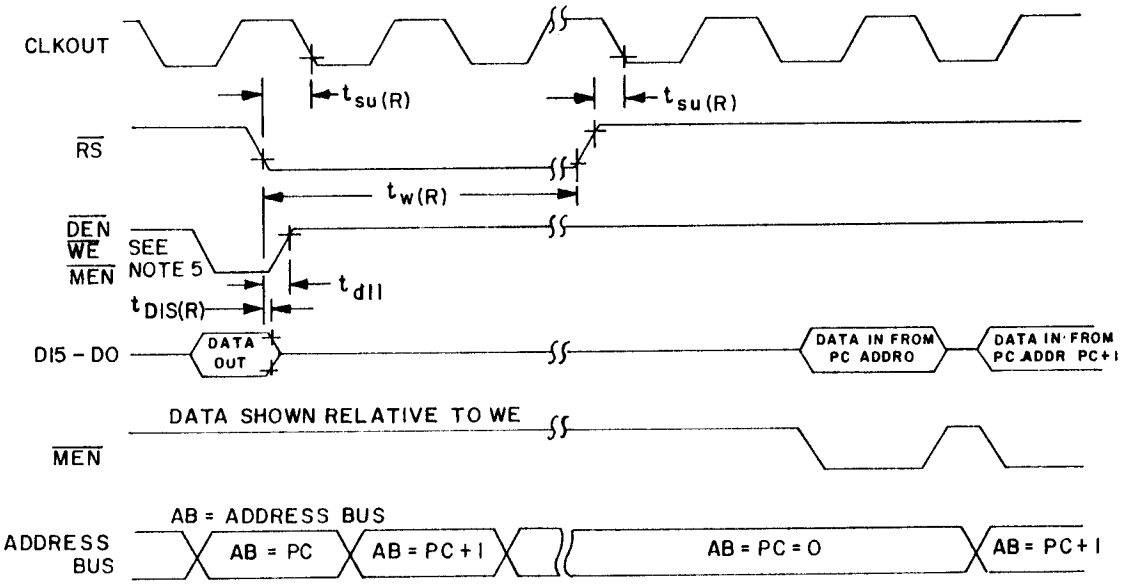


SUGGESTED INPUT SYNCHRONIZATION CIRCUITS
FOR ASYCHRONOUS INTERRUPT AND BIO SYSTEM DESIGN

RESET TIMING



NOTES:

1. $\overline{RS}$ forces $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ high and three-states data bus DO through D15. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\downarrow\overline{RS}$.
2. $\overline{RS}$ must be maintained active low for a minimum of five clock cycles to be recognized.
3. Resumption of normal program will commence after one complete CLK cycle for $\uparrow\overline{RS}$.
4. Due to the synchronizing action on $\overline{RS}$, time to execute the function can vary dependent upon when $\uparrow\overline{RS}$ or $\downarrow\overline{RS}$ occur in the CLK cycle.
5. Diagram shown is for definition purpose only. $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ are mutually exclusive.
6. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
7. During a write cycle, $\overline{RS}$ may produce an invalid write address.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}/C_{OUT}/C_{I/O}$/C1/C2 measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum of 5 devices shall be required with zero rejects.

d. Subgroups 7 and 8 shall verify the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Initial electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8 9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8A,10

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Terms and definitions. The terms and definitions used herein are defined as follows:

TERMINAL	I/O	DEFINITION
A11-A0/ PA2-PA0	OUT	External address bus. I/O port address multiplexed over PA2-PA0.
$\overline{BIO}$	IN	External polling input for bit test and jump operations.
CLKOUT	OUT	System clock output, 1/4 crystal/CLKIN frequency.
D15-D0	I/O	16-bit data bus.
$\overline{DEN}$	OUT	Data enable indicates the processor accepting input data on D15-D0.
$\overline{INT}$	IN	Interrupt.
MC/$\overline{MP}$	IN	Memory mode select pin. High selects microcomputer mode. Low selects microprocessor mode.
$\overline{MEN}$	OUT	Memory enable indicates that D15-D0 will accept external memory instruction.
$\overline{RS}$	IN	Reset used to initialize the device.
V_{CC}	IN	Power.
V_{SS}	IN	Ground.
$\overline{WE}$	OUT	Write enable indicates valid data on D15-D0.
X1	IN	Crystal input.
X2/CLKIN	IN	Crystal input or external clock input.

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6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
8405301QX	01295	SMJ32010JDS
8405301QX	60991	DSP32010BQX
8405301ZX	01295	SMJ32010FDS
8405301ZX	60991	DSP32010BUX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor FSCM number	Vendor name and address
01295	Texas Instruments P.O. Box 6448 Midland, TX 79711
60991	General Instrument Corporation Microelectronics Division 2355 W. Chandler Boulevard Chandler, AZ 85224-6199

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