

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Converted to military drawing format. Change V_{IL} , I_{IL} , V_{OH} , and propagation delays. Remove vendor CAGE 01295 for device 02.	86-10-14	C. Reusing
B	Change input voltage range. Changes made to table I. Change Logic diagram. Editorial changes throughout. Change code ident. No to 67268. Change vendor similar part no. to indicate A version.	87-09-11	N. A. Hauck
C	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	05-01-13	Raymond Monnin
D	Update to current MIL-PRF-38535 requirements. - jt	14-10-16	C. SAFFLE
E	Update drawing to latest MIL-PRF-38535 requirements. - jt	19-07-01	C. SAFFLE



THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

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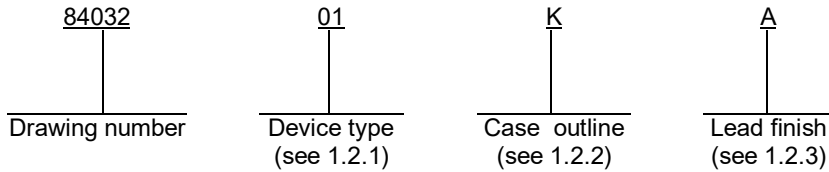
REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12				

PMIC N/A	PREPARED BY David W. Queenan	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime</p>					
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY D. A. DiCenzo						
	APPROVED BY Charles Reusing	<p align="center">MICROCIRCUITS, DIGITAL, ADVANCED LOW POWER SCHOTTKY TTL, DUAL 4-BIT TRANSPARENT LATCH, MONOLITHIC SILICON</p>					
	DRAWING APPROVAL DATE 84-05-17						
	REVISION LEVEL E	SIZE A	CAGE CODE 14933	84032			
		SHEET 1 OF 12					

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ALS873	Dual 4-bit D-type transparent latch with three-state outputs
02	54ALS880	Dual 4-bit D-type transparent latch with inverted three-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
K	GDFP2-F24 or CDFP3-F24	24	flat
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line
3	CQCC1-N28	28	leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	+1.2 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) ^{1/} :	
Device types 01 and 02	170.5 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Junction temperature (T _J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V _{IH})	2.0 V dc
Maximum low level input voltage (V _{IL})	0.7 V dc
Case operating temperature range (T _C)	-55°C to +125°C
Input set-up time, t _(setup) :	
Device types 01 and 02	10 ns minimum
Input hold time, t _(hold) :	
Device type 01	7 ns minimum
Device type 02	10 ns minimum

^{1/} Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short circuit test; e.g., I_o.

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1.4 Recommended operating conditions - Continued.

Input pulse width, $t_{(p)}$:	
Device type 01 (enable)	10 ns minimum
Device type 02 (enable)	15 ns minimum
Device type 01 (clear)	15 ns minimum
Device type 02 (preset)	15 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

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3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -1.0 mA V _{IN} = 0.7 V or 2.0 V		1, 2, 3	All	2.4		V
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA V _{IN} = 0.7 V or 2.0 V		1, 2, 3	All		0.4	V
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA, T _C = +25°C		1	All		-1.5	V
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _{IL} = 0.4 V		1, 2, 3	All		-200	μA
High level input current	I _{IH1}	V _{CC} = 5.5 V, V _{IH} = 2.7 V		1, 2, 3	All		20	μA
	I _{IH2}	V _{CC} = 5.5 V, V _{IH} = 7.0 V		1, 2, 3	All		110	μA
Output current	I _O	V _{CC} = 5.5 V, V _O = 2.25 V _{1/}		1, 2, 3	All	-15	-112	mA
Output current, high level, outputs OFF	I _{OZH}	V _{CC} = 5.5 V, V _{OH} = 2.7 V		1, 2, 3	All		20	μA
Output current, low level, outputs OFF	I _{OZL}	V _{CC} = 5.5 V, V _{OH} = 0.4 V		1, 2, 3	All		-20	μA
Supply current, outputs high	I _{CCH}	V _{CC} = 5.5 V,	V _{IN} = 5.0 V	1, 2, 3	01		21	mA
			V _{IN} = 0 V		02		21	
Supply current, outputs low	I _{CCL}	V _{CC} = 5.5 V	V _{IN} = 0 V	1, 2, 3	01		29	mA
			V _{IN} = 5.0 V		02		29	
Supply current, outputs disabled	I _{CCZ}	V _{CC} = 5.5 V, V _{OC} = 5.0 V	V _{IN} = 0 V	1, 2, 3	01		31	mA
			V _{IN} = 5.5 V		02		31	
Propagation delay time to low level (clear or preset to output)	t _{PHL1}	V _{CC} = 5.0 V, C _L = 50 pF ±10%, R _L = 500Ω		9, 10, 11	All		27	ns
Propagation delay time to high level (enable to output)	t _{PLH2}			9, 10, 11	All		31	ns
Propagation delay time to low level (enable to output)	t _{PHL2}			9, 10, 11	All		26	ns

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time to high level (data to output)	t _{PLH3}	V _{CC} = 5.0 V, C _L = 50 pF ±10% R _L = 500Ω	9, 10, 11	01		23	ns
			9, 10, 11	02		23	ns
Propagation delay time to low level (enable to output)	t _{PHL3}		9, 10, 11	All		17	ns
Output control, ON to high level output	t _{PZH}		9, 10, 11	All		24	ns
Output control, ON to low level output	t _{PZL}		9, 10, 11	All		23	ns
High level output to output, control OFF	t _{PHZ}		9, 10, 11	All		12	ns
Low level output to output, control OFF	t _{PLZ}		9, 10, 11	All		30	ns

1/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}.

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Case outlines	01 L, K	01 3	02 L, K	02 3
Terminal number	Terminal symbols	Terminal symbols	Terminal symbols	Terminal symbols
1	1 CLR	NC	1 PRE	NC
2	1 OC	1 CLR	1 OC	1 PRE
3	1D1	1 OC	1D1	1 OC
4	1D2	1D1	1D2	1D1
5	1D3	1D2	1D3	1D2
6	1D4	1D3	1D4	1D3
7	2D1	1D4	2D1	1D4
8	2D2	NC	2D2	NC
9	2D3	2D1	2D3	2D1
10	2D4	2D2	2D4	2D2
11	2 OC	2D3	2 OC	2D3
12	GND	2D4	GND	2D4
13	2 CLR	2 OC	2 PRE	2 OC
14	2C (ENABLE)	GND	2C (ENABLE)	GND
15	2Q4	NC	2 Q 4	NC
16	2Q3	2 CLR	2 Q 3	2 PRE
17	2Q2	2C (ENABLE)	2 Q 2	2C (ENABLE)
18	2Q1	2Q4	2 Q 1	2 Q 4
19	1Q4	2Q3	1 Q 4	2 Q 3
20	1Q3	2Q2	1 Q 3	2 Q 2
21	1Q2	2Q1	1 Q 2	2 Q 1
22	1Q1	NC	1 Q 1	NC
23	1C (ENABLE)	1Q4	1C (ENABLE)	1 Q 4
24	V _{cc}	1Q3	V _{cc}	1 Q 3
25	---	1Q2	---	1 Q 2
26	---	1Q1	---	1 Q 1
27	---	1C (ENABLE)	---	1C (ENABLE)
28	---	V _{cc}	---	V _{cc}

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Device type 01

Output control	Clear	Enable	Data	Output
\overline{OC}	\overline{CLR}	C	D	Q
H	X	X	X	Z
L	L	X	X	L
L	H	L	X	Q ₀
L	H	H	L	L
L	H	H	H	H

Device type 02

Output control	Clear	Enable	Data	Output
\overline{OC}	\overline{PRE}	C	D	\overline{Q}
H	X	X	X	Z
L	L	X	X	L
L	H	L	X	Q ₀
L	H	H	L	L
L	H	H	H	H

H = High level (steady state).

L = Low level, (steady state).

Z = High impedance state.

X = Irrelevant.

Q₀ = The level of Q or \overline{Q} before the indicated input conditions were established.

FIGURE 2. Truth table.

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Device type 01

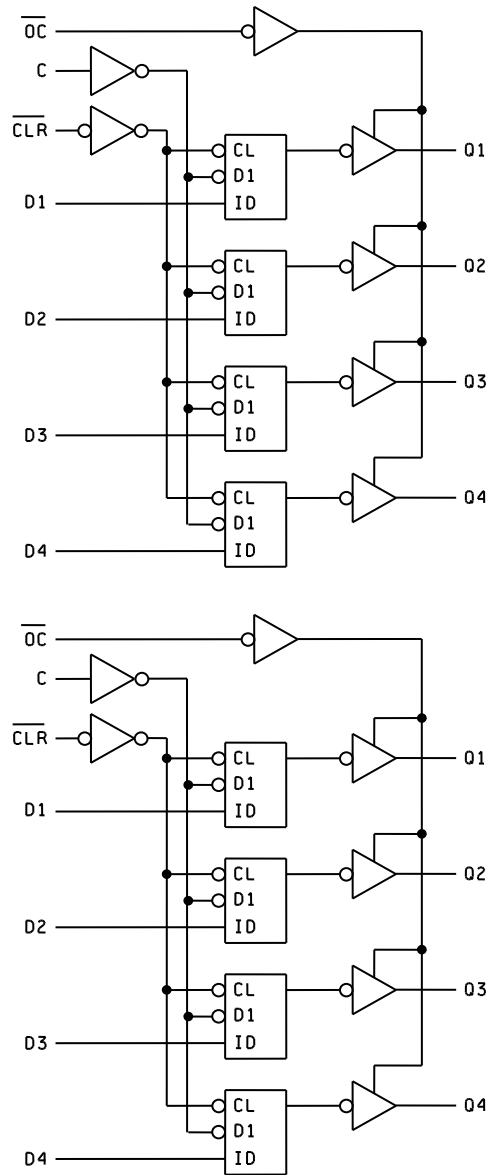


FIGURE 3. Logic diagram.

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Device type 02

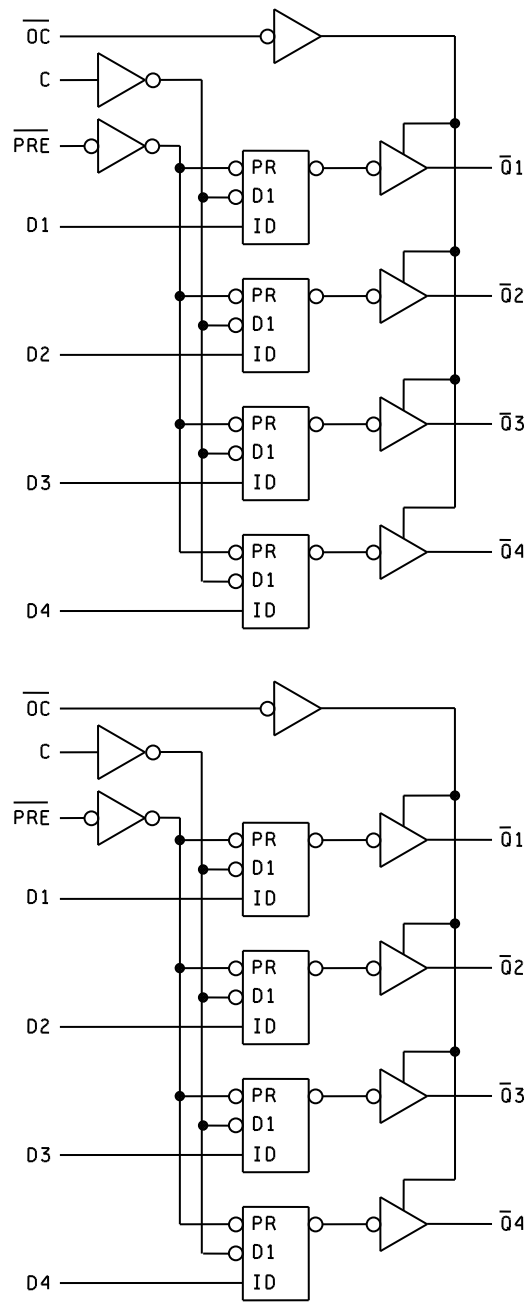


FIGURE 3. Logic diagram - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6 and 8 in table I and table II, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-01

Approved sources of supply for SMD 84032 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification part number
8403201LA	01295	SNJ54ALS873BJT	M38510/38203BLA
8403201KA	01295	SNJ54ALS873BW	M38510/38203BKA
84032013A	01295	SNJ54ALS873BFK	M38510/38203B3A
8403202LA	<u>3/</u>	SNJ54ALS880AJT	M38510/38204BLA
8403202KA	<u>3/</u>	SNJ54ALS880AW	M38510/38204BKA
84032023A	<u>3/</u>	SNJ54ALS880AFK	M38510/38204B3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
P.O. Box 660199
Dallas, TX 75243

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