REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Change power dissipation to 22 mW. Change clock pulse setup, hold, and propagation delay times. Change clock frequency. Change to military drawing format. Change code ident. no. to 67268. Change table I footnotes. Add figure 4. Editorial changes throughout.	88-04-06	M. A. Frye
D	Changes in accordance with NOR 5962-R246-92. -tmh	92-07-10	Monica L. Poelking
E	Changes in accordance with NOR 5962-R097-93. -ltg	93-03-12	Monica L. Poelking
F	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	02-07-29	Raymond Monnin
G	Update to reflect latest changes in format and requirements. Correct paragraph in 3.5. Editorial changes throughout. –les	05-07-26	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY

Joseph A. Kirby

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Raymond Monnin

APPROVED BY

Michael A. Frye

DRAWING APPROVAL DATE

84-05-04

REVISION LEVEL

G

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW-POWER SCHOTTKY TTL, DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOPS WITH CLEAR AND RESET, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**84011**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

84011	01	C	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS74	Dual D-type positive-edge-triggered flip-flops

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	22 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL}) :	
T_C = +125°C	0.7 V dc
T_C = +25°C	0.8 V dc
T_C = -55°C	0.8 V dc
Setup time before CLK, data (t_{su})	15 ns
Setup time before CLK, $\overline{PRE}$ or $\overline{CLR}$ inactive (t_{su})	10 ns

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit test; e.g., I_O.

Hold time, data after CLK (t_h)	0 ns
Pulse duration, $\overline{PRE}$ or $\overline{CLR}$ low (t_W)	15 ns
Pulse duration, CLK high or low (t_W)	16.5 ns
Clock frequency (f_{CLOCK})	30 MHz
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuits and switching waveforms. The test circuits and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ 2/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OH} = -0.4 mA 3/	V_{IL} = 0.7 V	2	All	2.5		V
			V_{IL} = 0.8 V	1, 3		2.5		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = 4.0 mA 3/	V_{IL} = 0.7 V	2	All		0.4	V
			V_{IL} = 0.8 V	1, 3			0.4	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3	All		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V, All other inputs = 4.5 V	CLK or D	1, 2, 3	All		-0.2	mA
			$\overline{PRE}$ or $\overline{CLR}$				-0.4	
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V, All other inputs = 0.0 V	CLK or D	1, 2, 3	All		20	µA
			$\overline{PRE}$ or $\overline{CLR}$				40	
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V, All other inputs = 0.0 V	CLK or D	1, 2, 3	All		0.1	mA
			$\overline{PRE}$ or $\overline{CLR}$				0.2	
Output current	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V 4/		1, 2, 3	All	-20	-112	mA
Supply current	I_{CC}	V_{CC} = 5.5 V, 5/		1, 2, 3	All		4.0	mA
Functional tests		See 4.3.1c 6/		7, 8	All			
Propagation delay time, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$	t_{PLH1}	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500Ω, See figure 4 7/		9, 10, 11	All	3	18	ns
	t_{PHL1}			9, 10, 11	All	5	17	
Propagation delay time, CLK to Q or $\overline{Q}$	t_{PLH2}			9, 10, 11	All	5	17	ns
	t_{PHL2}			9, 10, 11	All	5	18	

1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V or ≤ 0.4 V.

2/ Unused inputs shall not exceed 5.5 V or go less than 0.0 V. No input shall be floated.

3/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or the V_{IH} minimum input.

4/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.

5/ I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

6/ Functional tests shall be conducted at input test conditions of $GND \le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

7/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

Device types	01	01
Case outlines	C, D	2
Terminal number	Terminal symbols	
1	1 $\overline{CLR}$	NC
2	1D	1 $\overline{CLR}$
3	1CLK	1D
4	1 $\overline{PRE}$	1CLK
5	1Q	NC
6	1 $\overline{Q}$	1 $\overline{PRE}$
7	GND	NC
8	2 $\overline{Q}$	1Q
9	2Q	1 $\overline{Q}$
10	2 $\overline{PRE}$	GND
11	2CLK	NC
12	2D	2 $\overline{Q}$
13	2 $\overline{CLR}$	2Q
14	V_{CC}	2 $\overline{PRE}$
15	- - -	NC
16	- - -	2CLK
17	- - -	NC
18	- - -	2D
19	- - -	2 $\overline{CLR}$
20	- - -	V_{CC}

FIGURE 1. Terminal connections.

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FIGURE 2. Truth tables.

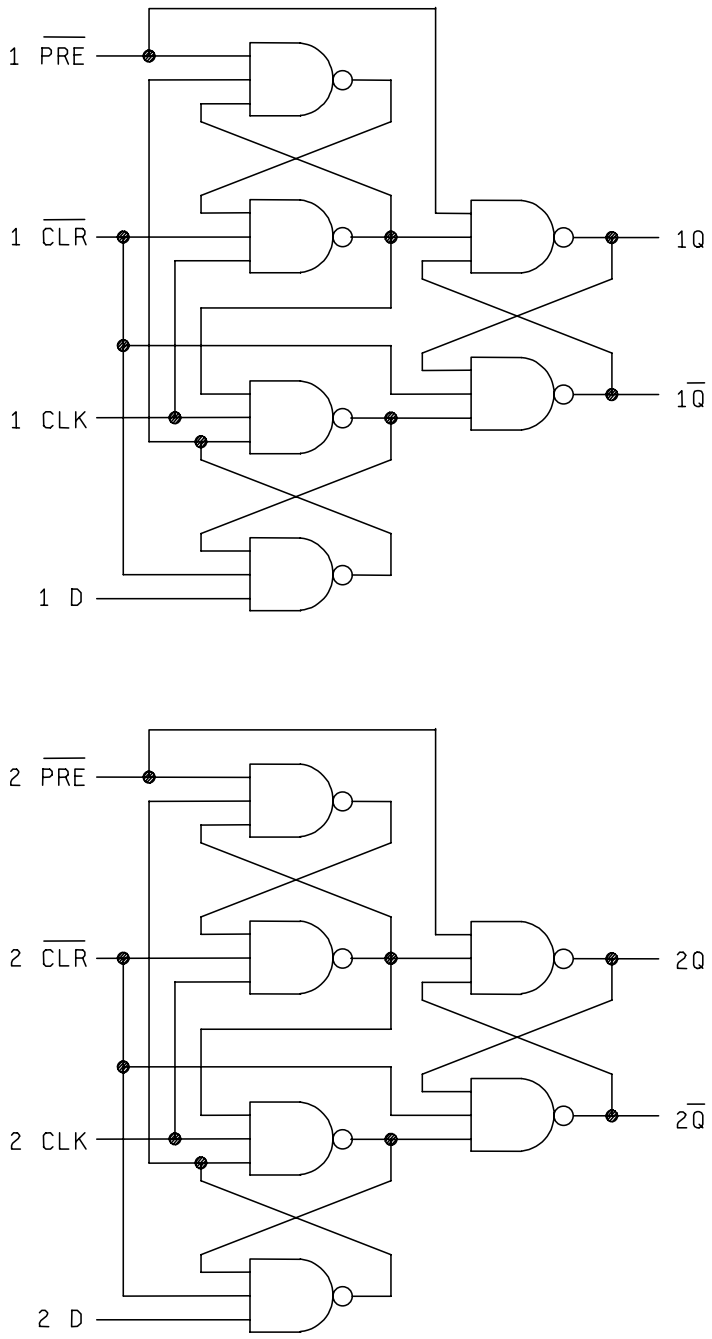
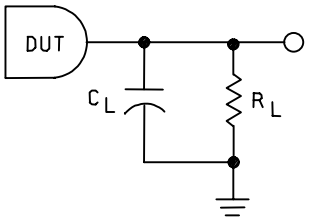
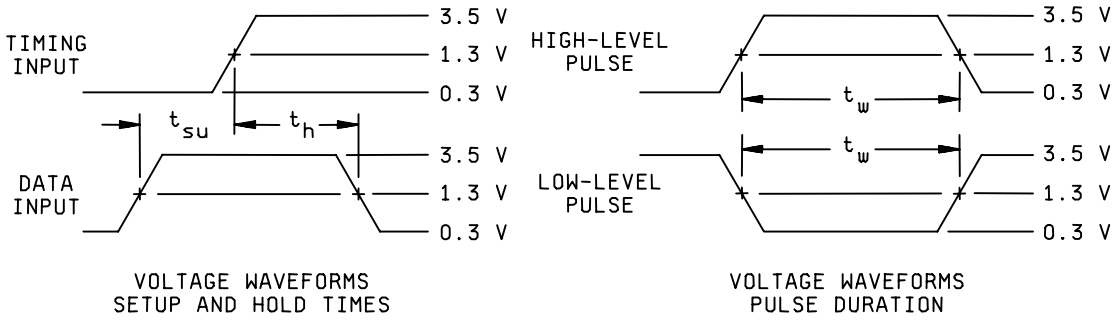


FIGURE 3. Logic diagram.

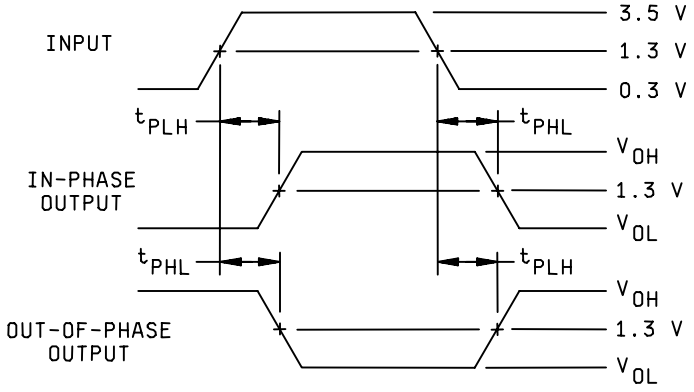


LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:
1. C_L includes probe and jig capacitance.
2. All inputs have the following characteristics: PRR ≤ 10 MHz, duty cycle = 50 percent, $t_r = t_f = 3$ ns ±1 ns.
3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Test circuit and switching waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-07-26

Approved sources of supply for SMD 84011 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
8401101AA	3/	- - -	M38510/37101BAA
8401101BA	3/	- - -	M38510/37101BBA
8401101CA	01295 3/ 3/	SNJ54ALS74AJ 54ALS74J/883 54ALS74A/BCA	M38510/37101BCA
8401101DA	01295 3/ 3/	SNJ54ALS74AW 54ALS74W/883 54ALS74A/BDA	M38510/37101BDA
84011012A	01295 3/ 3/	SNJ54ALS74AFK 54ALS74E/883 54ALS74A/B2A	M38510/37101B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, Tx 75243 POC U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493