

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor, FSCM 04713. Editorial changes throughout.	85-04-23	N. A. HAUCK
B	Change FMAX and prop delays in table I. Change recommended width of clock pulse.	85-09-23	N. A. HAUCK
C	Add vendor FSCM 27014. Change VIL and ICCL. Editorial changes throughout	86-04-21	N. A. HAUCK
D	Change propagation delays. Convert to military drawing format. Device 01, Case R inactive for new design.	87-02-24	N. A. HAUCK
E	Change input voltage range. Update table I and Figure 2. Update 6.4.	87-06-26	N. A. HAUCK
F	Table I, added footnotes and changed propagation delay times. Added figure 4, switching waveforms and test circuit. Editorial changes throughout. Added CAGE 18324. Table II, subgroups added. Device type 01, case 2 is inactive for new design.	88-05-13	M. A. FRYE
G	Changes in accordance with NOR 5962-R258-92. - car	92-07-10	M. L. POELKING
H	Changes in accordance with NOR 5962-R125-93. - tvn	93-06-09	M. L. POELKING
J	Update to reflect latest changes in format and requirements. Editorial changes throughout. Reactivate device type 01, case 2 for new design. - les	02-07-29	R. MONNIN
K	Make a correction to the Marking paragraph 3.5. - ro	05-06-29	R. MONNIN
L	Update drawing to current MIL-PRF-38535 requirements. - jt	15-06-24	C. SAFFLE
M	Update drawing to latest MIL-PRF-38535 requirements. - jt	20-04-02	James R. Eschmeyer



CURRENT CAGE CODE 67268

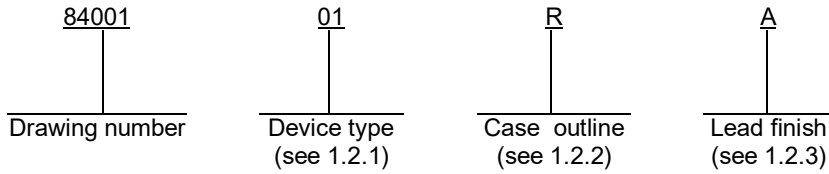
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS OF SHEETS	REV	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY GREG A. PITZ				DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime														
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. A. DiCENZO																		
	APPROVED BY N. A. HAUCK																		
	DRAWING APPROVAL DATE 84-04-12																		
	REVISION LEVEL M																		
				SIZE A	CAGE CODE 14933	84001													
				SHEET		1 OF 14													

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ALS574	Octal D-type flip-flop with three state outputs
02	54ALS576	Octal D-type flip-flop with three state inverted outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.2 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (Pd) ^{1/} :	
Device type 01	154.0 mW
Device type 02	165.0 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Junction temperature (T _J)	+175°C

^{1/} Maximum power dissipation is defined as VCC x ICC, and must withstand the added PD due to short-circuit test; e.g., IO.

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1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V _{IH})	2.0 V dc
Maximum low level input voltage (V _{IL}) :	
T _C = +125°C	0.7 V dc
T _C = +25°C	0.8 V dc
T _C = -55°C	0.8 V dc
Case operating temperature range (T _C)	-55°C to +125°C
Width of clock pulse (t _w) :	
Device type 01	16.5 ns minimum
Device type 02	25 ns minimum
Data setup time (t _{su})	15 ns minimum
Data hold time (t _h)	4 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -0.4 mA, 2/ V _{IH} = 2.0 V, V _{IL} = 0.7 or 0.8 V	1, 2, 3	All	2.5		V
		V _{CC} = 4.5 V, I _{OH} = -1.0 mA, 2/ V _{IH} = 2.0 V, V _{IL} = 0.7 or 0.8 V			2.4		
Low level output voltage	V _{OL}	I _{OL} = 12 mA, V _{CC} = 4.5 V, 2/ V _{IH} = 2.0 V, V _{IL} = 0.7 or 0.8 V	1, 2, 3	All		0.4	V
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA	1, 2, 3	All		-1.2	V
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.4 V, all other inputs = 4.5 V	1, 2, 3	All		-0.2	mA
High level input current	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.7 V, unused inputs = 0.0 V	1, 2, 3	All		20	μA
	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 7.0 V, unused inputs = 0.0 V				100	
Off-state output current	I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V	1, 2, 3	All		20	μA
	I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.4 V				-20	
Output current	I _O	V _{CC} = 5.5 V, V _{OUT} = 2.25 V 3/	1, 2, 3	01	-20	-112	mA
				02	-15	-112	
Supply current	I _{CCH}	V _{CC} = 5.5 V, V _{IN} ≥ 4.5 V	1, 2, 3	01		18	mA
		V _{CC} = 5.5 V, V _{IN} ≤ 0.4 V		02		18	
	I _{CCL}	V _{CC} = 5.5 V, V _{IN} ≤ 0.4 V	01		27		
		V _{CC} = 5.5 V, V _{IN} ≥ 4.5 V	02		24		
Supply current outputs disabled	I _{CCZ}	V _{CC} = 5.5 V, V _{IN} ≥ 4.5 V	1, 2, 3	01		28	mA
				02		30	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional tests		See 4.3.1c <u>4/</u>	7, 8	All			
Maximum clock frequency	f _{MAX}	V _{CC} = 4.5 V to 5.5 V, <u>5/</u> C _L = 50 pF ± 10%, R _L = 500 Ω ± 5%, see figure 4	9, 10, 11	01	30		MHz
				02	22		
Propagation delay time, CLK to any Q or \bar{Q}	t _{PLH1}	V _{CC} = 4.5 V to 5.5 V, <u>5/</u> C _L = 50 pF ± 10%, R _L = 500 Ω ± 5%, see figure 4	9, 10, 11	01	4	16	ns
				02	4	24	
	t _{PHL1}	R _L = 500 Ω ± 5%, see figure 4	01	4	14		
			02	4	20		
Output enable \overline{OC} to any Q or \bar{Q}	t _{PZL}	V _{CC} = 4.5 V to 5.5 V, <u>5/</u> C _L = 50 pF ± 10%, R _L = 500 Ω ± 5%, see figure 4	9, 10, 11	01	4	26	ns
				02	3	23	
	t _{PZH}	R _L = 500 Ω ± 5%, see figure 4	01	4	18.5		
			02	4	24		
Output disable \overline{OC} to any Q or \bar{Q}	t _{PLZ}	V _{CC} = 4.5 V to 5.5 V, <u>5/</u> C _L = 50 pF ± 10%, R _L = 500 Ω ± 5%, see figure 4	9, 10, 11	01	2	15	ns
				02	2	29	
	t _{PHZ}	R _L = 500 Ω ± 5%, see figure 4	01	2	10		
			02	2	14		

1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V or ≤ 0.4 V. Unused inputs shall not exceed 5.5 V or go less than 0.0 V. No input shall be floated.

2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or the V_{IH} minimum input.

3/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.

4/ Functional tests shall be conducted at input test conditions of GND ≤ V_{IL} ≤ V_{OL} and V_{OH} ≤ V_{IH} ≤ V_{CC}.

5/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

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Device types	01		02	
Case outlines	R, S	2	R, S	2
Terminal number	Terminal symbols			
1	\overline{OC}	\overline{OC}	\overline{OC}	\overline{OC}
2	1D	1D	1D	1D
3	2D	2D	2D	2D
4	3D	3D	3D	3D
5	4D	4D	4D	4D
6	5D	5D	5D	5D
7	6D	6D	6D	6D
8	7D	7D	7D	7D
9	8D	8D	8D	8D
10	GND	GND	GND	GND
11	CLK	CLK	CLK	CLK
12	8Q	8Q	$8\overline{Q}$	$8\overline{Q}$
13	7Q	7Q	$7\overline{Q}$	$7\overline{Q}$
14	6Q	6Q	$6\overline{Q}$	$6\overline{Q}$
15	5Q	5Q	$5\overline{Q}$	$5\overline{Q}$
16	4Q	4Q	$4\overline{Q}$	$4\overline{Q}$
17	3Q	3Q	$3\overline{Q}$	$3\overline{Q}$
18	2Q	2Q	$2\overline{Q}$	$2\overline{Q}$
19	1Q	1Q	$1\overline{Q}$	$1\overline{Q}$
20	Vcc	Vcc	Vcc	Vcc

FIGURE 1. Terminal connections.

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Device type 01

\overline{OC}	CLK	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

H = High level

L = Low level

X = Irrelevant

↑ = Transition from low to high level

Q₀ = The level of Q before the indicated steady-state input conditions were established

Z = High impedance state

Device type 02

\overline{OC}	CLK	D	Output \overline{Q}
L	↑	H	L
L	↑	L	H
L	L	X	\overline{Q}_0
H	X	X	Z

H = High level

L = Low level

X = Irrelevant

↑ = Transition from low to high level

\overline{Q}_0 = The level of \overline{Q} before the indicated steady-state input conditions were established

Z = High impedance state

FIGURE 2. Truth tables.

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Device type 01

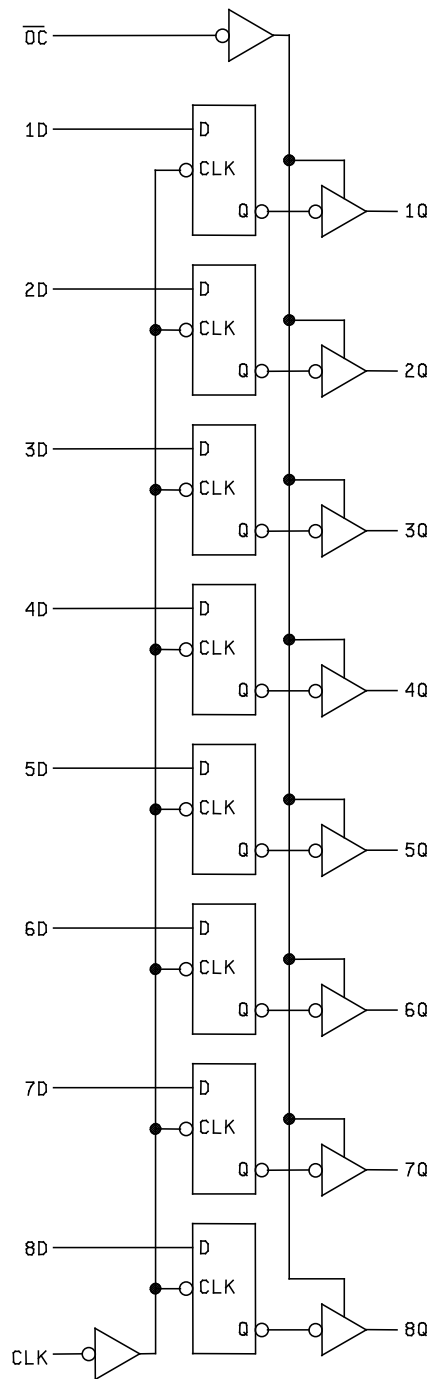


FIGURE 3. Logic diagrams.

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Device type 02

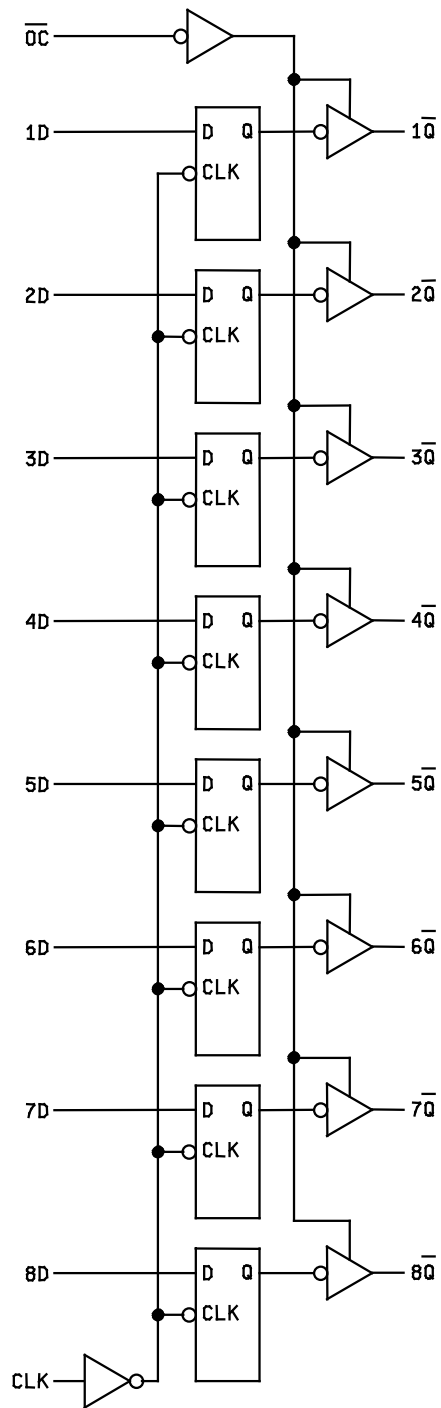


FIGURE 3. Logic diagrams - Continued.

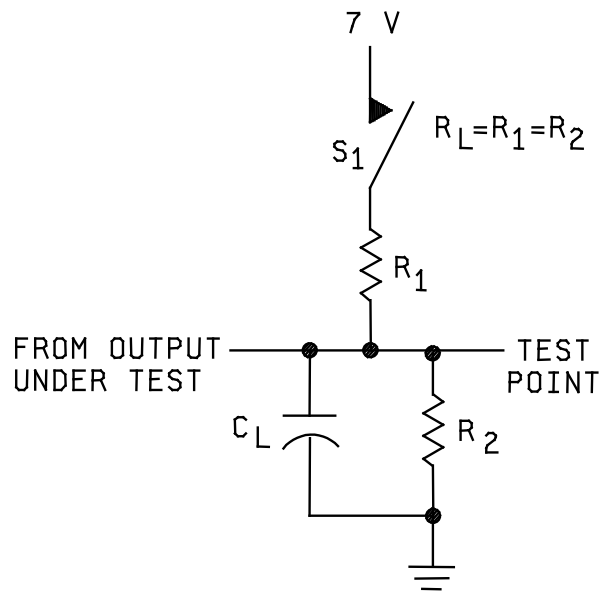
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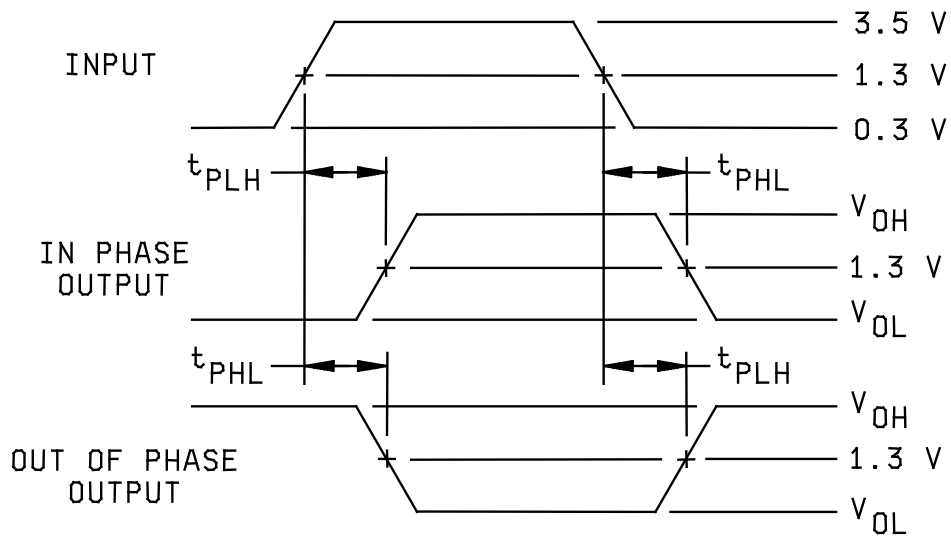
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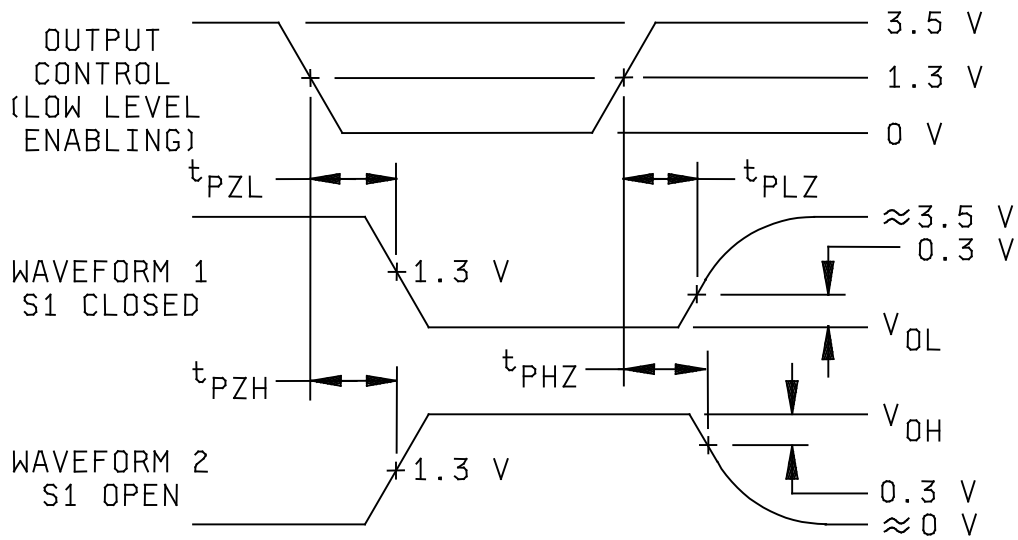
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

FIGURE 4. Test circuits and switching waveforms.

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NOTES:

1. C_L includes probe and jig capacitance.
2. All inputs have the following characteristics: PRR ≤ 10 MHz, duty cycle = 50 percent, t_r = t_f = 3 ns ± 1 ns.
3. The outputs are measured one at a time with one input transition per measurement.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. When measuring propagation delay times of three-state outputs, switch S1 is open.

FIGURE 4. Test circuits and switching waveforms - Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth tables.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-04-02

Approved sources of supply for SMD 84001 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification PIN
8400101RA	01295	SNJ54ALS574BJ	M38510/37104BRA
	<u>3/</u>	54ALS574BJ/883	
	<u>3/</u>	54ALS574A/BRA	
	<u>3/</u>	54ALS574A/BRAJC	
8400101SA	01295	SNJ54ALS574BW	M38510/37104BSA
	<u>3/</u>	54ALS574BW/883	
	<u>3/</u>	54ALS574A/BSA	
	<u>3/</u>	54ALS574A/BSAJC	
84001012A	01295	SNJ54ALS574BFBK	M38510/37104B2A
	<u>3/</u>	54ALS574BE/883	
	<u>3/</u>	54ALS574A/B2A	
	<u>3/</u>	54ALS574A/B2AJC	
8400102RA	01295	SNJ54ALS576BJ	M38510/37105BRA
	<u>3/</u>	54ALS576AJ/883	
8400102SA	<u>3/</u>	SNJ54ALS576BW	M38510/37105BSA
	<u>3/</u>	54ALS576AW/883	
84001022A	01295	SNJ54ALS576BFBK	M38510/37105B2A
	<u>3/</u>	54ALS576AE/883	

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
P.O. Box 660199
Dallas, TX 75243

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