

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change output current, Io. Complete document update.	85-03-06	N. A. Hauck
B	Case E inactive for new design. Remove Vendor FSCM 04713. Editorial changes throughout.	85-07-25	N. A. Hauck
C	Changes in accordance with NOR 5962-R081-92	92-07-07	Phu Nguyen
D	Redraw with changes. Update current requirements. Editorial changes throughout. - gap	05-10-26	Raymond Monnin
E	Update drawing to current MIL-PRF-38535 requirements. - jt	17-09-08	Charles Saffle

CURRENT CAGE CODE 67268

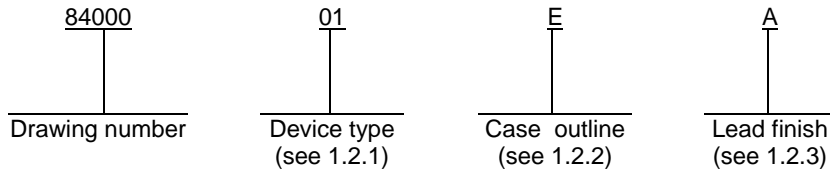


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PMIC N/A	PREPARED BY Greg A. Pitz	<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil</p> <p align="center">MICROCIRCUITS, DIGITAL, ADVANCED LOW-POWER SCHOTTKY TTL, J-K FLIP-FLOPS, MONOLITHIC SILICON</p>																		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p>	CHECKED BY D. A. DiCenzo																			
	APPROVED BY N. A. Hauck																			
	DRAWING APPROVAL DATE 84-04-12																			
AMSC N/A	REVISION LEVEL E	SIZE A	CAGE CODE 14933	84000																
		SHEET		1 OF 11																

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ALS109	Dual J-K flip-flop with clear and preset (active high)
02	54ALS112A	Dual J-K flip-flop with clear and preset (active low)

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	flat package
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V _{CC} +0.5 V dc
DC V _{CC} or GND current (per pin)	±50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) per flip-flop <u>1</u> /:	
Device type 01	11 mW
Device type 02	13 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ _{JC}):	See MIL-STD-1835
Junction temperature (T _J)	+175°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_o).

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1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to +6.0 V dc
Minimum high level input voltage (V_{IH})	2.0 V
Maximum low level input voltage (V_{IL})	0.8 V
Case operating temperature range (T_C)	-55°C to +125°C
Minimum width of CLOCK pulse (t_p CLOCK):	
Device type 01	16.5 ns
Device type 02	20 ns
Minimum width of CLEAR pulse (t_p $\overline{\text{CLEAR}}$):	
Device types 01 and 02	15 ns
Minimum width of PRESET pulse (t_p $\overline{\text{PRESET}}$):	
Device types 01 and 02	15 ns
Minimum data setup time:	
Device type 01	15 ns
Device type 02	25 ns
Minimum $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ inactive state setup time:	
Device type 01	10 ns
Device type 02	22 ns
Minimum data hold time (t_p HOLD):	
Device types 01 and 02	0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 2.

3.2.4 Truth tables. The truth tables shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High-level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IH} = 2.0 V, I _{OH} = -400 μA, V _{IL} = 0.8 V	All	1, 2, 3	2.5		V
Low-level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IH} = 2.0 V, I _{OH} = 4 mA, V _{IL} = 0.8 V	All	1, 2, 3		0.4	V
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA, T _C = 25°C	All	1		-1.5	V
Low level input current at J or \bar{K}	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	All	1, 2, 3		-200	μA
Low level input current \overline{PRE} , \overline{CLR} , or CLK	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	All	1, 2, 3		-400	μA
High level input current at J or \bar{K}	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	All	1, 2, 3		20	μA
High-level input current at \overline{PRE} or \overline{CLR}	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	All	1, 2, 3		40	μA
High level input current at CLK	I _{IH3}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	All	1, 2, 3		80	μA
Output current <u>1/</u>	I _O	V _{CC} = 5.5 V, V _O = 2.25 V	All	1, 2, 3	-20	-112	mA
Supply current <u>2/</u>	I _{CC}	V _{CC} = 5.5 V, V _{IN} = 0 V	01	1, 2, 3		4	mA
			02			4.5	
High level input current J or \bar{K}	I _{IH4}	V _{CC} = 5.5 V, V _{IN} = 7.0 V	All	1, 2, 3		100	μA
High level input current \overline{PRE} or \overline{CLR}	I _{IH5}	V _{CC} = 5.5 V, V _{IN} = 7.0 V	All	1, 2, 3		200	μA
High level input current at CLK	I _{IH6}	V _{CC} = 5.5 V, V _{IN} = 7.0 V	All	1, 2, 3		400	μA
Propagation delay time \overline{CLR} or \overline{PRE} to output	t _{PLH1}	V _{CC} = 5.0 V, C _L = 50 pF ±10%, R _L = 500 Ω	01	9, 10, 11	3	18	ns
			02		3	26	
	t _{PHL1}		01	9, 10, 11	5	17	ns
			02		4	23	
Propagation delay time CLK to output	t _{PLH2}	V _{CC} = 5.0 V, C _L = 50 pF ±10%, R _L = 500 Ω	01	9, 10, 11	5	21	ns
			02		3	23	
	t _{PHL2}		01	9, 10, 11	5	20	ns
			02		5	24	
Maximum clock frequency	f _{max}	V _{CC} = 5.0 V, C _L = 50 pF ±10%, R _L = 500 Ω	01	9, 10, 11	30		MHz
			02		25		

1/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

2/ I_{CC} is measured with outputs open with J, K, CLK and \overline{PRE} grounded; then with J, K, CLK, and \overline{CLR} grounded.

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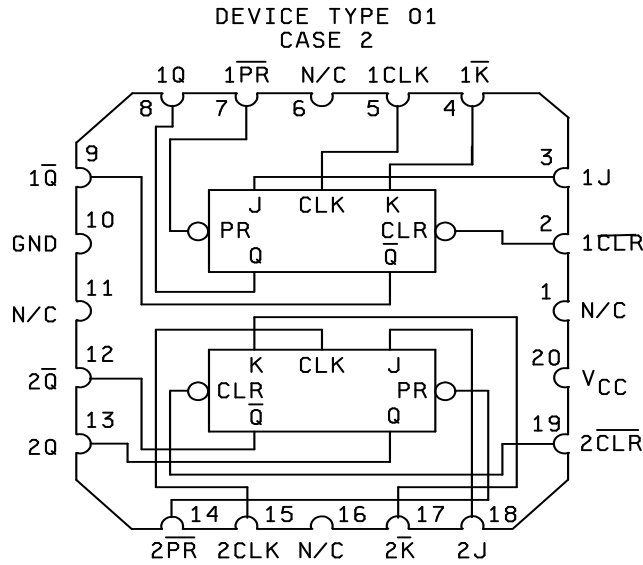
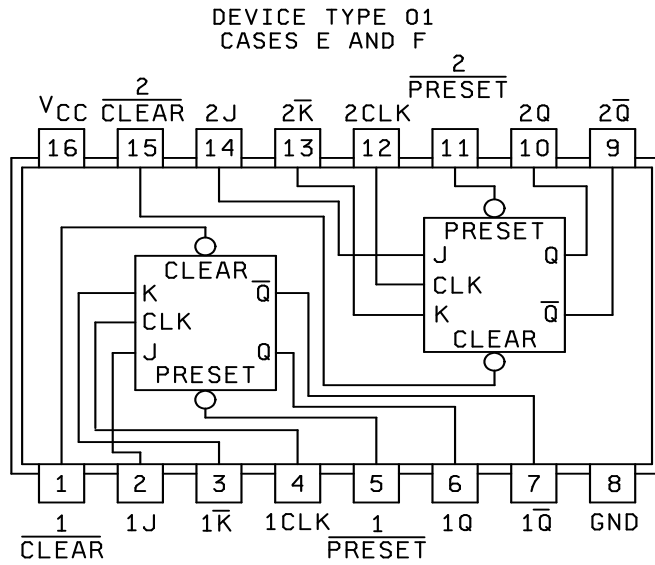


FIGURE 1. Terminal connections (top view).

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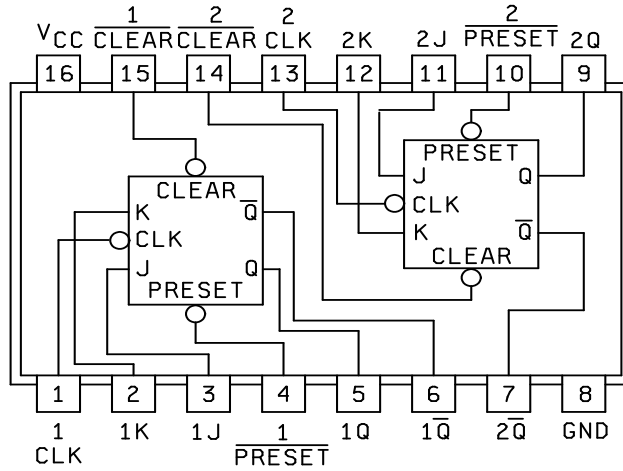
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DEVICE TYPE 02
CASES E AND F



DEVICE TYPE 02
CASE 2

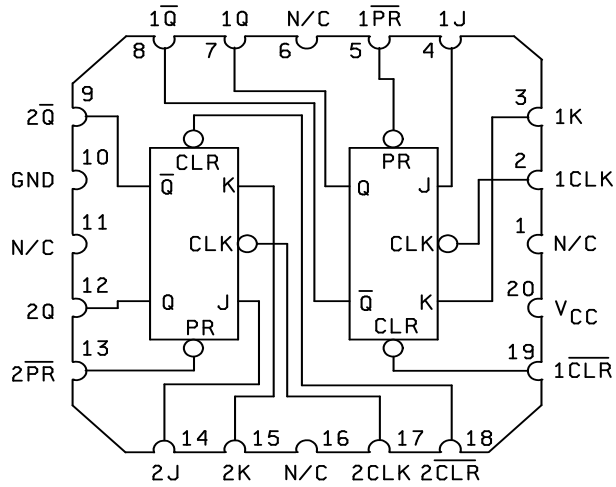


FIGURE 1. Terminal connections (top view). - Continued.

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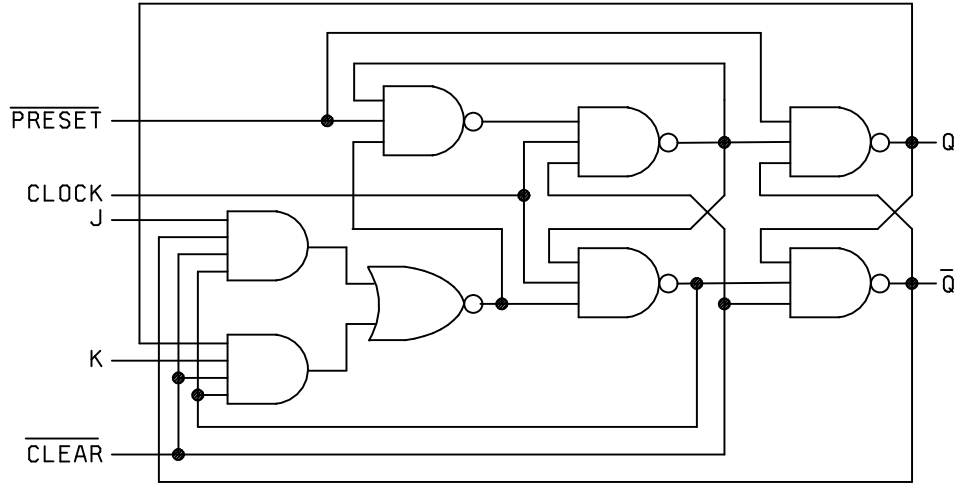
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DEVICE TYPE 01



DEVICE TYPE 02

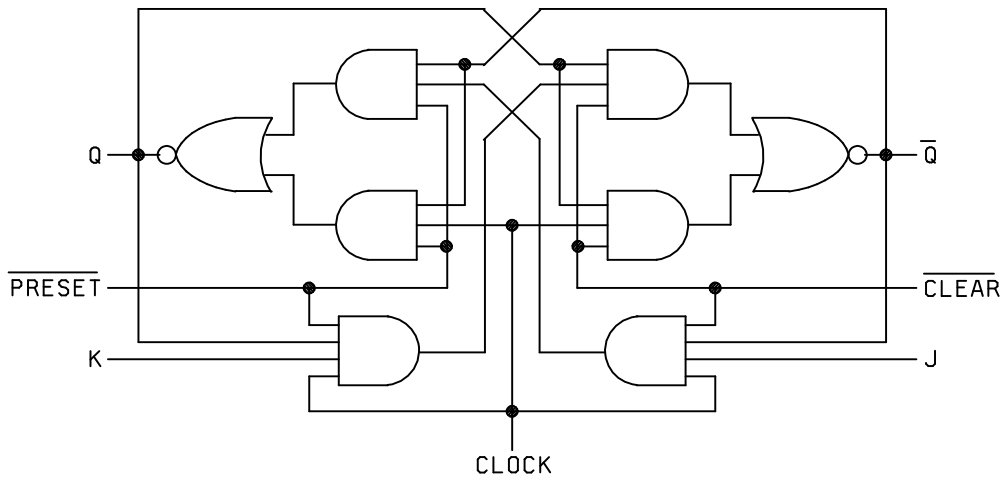


FIGURE 2. Logic diagrams.

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Device type 01

INPUTS					OUTPUTS	
$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	CLOCK	J	\overline{K}	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q _o	\overline{Q}_o
H	H	↑	H	H	H	L
H	H	L	X	X	Q _o	\overline{Q}_o

H = High level (steady state)

L = Low level (steady state)

X = Irrelevant

↑ = Transition from low to high level

Q_o = The level of Q before the indicated steady state input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↑ clock transition.

* This configuration is nonstable; that is it will not persist when preset and clear inputs return to their inactive (high) level.

Device type 02

INPUTS					OUTPUTS	
$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	CLOCK	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q _o	\overline{Q}_o
H	H	↓	L	H	L	H
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q _o	\overline{Q}_o

H = High level (steady state)

L = Low level (steady state)

X = Irrelevant

↓ = Transition from high to low level

Q_o = The level of Q before the indicated steady state input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

* This configuration is nonstable; that is it will not persist when preset and clear inputs return to their inactive (high) level.

FIGURE 3. Truth tables.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-09-08

Approved sources of supply for SMD 84000 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification part number
8400001EA	01295	SNJ54ALS109AJ	M38510/37102BEA
8400001FA	<u>3/</u>	SNJ54ALS109AW	M38510/37102BFA
84000012A	01295	SNJ54ALS109AFK	M38510/37102B2A
8400002EA	01295	SNJ54ALS112AJ	M38510/37103BEA
8400002FA	<u>3/</u>	SNJ54ALS112AW	M38510/37103BFA
84000022A	<u>3/</u>	SNJ54ALS112AFK	M38510/37103B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
P.O. Box 660199
Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.