REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert to military drawing format. Case E inactive for new design. Change V_{IL}, t_{PLH1}, t_{PHL1}, and t_{PLH2}. Delete minimum limits from I_{IL} and propagation delays.	86-10-02	M. A. Frye
D	Delete f_{MAX} and t_p clock at +25°C. Change f_{MAX} (-55°C and +125°C). Change table I, I_O (Q and RCO outputs) to I_O (Q outputs) and (CCO outputs, all) to (CCO and RCO outputs, 02). In table I, device type 02, change propagation delay times. Figure 2, device type 01, change RCO:L to RCO:H (last two entries). Figure 2, device type 02. For Q outputs disabled and load, under U/D change the X to an H. Figure 3, change $\overline{ACD}$ to $\overline{RCO}$. Delete footnote 2/ from table I. Editorial changes throughout. Case 2, device 01 is inactive for design.	87-06-10	M. A. Frye
E	Split V_{IL} into temperatures. Add figure 5. Add footnotes to table I. Change propagation delays. Editorial changes throughout. Change in Table II.	88-05-16	M. A. Frye
F	Changes in accordance with NOR 5962-R083-92. Editorial changes throughout. --pn	92-07-06	Monica L. Poelking
G	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	02-07-31	Raymond Monnin
H	Update to reflect latest changes in format and requirements. Correct paragraph in 3.5. Editorial changes throughout. –les	05-07-21	Raymond Monnin
J	Update drawing to current MIL-PRF-38535 requirements. -jt	17-05-26	Charles Saffle

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	J	J	J	J																
SHEET	15	16	17	18																

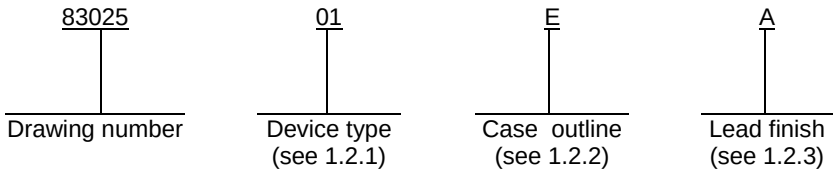
REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Monica L. Poelking	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Raymond Monnin APPROVED BY Michael A. Frye DRAWING APPROVAL DATE 84-03-01 REVISION LEVEL J	MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW-POWER SCHOTTKY TTL, 4-BIT UP/DOWN BINARY COUNTER, MONOLITHIC SILICON SIZE A | CAGE CODE **14933** | **83025** SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS169	Synchronous 4-bit up/down binary counter
02	54ALS569	Synchronous 4-bit up/down binary counter with three-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	flat
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/:	
Device type 01	137.5 mW
Device type 02	176 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit test; e.g., I_O.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL}) :	
V_{IL} = +125°C	0.7 V dc
V_{IL} = +25°C	0.8 V dc
V_{IL} = -55°C	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Width of clock pulse (t_p CLK) :	
Device type 01	20 ns minimum
Device type 02 :	
CLK High	20 ns minimum
CLK Low	23 ns minimum
Width of asynchronous clear pulse (t_p $\overline{\text{ACLR}}$):	
Device type 02	20 ns minimum
Setup times before clock (t_{su}):	
Data:	
Device type 01	20 ns minimum
Device type 02	25 ns minimum
Synchronous clear $\overline{\text{SCLR}}$:	
Device type 02 (low)	20 ns minimum
Device type 02 (inactive)	35 ns minimum
Asynchronous clear ($\overline{\text{ACLR}}$):	
Device type 02 (inactive)	10 ns minimum
Synchronous $\overline{\text{LOAD}}$:	
Device types 01, 02 (low)	20 ns minimum
Device type 02 (inactive)	35 ns minimum
$\overline{\text{ENP}}$ / $\overline{\text{ENT}}$:	
Device types 01 and 02 (low)	25 ns minimum
Device 01 (high)	25 ns minimum
Device type 02 (high)	35 ns minimum
U/$\overline{\text{D}}$:	
Device type 01	28 ns minimum
Device type 02	35 ns minimum
Hold time (t_h):	
Device types 01, 02	0 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Counting sequences. The counting sequences shall be as specified on figure 3.

3.2.5 Logic diagrams. The logic diagrams shall be as specified on figure 4.

3.2.6 Test circuits and switching waveforms. The test circuits and switching waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH1}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} at: -55°C = 0.8 V, +25°C = 0.8 V, +125°C = 0.7 V	I_{OH} = -0.4 mA All outputs 2/	1, 2, 3	01	2.5		V
			$\overline{RCO}$ and $\overline{CCO}$		02	2.5		V
	V_{OH2}		I_{OH} = -1.0 mA Q outputs	1, 2, 3	02	2.4		V
Low level output voltage	V_{OL1}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} at: -55°C = 0.8 V, +25°C = 0.8 V, +125°C = 0.7 V	I_{OL} = 4.0 mA All outputs 2/	1, 2, 3	01		0.4	V
			I_{OL} = 4.0 mA $\overline{RCO}$ and $\overline{CCO}$		02		0.4	V
	V_{OL2}		I_{OL} = 12 mA Q outputs	1, 2, 3	02		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3	All		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V, Unused inputs = 4.5 V		1, 2, 3	All		-0.2	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V, Unused inputs = 0.0 V		1, 2, 3	All		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V, Unused inputs = 0.0 V		1, 2, 3	All		0.1	mA
Output current	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V, 3/	Q outputs	1, 2, 3	All	-20	-112	mA
			$\overline{RCO}$ and $\overline{CCO}$ outputs		02	-15	-70	mA
Off-state output current	I_{OZL}	V_{CC} = 5.5 V, V_{OUT} = 0.4 V,	Q outputs	1, 2, 3	02		-20	µA
	I_{OZH}	V_{CC} = 5.5 V, V_{OUT} = 2.7 V,	Q outputs	1, 2, 3	02		20	µA
Supply current	I_{CC}	V_{CC} = 5.5 V		1, 2, 3	01		25	mA
Supply current	I_{CCH}			1, 2, 3	02		26	mA
	I_{CCL}				02		32	
	I_{CCZ}				02		32	
Functional tests		See 4.3.1c 4/		7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Maximum clock frequency	f_{MAX}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500Ω See figures 4 and 5 5/	9, 10, 11	01	25		MHz
				02	22		
Propagation delay time, CLK to Q	t_{PLH1}		9, 10, 11	01	2	15	ns
				02	4	21	
	t_{PHL1}		9, 10, 11	01	5	20	ns
				02	7	19	
Propagation delay time, CLK to $\overline{RCO}$	t_{PLH2}		9, 10, 11	01	3	20	ns
				02	12	37	
	t_{PHL2}		9, 10, 11	01	6	21	ns
				02	10	28	
Propagation delay time, CLK to $\overline{CCO}$	t_{PLH3}		9, 10, 11	02	5	17	ns
	t_{PHL3}		9, 10, 11	02	6	30	ns
Propagation delay time, $\overline{ENT}$ to $\overline{RCO}$	t_{PLH4}		9, 10, 11	01	2	14	ns
				02	6	21	
	t_{PHL4}		9, 10, 11	01	3	24	ns
				02	4	20	
Propagation delay time, $\overline{ENT}$ to $\overline{CCO}$	t_{PLH5}		9, 10, 11	02	5	18	ns
	t_{PHL5}		9, 10, 11	02	9	32	ns
Propagation delay time, $\overline{ENP}$ to $\overline{CCO}$	t_{PLH6}		9, 10, 11	02	4	18	ns
	t_{PHL6}		9, 10, 11	02	5	18	ns
Propagation delay time, U/$\overline{D}$ to $\overline{RCO}$	t_{PLH7}		9, 10, 11	01	4	21	ns
				02	9	31	
	t_{PHL7}		9, 10, 11	01	5	26	ns
				02	9	33	
Propagation delay time, $\overline{ACLR}$ to Q	t_{PHL8}		9, 10, 11	02	9	25	ns
Enable time, $\overline{G}$ to Q	t_{PZH}		9, 10, 11	02	6	23	ns
	t_{PZL}				6	29	
Disable time, $\overline{G}$ to Q	t_{PHZ}		9, 10, 11	02	1	12	ns
	t_{PLZ}				3	29	

1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V or ≤ 0.4 V. No unused input shall exceed 5.5 V or go less than 0.0 V. No input shall be floated.

2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or the V_{IH} minimum input.

3/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.

4/ Functional tests shall be conducted at input test conditions of $GND \le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

5/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

Device types	01	01	02	02
Case outlines	E, F	2	R, S	2
Terminal number	Terminal symbols		Terminal symbols	
1	$U/\overline{D}$	NC	$U/\overline{D}$	$U/\overline{D}$
2	CLK	$U/\overline{D}$	CLK	CLK
3	A	CLK	A	A
4	B	A	B	B
5	C	B	C	C
6	D	NC	D	D
7	$\overline{ENP}$	C	$\overline{ENP}$	$\overline{ENP}$
8	GND	D	$\overline{ACLR}$	$\overline{ACLR}$
9	$\overline{LOAD}$	$\overline{ENP}$	$\overline{SCLR}$	$\overline{SCLR}$
10	$\overline{ENT}$	GND	GND	GND
11	Q_D	NC	$\overline{SLOAD}$	$\overline{SLOAD}$
12	Q_C	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENT}$
13	Q_B	$\overline{ENT}$	Q_D	Q_D
14	Q_A	Q_D	Q_C	Q_C
15	$\overline{RCO}$	Q_C	Q_B	Q_B
16	V_{CC}	NC	Q_A	Q_A
17	- - -	Q_B	$\overline{G}$	$\overline{G}$
18	- - -	Q_A	$\overline{CCO}$	$\overline{CCO}$
19	- - -	$\overline{RCO}$	$\overline{RCO}$	$\overline{RCO}$
20	- - -	V_{CC}	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Device type 01

Operation	Inputs at time t_n									Outputs at time t_{n+1}				
	CLK	$\overline{ENP}$	$\overline{ENT}$	$\overline{LOAD}$	A	B	C	D	U/$\overline{D}$	Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$
Load	↑	L	L	L	X	X	X	X	X	A	B	C	D	L if count = 15 H if count ≠ 15
count up	↑	L	L	H	X	X	X	X	H	Previous count plus 1				L if count = 15 H if count ≠ 15
count down	↑	L	L	H	X	X	X	X	L	Previous count minus 1				L if count = 0 H if count ≠ 0
Inhibit	↑	H	L	H	X	X	X	X	X	No change				No change
	↑	L	H	H	X	X	X	X	X					H
	↑	H	H	H	X	X	X	X	X					H

Device type 01

Count up sequence				
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	L

Count down sequence				
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$
H	H	H	H	H
H	H	H	L	H
H	H	L	H	H
H	H	L	L	H
H	L	H	H	H
H	L	H	L	H
H	L	L	H	H
H	L	L	L	H
L	H	H	H	H
L	H	H	L	H
L	H	L	H	H
L	H	L	L	H
L	L	H	H	H
L	L	H	L	H
L	L	L	H	H
L	L	L	L	L

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level

FIGURE 2. Truth tables.

Device type 02

Operation	Inputs at time t_n								Outputs at time t_{n+1}									
	$\overline{G}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	$U/\overline{D}$	CLK	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$	$\overline{CCO}$
Q outputs disabled	H	X	X	X	X	X	H	X	X	X	X	X	Z	Z	Z	Z	L if count ≠ 15 H if count = 15	1/
Asynchronous clear	L	L	X	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
Synchronous clear	L	H	L	X	X	X	X	↑	X	X	X	X	L	L	L	L	H	H
Load	L	H	H	L	X	X	H	↑	X	X	X	X	A	B	C	D	L if count = 15 H if count ≠ 15	1/
Count up	L	H	H	H	L	L	H	↑	X	X	X	X	Previous count plus 1				L if count = 15 H if count ≠ 15	1/
Count down	L	H	H	H	L	L	L	↑	X	X	X	X	Previous count minus 1				L if count = 0 H if count ≠ 0	1/
Inhibit count	L	H	H	H	X	H	X	X	X	X	X	X	No change (hold)				2/	1/
	L	H	H	H	H	X	X	X	X	X	X	X						
	L	H	H	H	H	H	X	X	X	X	X	X						

Device type 02

Count up sequence					
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$	$\overline{CCO}$
L	L	L	L	H	H
L	L	L	H	H	H
L	L	H	L	H	H
L	L	H	H	H	H
L	H	L	L	H	H
L	H	L	H	H	H
L	H	H	L	H	H
L	H	H	H	H	H
H	L	L	L	H	H
H	L	L	H	H	H
H	L	H	L	H	H
H	L	H	H	H	H
H	H	L	L	H	H
H	H	L	H	H	H
H	H	H	L	H	H
H	H	H	H	L	1/

Count down sequence					
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$	$\overline{CCO}$
H	H	H	H	H	H
H	H	H	L	H	H
H	H	L	H	H	H
H	H	L	L	H	H
H	L	H	H	H	H
H	L	H	L	H	H
H	L	L	H	H	H
H	L	L	L	H	H
L	H	H	H	H	H
L	H	H	L	H	H
L	H	L	H	H	H
L	H	L	L	H	H
L	L	H	H	H	H
L	L	H	L	H	H
L	L	L	H	H	H
L	L	L	L	L	1/

H = High level
L = Low level
Z = Disabled (High impedance state)
X = Irrelevant
↑ = Transition from low to high level

1/ $\overline{CCO}$ produces a low level pulse for the duration equal to that of the low level of the clock when $\overline{RCO}$ is low and the counter is enabled, otherwise $\overline{CCO}$ is high.

2/ $\overline{RCO}$ produces a low level pulse while the count is 15 when counting up, or while the count is 0 when counting down.

FIGURE 2. Truth tables - Continued.

Device type 01

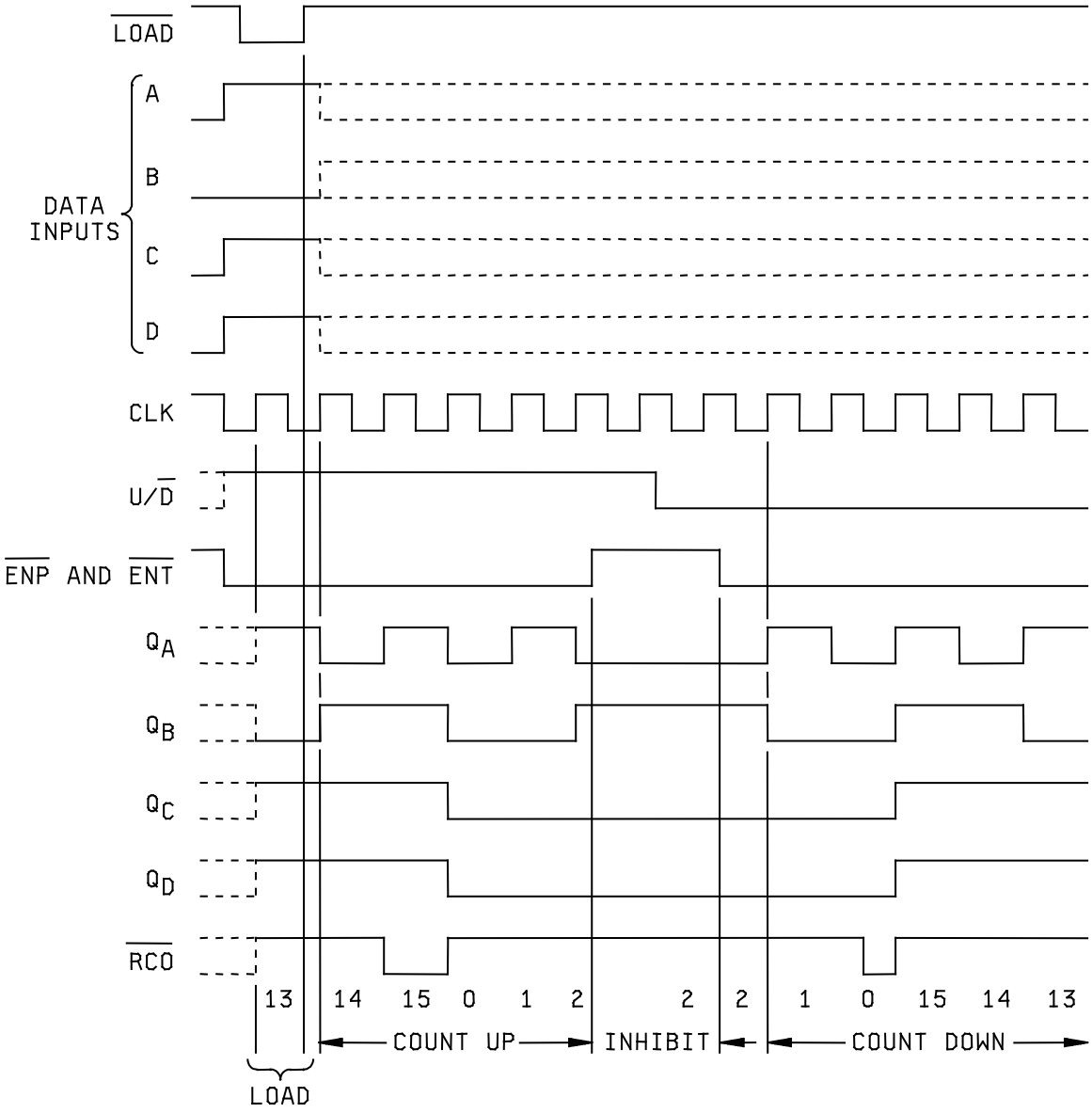


FIGURE 3. Counting sequences.

Device type 02

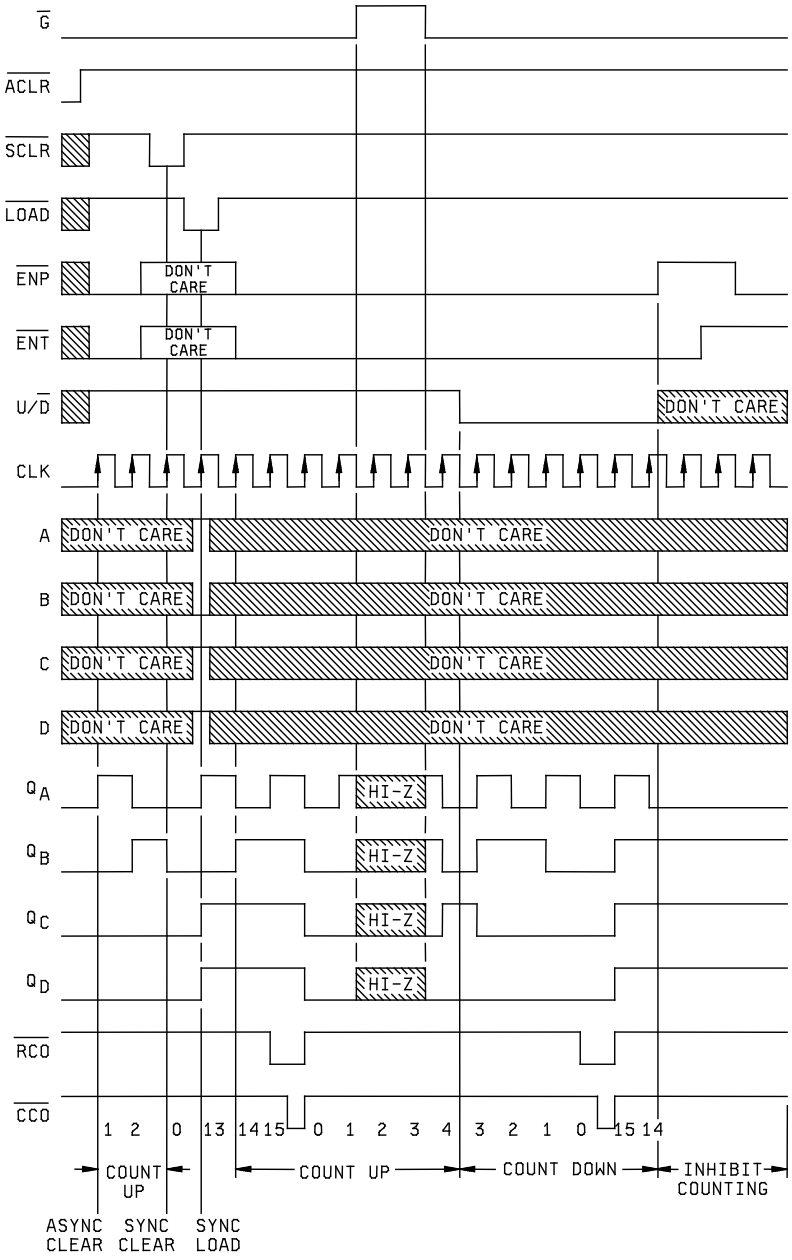


FIGURE 3. Counting sequences - Continued.

Device type 01

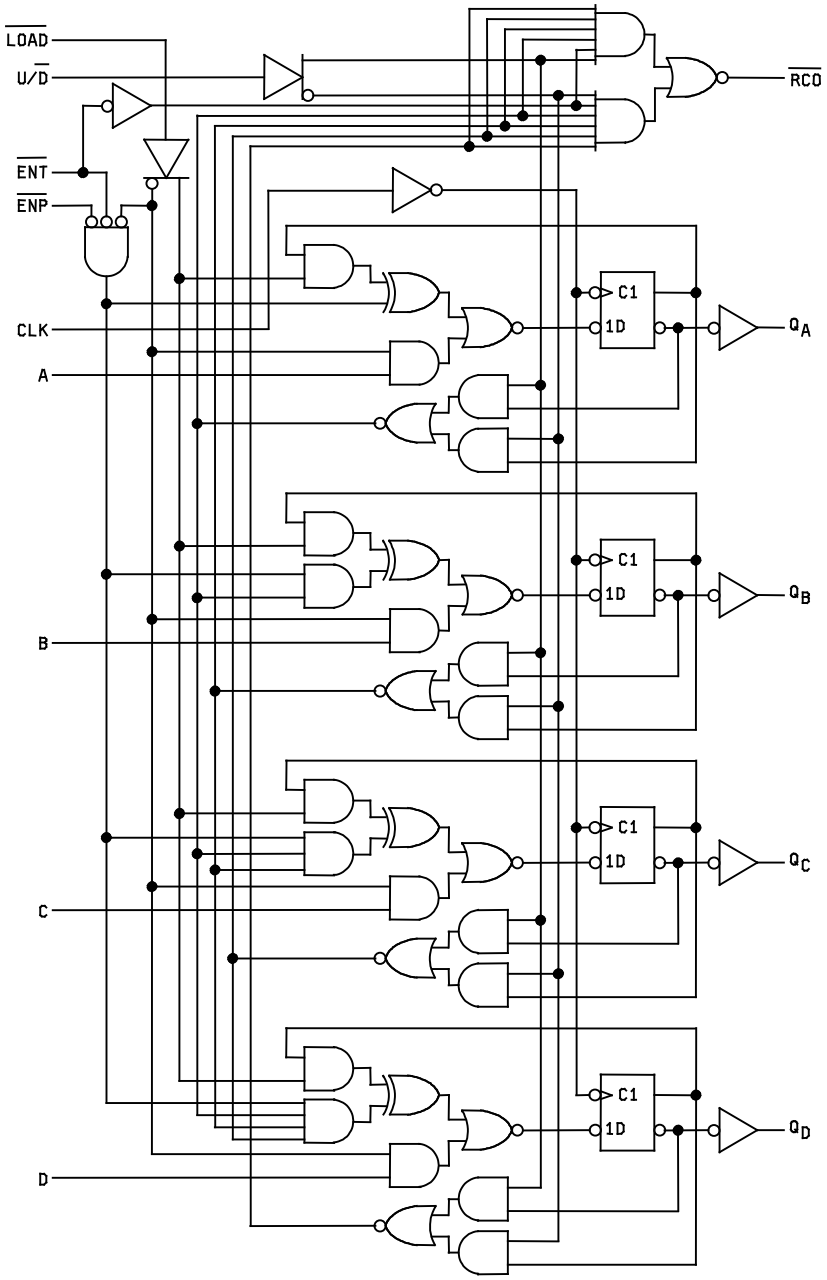


FIGURE 4. Logic diagrams.

Device type 02

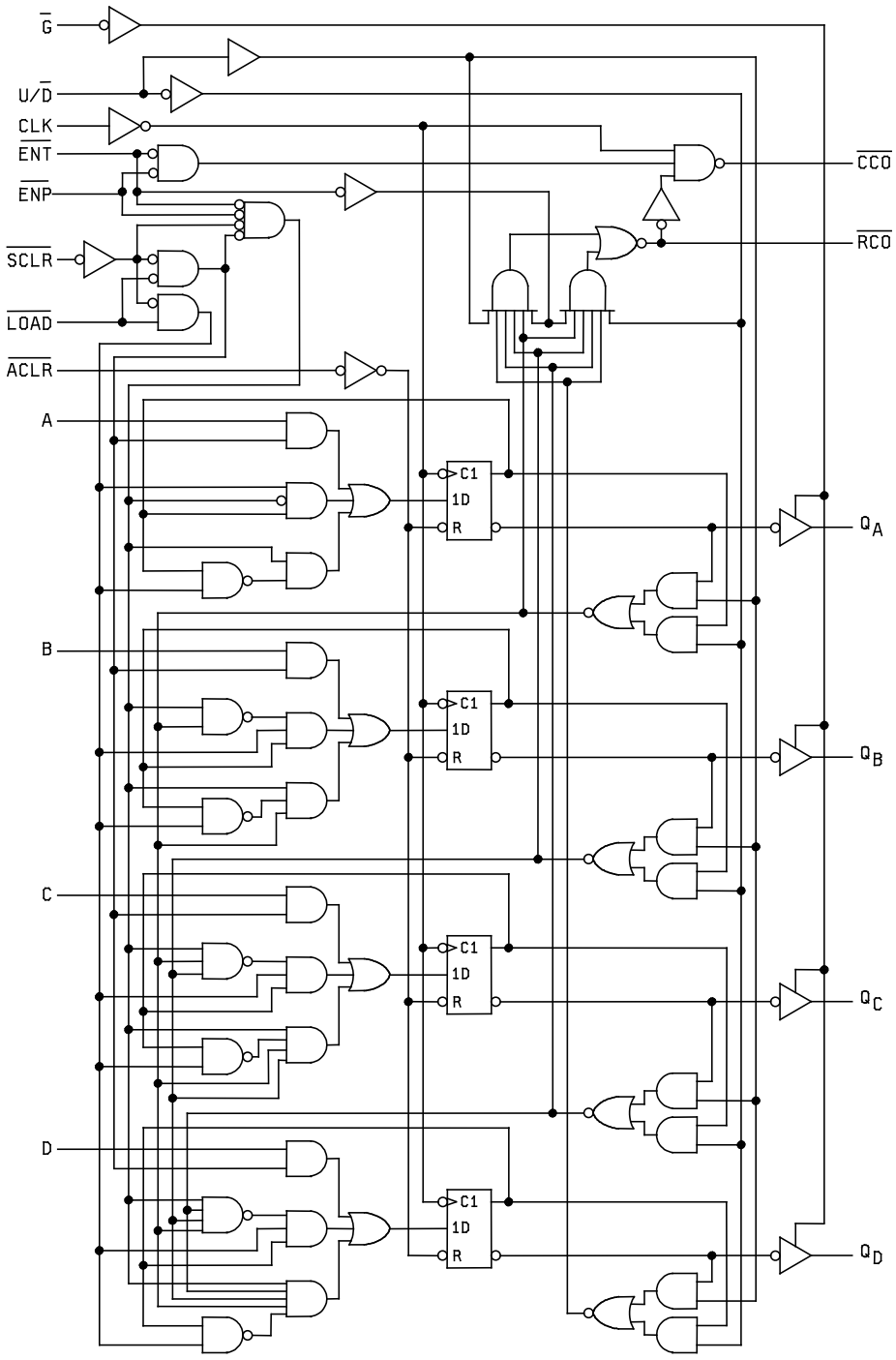


FIGURE 4. Logic diagrams - Continued.

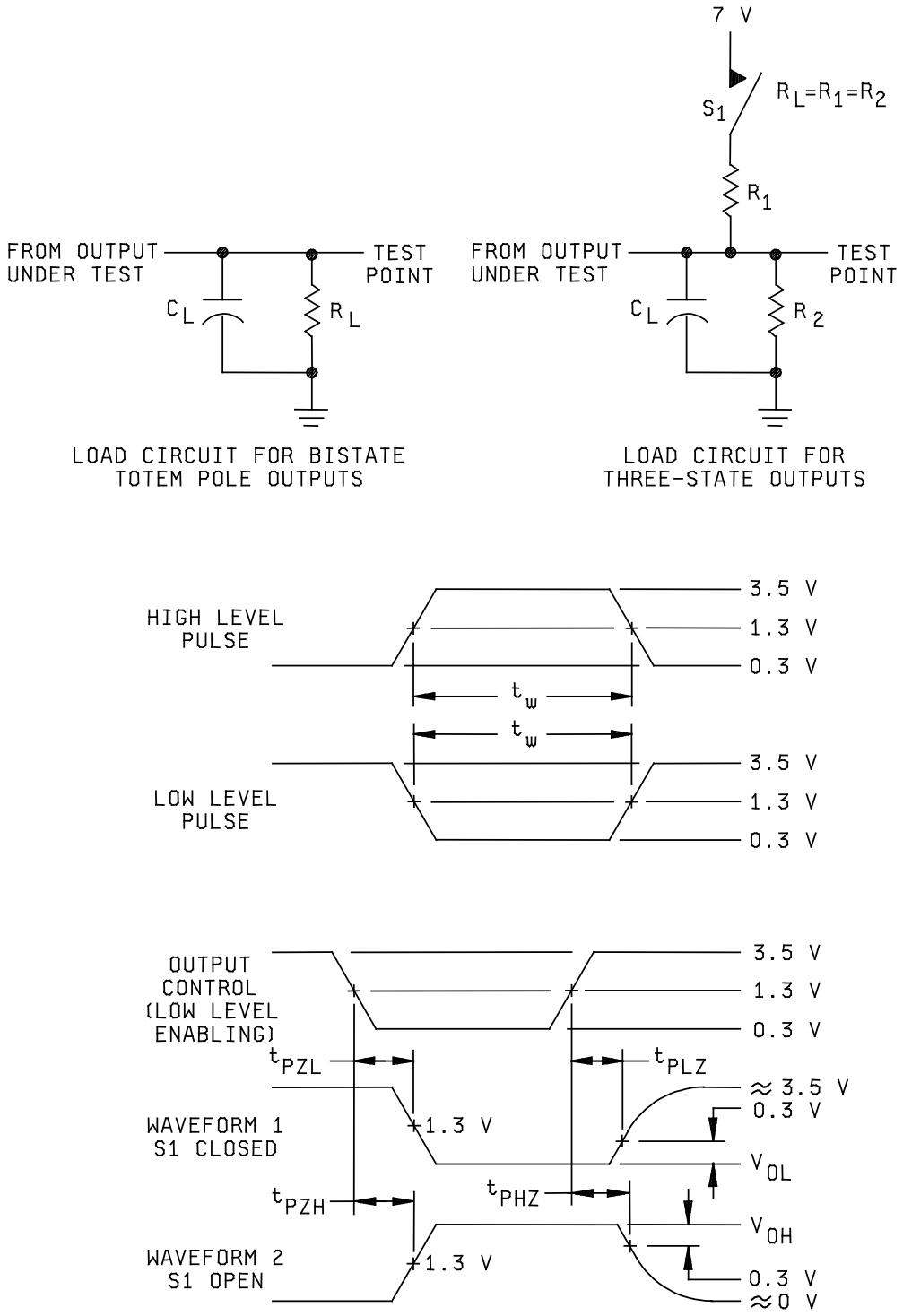
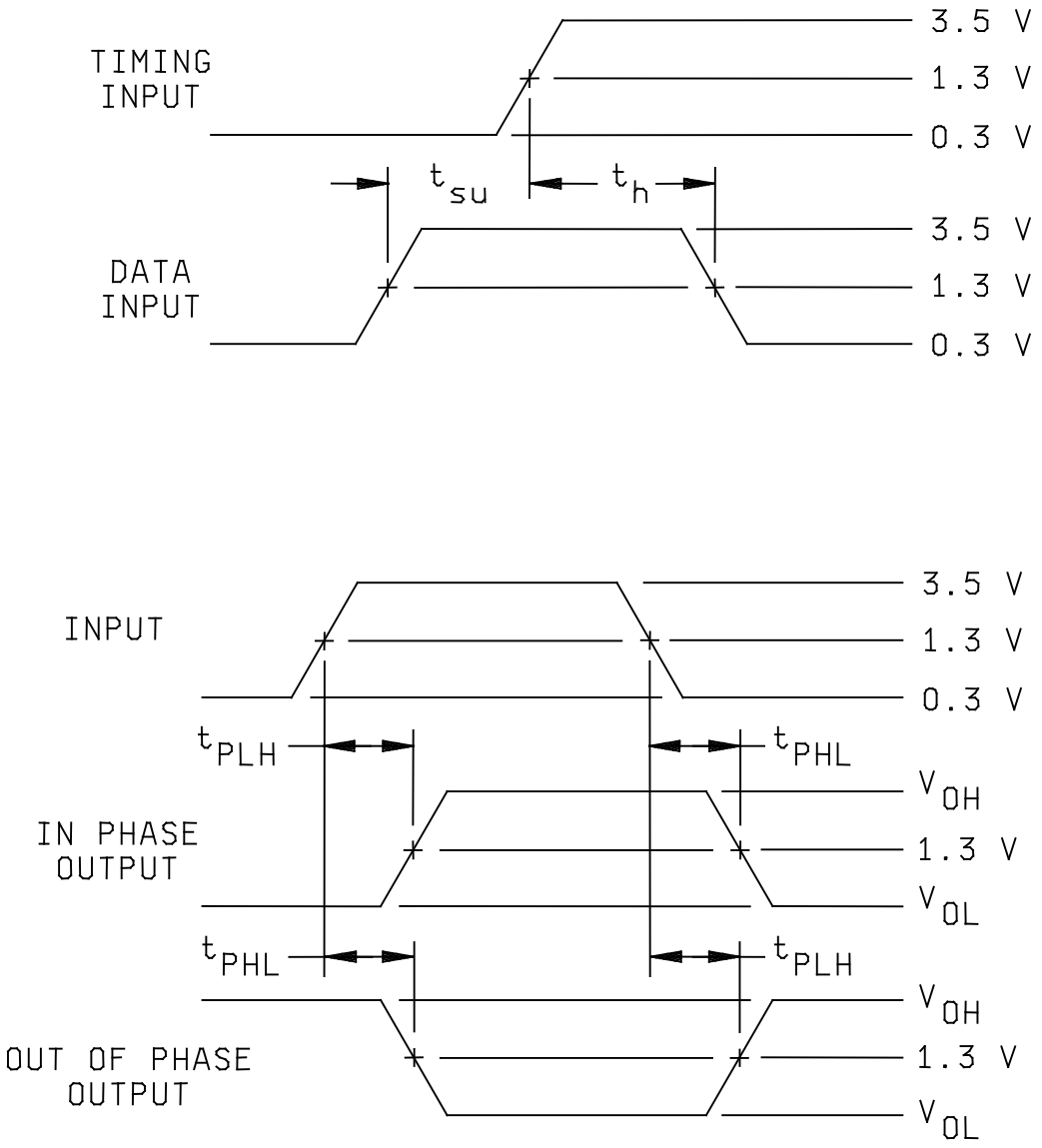


FIGURE 5. Test circuits and switching waveforms.



PROPAGATION DELAY TIMES

NOTES:
1. C_L includes probe and jig capacitance.
2. All inputs have the following characteristics: PRR ≤ 10 MHz, duty cycle = 50 percent, $t_r = t_f$ = 3 ns ±1 ns.
3. The outputs are measured one at a time with one input transition per measurement.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. When measuring propagation delay times of three-state outputs, switch S1 is open.

FIGURE 5. Test circuits and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-05-26

Approved sources of supply for SMD 83025 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
8302501EA	01295 3/	SNJ54ALS169BJ 54ALS169BJ/883	M38510/38003BEA
8302501FA	01295 3/	SNJ54ALS169BW 54ALS169BW/883	M38510/38003BFA
83025012A	3/ 3/	SNJ54ALS169BFK 54ALS169BFK/883	M38510/38003B2A
8302502RA	01295	SNJ54ALS569AJ	M38510/38005BRA
8302502SA	3/	SNJ54ALS569AW	M38510/38005BSA
83025022A	01295	SNJ54ALS569AFK	M38510/38005B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243