REVISIONS			
C	Change V_{IL}, tp(clock), f_{MAX}, and propagation delay limits. Delete minimum limits from I_{IL} and propagation delays. Convert to military drawing format. Case E inactive for new design.	87-03-03	D. Cool
D	Change drawing CAGE number to 67268, Change I_{IL} condition. Change t_{PLH2}. Correct vendor p/n. Case 2, device types 01 and 02 are inactive.	87-12-01	D. Cool
E	Change clock pulse and setup times. Split V_{IL} into temperatures. Change propagation delays. Add footnotes to table I. Change footnote 1/ in 1.3 Add figure 5. Editorial changes throughout. Delete CAGE number 04713. Add CAGE numbers 18324 and 27014. Change in t_p CLK, t_s (device 03), I_{IH}, I_{CC}, f_{MAX}, and figure 2. Change in table II.	88-05-28	D. Cool
F	Technical change in table I, t_{pLZ}, device 03. Added clarification to voltage waveforms. Added a source to device type 03. Editorial changes throughout.	89-10-17	W. Heckman
G	Technical change in table I, I_0. Change to the truth table in figure 2. Clarify the note in figure 2. Editorial changes throughout.	92-07-16	Monica L. Poelking
H	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	02-07-25	Raymond Monnin
J	Update to reflect latest changes in format and requirements. Correct paragraph in 3.5. Editorial changes throughout. –les	05-07-21	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	J	J	J	J	J	J														
SHEET	15	16	17	18	19	20														

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY

Monica L. Poelking

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

David H. Johnson

APPROVED BY

D. Cool

DRAWING APPROVAL DATE

84-04-30

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW-POWER SCHOTTKY TTL, COUNTERS, MONOLITHIC SILICON

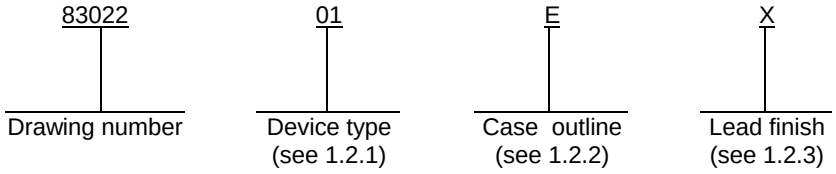
REVISION LEVEL	SIZE	CAGE CODE	
J	A	**14933**	**83022**

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS161	Synchronous 4-bit binary counter with asynchronous clear
02	54ALS163	Synchronous 4-bit binary counter with synchronous clear
03	54ALS561	Synchronous 4-bit binary counter with three-state outputs

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	flat
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/:	
Device type 01	115.5 mW
Device type 02	137.5 mW
Device type 03	209 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit test; e.g., I_O.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL}) :	
V_{IL} = +125°C	0.7 V dc
V_{IL} = +25°C	0.8 V dc
V_{IL} = -55°C	0.8 V dc
Width of clock pulse (t_p CLK) :	
Device types 01 and 02	20 ns minimum
Device type 03 :	
High	20 ns minimum
Low	25 ns minimum
Width of asynchronous clear pulse (t_p $\overline{\text{ACLR}}$), t_p $\overline{\text{CLR}}$:	
Device types 01, and 03	20 ns minimum
Width of asynchronous load pulse (t_p $\overline{\text{ALOAD}}$):	
Device type 03	20 ns minimum
Setup times before clock:	
Data:	
Device types 01 and 02	20 ns minimum
Device type 03	25 ns minimum
Synchronous $\overline{\text{CLR}}$; $\overline{\text{SCLR}}$	
Low:	
Device type 02	20 ns minimum
Device type 03	21 ns minimum
Inactive:	
Device type 02	20 ns minimum
Device type 03	35 ns minimum
Asynchronous $\overline{\text{CLR}}$, $\overline{\text{ACLR}}$	
Inactive:	
Device types 01 and 03	10 ns minimum
Asynchronous $\overline{\text{ALOAD}}$:	
Inactive:	
Device type 03	12 ns minimum
Synchronous $\overline{\text{LOAD}}$:	
Device types 01 and 02	20 ns minimum
Low:	
Device type 03	20 ns minimum
Inactive:	
Device type 03	35 ns minimum
ENP/ENT:	
Low:	
Device types 01 and 03	25 ns minimum
Device type 02	20 ns minimum
High:	
Device types 01 and 03	25 ns minimum
Hold times (t_h):	
Device types 01, 02, and 03	0 ns minimum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Counting sequences. The counting sequences shall be as specified on figure 4.

3.2.6 Test circuits and switching waveforms. The test circuits and switching waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH1}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} at: -55°C = 0.8 V +25°C = 0.8 V +125°C = 0.7 V	I_{OH} = -0.4 mA 2/	1, 2, 3	01, 02	2.5		V
			I_{OH} = -0.4 mA RCO and CCO		03	2.5		V
	V_{OH2}		I_{OH} = -1.0 mA Q outputs		03	2.4		V
Low level output voltage	V_{OL1}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} at: -55°C = 0.8 V +25°C = 0.8 V +125°C = 0.7 V	I_{OL} = 4.0 mA All outputs 2/		01, 02		0.4	V
			I_{OL} = 4.0 mA RCO and CCO		03		0.4	V
	V_{OL2}		I_{OL} = 12 mA Q outputs		03		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA			All		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V, unused inputs = 4.5 V			All		-0.2	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V, unused inputs = 0.0 V	$\overline{LOAD}$, CLK, ENT		01, 02		20	µA
			ENT/ENP		03		40	µA
			All other inputs		All		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V, unused inputs = 0.0 V	$\overline{LOAD}$, CLK, ENT		01, 02		0.1	mA
			ENT/ENP		03		0.2	mA
			All other inputs		All		0.1	mA
Output current	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V, 3/	Q outputs		All	-20	-112	mA
			RCO and CCO outputs		03	-15	-100	mA
Off-state output current	I_{OZL}	V_{CC} = 5.5 V, V_{OUT} = 0.4 V,	Q outputs		03		-20	µA
	I_{OZH}	V_{CC} = 5.5 V, V_{OUT} = 2.7 V,			03		20	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	01		21	mA
				02		25	
	I_{CCH}			03		35	mA
	I_{CCL}					38	
	I_{CCZ}					36	
Functional tests		See 4.3.1c 4/	7, 8	All			
Maximum input clock or count up frequency	f_{MAX}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500Ω	9, 10, 11	01	25		MHz
				02	35		
				03	20		
Propagation delay time, CLK to Q	t_{PLH1}	See figures 4 and 5 5/		01	4	15	ns
				02	4	21	
				03	4	15	
	t_{PHL1}			01	6	20	ns
				02	6	25	
				03	5	21	
Propagation delay time, CLK to RCO	t_{PLH2}			01	5	24	ns
				02, 03	5	35	
	t_{PHL2}			01	5	20	ns
				02	5	26	
				03	8	29	
Propagation delay time, CLK to CCO	t_{PLH3}			03	8	35	ns
	t_{PHL3}			03	5	20	
Propagation delay time, $\overline{ALOAD}$ to Q	t_{PLH4}			03	10	38	ns
	t_{PHL4}			03	7	27	
Propagation delay time, $\overline{ALOAD}$ to RCO	t_{PLH5}			03	15	55	ns
	t_{PHL5}			03	12	35	
Propagation delay time, $\overline{ALOAD}$ to CCO	t_{PLH6}			03	25	65	ns
	t_{PHL6}			03	12	42	
Propagation delay time, DATA to Q	t_{PLH7}			03	8	35	ns
	t_{PHL7}			03	7	29	
Propagation delay time, ENT to RCO	t_{PLH8}			01	3	13	ns
				02	3	20	
				03	5	20	
	t_{PHL8}			01	3	13	ns
				02	3	16	
				03	4	18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, ENT to CCO	t_{PLH9}	V_{CC} = 4.5 V to 5.5 V	9, 10, 11	03	12	35	ns
	t_{PHL9}	C_L = 50 pF		03	4	25	
Propagation delay time, ENP to CCO	t_{PLH10}	R_L = 500Ω		03	5	22	ns
	t_{PHL10}	See figures 4 and 5 5/		03	4	14	
Propagation delay time, $\overline{CLR}$ to Q	t_{PHL11}			01	8	24	ns
				03	7	28	
Propagation delay time, $\overline{CLR}$ to RCO	t_{PHL12}			01	11	24.5	ns
Output enable time, $\overline{G}$ to Q	t_{PZH}			03	5	24	ns
	t_{PZL}			03	8	28	
Output disable time, $\overline{G}$ to Q	t_{PHZ}			03	2	15	ns
	t_{PLZ}			03	2	20	

1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V or ≤ 0.4 V. No unused input shall exceed 5.5 V or go less than 0.0 V. No input shall be floated.

2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or the V_{IH} minimum input.

3/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.

4 Functional tests shall be conducted at input test conditions of $GND \le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

5/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

Device types	01, 02	01, 02	03	03
Case outlines	E, F	2	R, S	2
Terminal number	Terminal symbols		Terminal symbols	
1	$\overline{CLR}$	NC	$\overline{ALOAD}$	$\overline{ALOAD}$
2	CLK	$\overline{CLR}$	CLK	CLK
3	A	CLK	A	A
4	B	A	B	B
5	C	B	C	C
6	D	NC	D	D
7	ENP	C	ENP	ENP
8	GND	D	$\overline{ACLR}$	$\overline{ACLR}$
9	$\overline{LOAD}$	ENP	$\overline{SCLR}$	$\overline{SCLR}$
10	ENT	GND	GND	GND
11	Q_D	NC	$\overline{SLOAD}$	$\overline{SLOAD}$
12	Q_C	$\overline{LOAD}$	ENT	ENT
13	Q_B	ENT	Q_D	Q_D
14	Q_A	Q_D	Q_C	Q_C
15	RCO	Q_C	Q_B	Q_B
16	V_{CC}	NC	Q_A	Q_A
17	- - -	Q_B	$\overline{G}$	$\overline{G}$
18	- - -	Q_A	CCO	CCO
19	- - -	RCO	RCO	RCO
20	- - -	V_{CC}	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Device types 01 and 02

Synchronous truth table

Inputs at time t_n									Outputs at time t_{n+1}				
CLK	ENP	ENT	$\overline{LOAD}$	A	B	C	D	$\overline{CLR}$	Q_A	Q_B	Q_C	Q_D	RCO
CP	L	X	H	X	X	X	X	H	NC	NC	NC	NC	NC
CP	X	L	H	X	X	X	X	H	NC	NC	NC	NC	L
CP	H	H	H	X	X	X	X	H	Previous count plus 1 See up count sequence table				H if count = 15 L if count < 15
CP	X	H	L	X	X	X	X	H	A	B	C	D	H if count = 15 L if count < 15
CP	X	L	L	X	X	X	X	H	A	B	C	D	L

L = V_{IL} for inputs, V_{OL} for outputs.
H = V_{IH} for inputs, V_{OH} for outputs.
X = V_{IH} or V_{IL}.
CP = Clock pulse.
NC = No change.

FIGURE 2. Truth tables.

Device type 01

Asynchronous truth table (clear function)

Inputs at time t_n									Outputs at time t_{n+1}				
CLK	ENP	ENT	$\overline{\text{LOAD}}$	A	B	C	D	$\overline{\text{CLR}}$	Q_A	Q_B	Q_C	Q_D	RCO
X	X	X	X	X	X	X	X	L	L	L	L	L	L

Device type 02

Synchronous truth table (clear function)

Inputs at time t_n									Outputs at time t_{n+1}				
CLK	ENP	ENT	$\overline{\text{LOAD}}$	A	B	C	D	$\overline{\text{CLR}}$	Q_A	Q_B	Q_C	Q_D	RCO
CP	X	X	X	X	X	X	X	L	L	L	L	L	L

L = V_{IL} for inputs, V_{OL} for outputs.
H = V_{IH} for inputs, V_{OH} for outputs.
X = V_{IH} or V_{IL}.
CP = Clock pulse.
NC = No change.

Device types 01 and 02

Up count sequence table

Q_A (LSB)	Q_B	Q_C	Q_D (MSB)
L	L	L	L
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth tables - Continued.

Device type 03

Operation	$\overline{G}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	A	B	C	D	Q_A	Q_B	Q_C	Q_D	RCO	CCO
Q outputs disabled	H	X	X	X	X	H	X	X	X	X	X	X	Z	Z	Z	Z	H if cnt = 15 L if cnt ≠ 15	See note 2
See note 1	H	H	H	H	H	H	H	H										
Asynchronous clear	L	L	X	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L
Asynchronous load	L	H	L	X	X	H	X	X	X	X	X	X	A	B	C	D	H if cnt = 15 L if cnt ≠ 15	See note 2
Synchronous clear	L	H	H	L	X	X	X	↑	X	X	X	X	L	L	L	L	L	L
Synchronous load	L	H	H	H	L	H	X	↑	X	X	X	X	A	B	C	D	H if cnt = 15 L if cnt ≠ 15	See note 2
Count	L	H	H	H	H	H	H	↑	X	X	X	X	Previous count plus 1				H if cnt = 15 L if cnt ≠ 15	See note 2
Inhibit counting	L	H	H	H	H	H	L	X	X	X	X	X	No change				H if cnt = 15 L if cnt ≠ 15	See note 2
						L	X										L	

Device type 03

Count up sequence					
Q_D	Q_C	Q_B	Q_A	RCO	CCO
L	L	L	L	L	L
L	L	L	H	L	L
L	L	H	L	L	L
L	L	H	H	L	L
L	H	L	L	L	L
L	H	L	H	L	L
L	H	H	L	L	L
L	H	H	H	L	L
H	L	L	L	L	L
H	L	L	H	L	L
H	L	H	L	L	L
H	L	H	H	L	L
H	H	L	L	L	L
H	H	L	H	L	L
H	H	H	L	L	L
H	H	H	H	H	See note 2

NOTES:
1. Counting continues.
2. CCO produces a high level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled, otherwise CCO is low.

FIGURE 2. Truth tables - Continued.

Device type 01

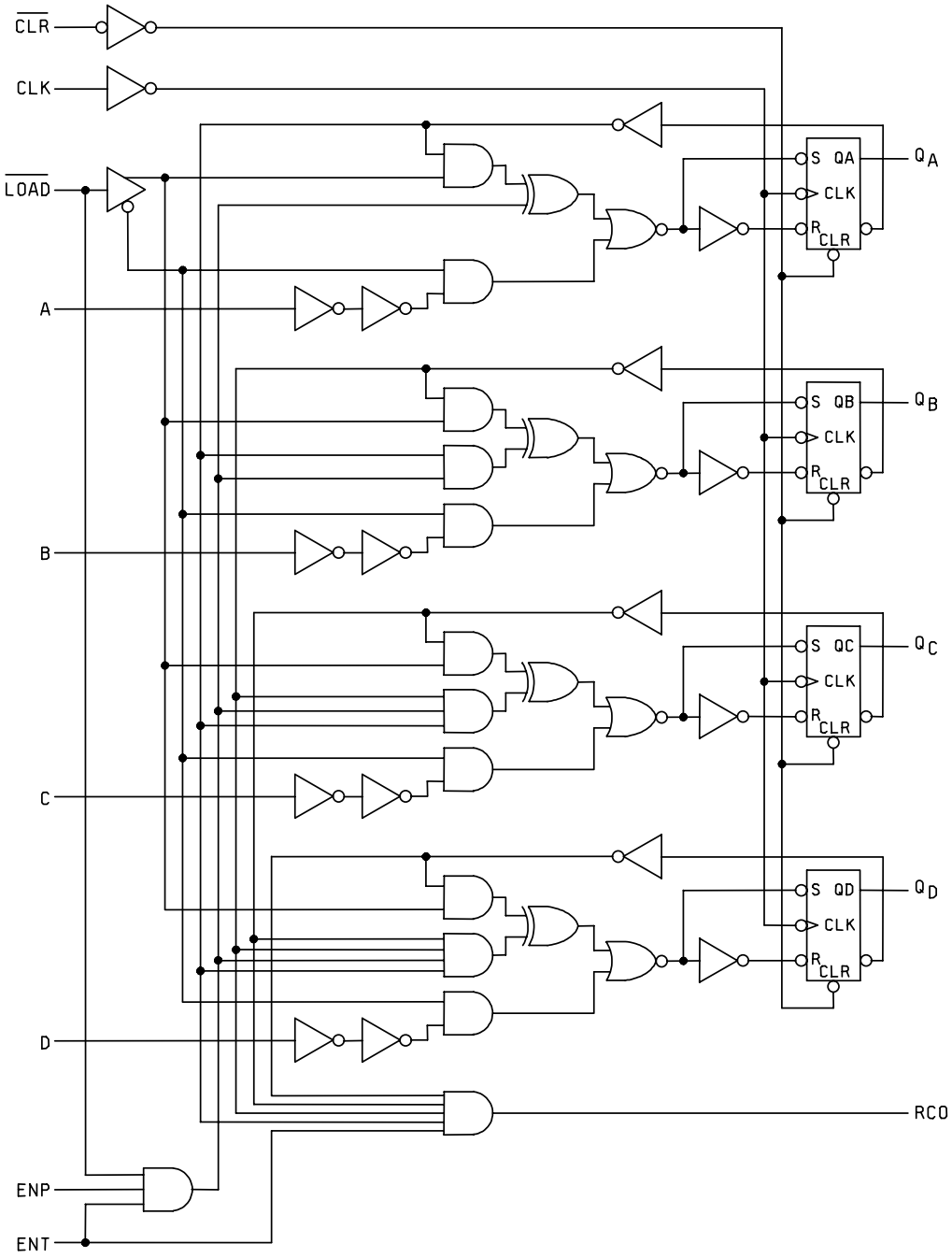


FIGURE 3. Logic diagrams.

Device type 02

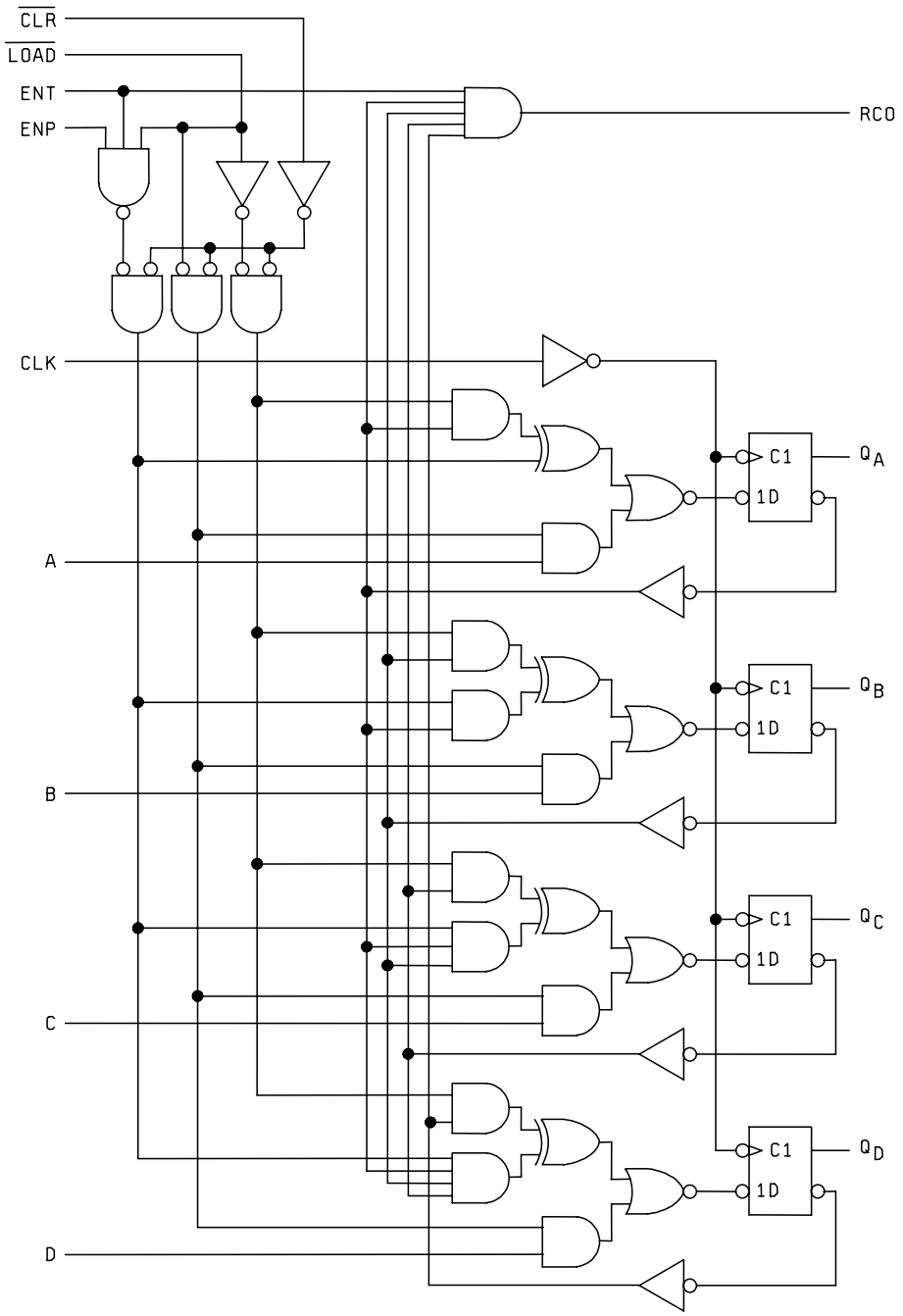


FIGURE 3. Logic diagrams - Continued.

Device type 03

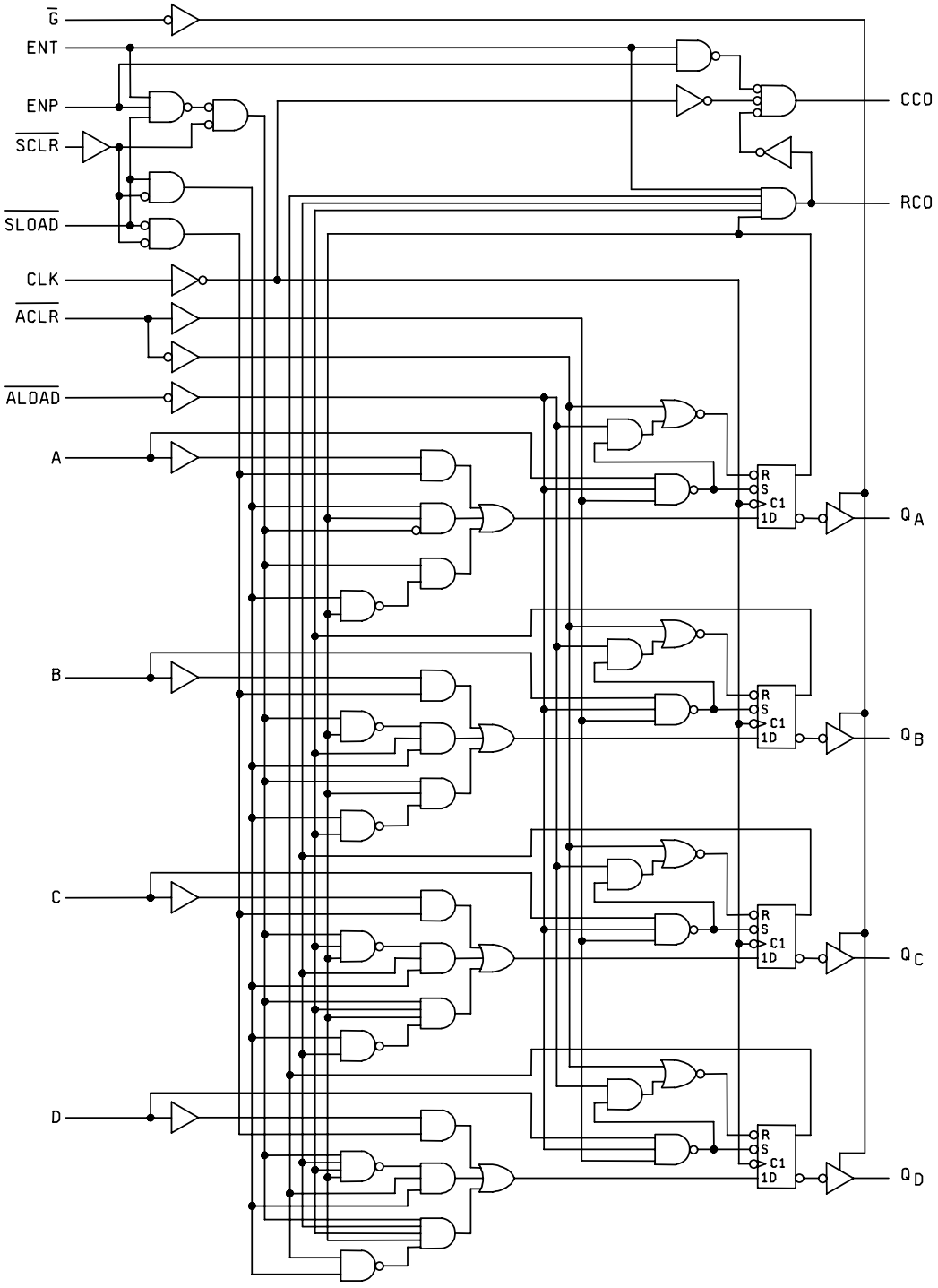


FIGURE 3. Logic diagrams - Continued.

Device types 01 and 02

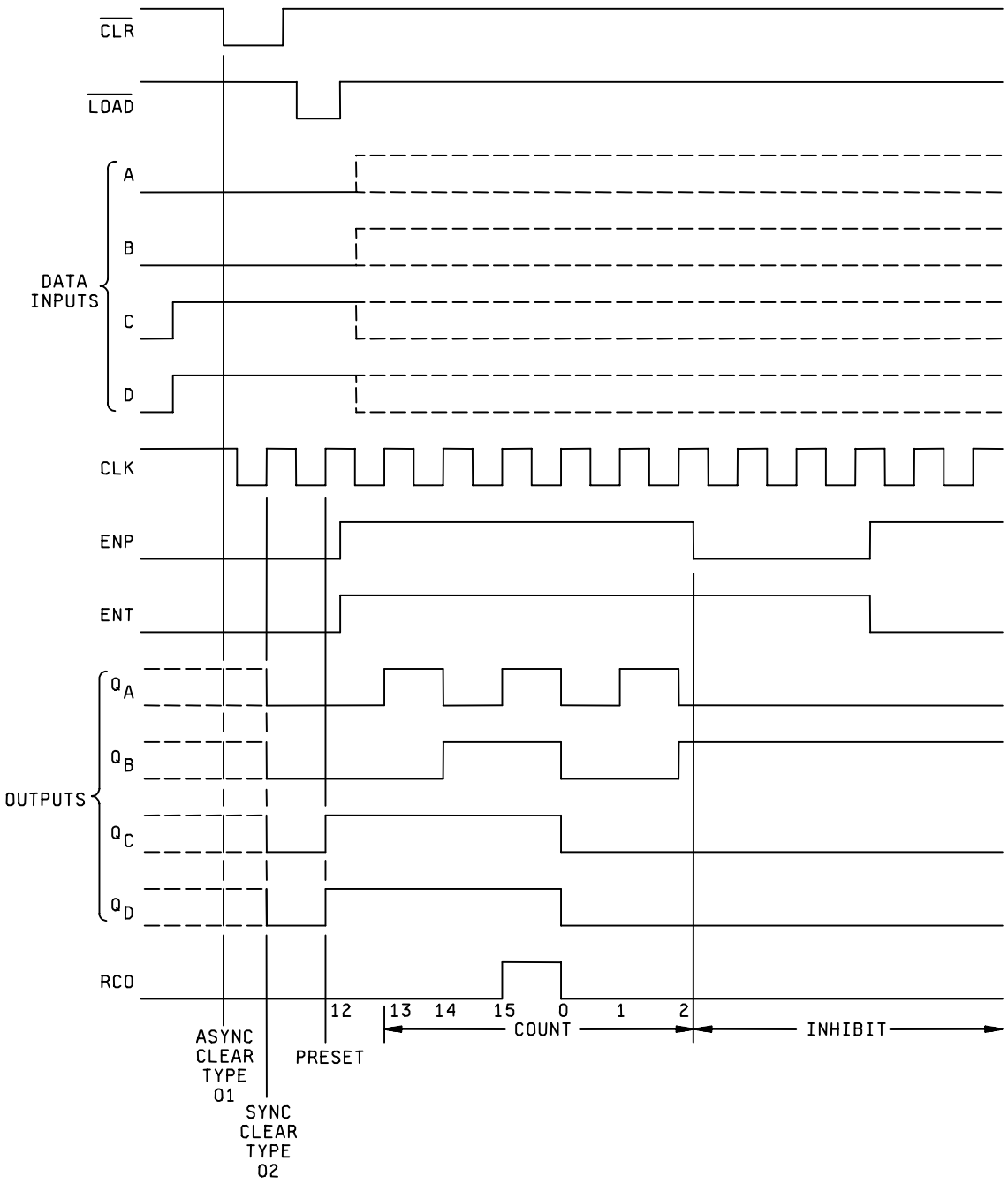


FIGURE 4. Counting sequences.

Device type 03

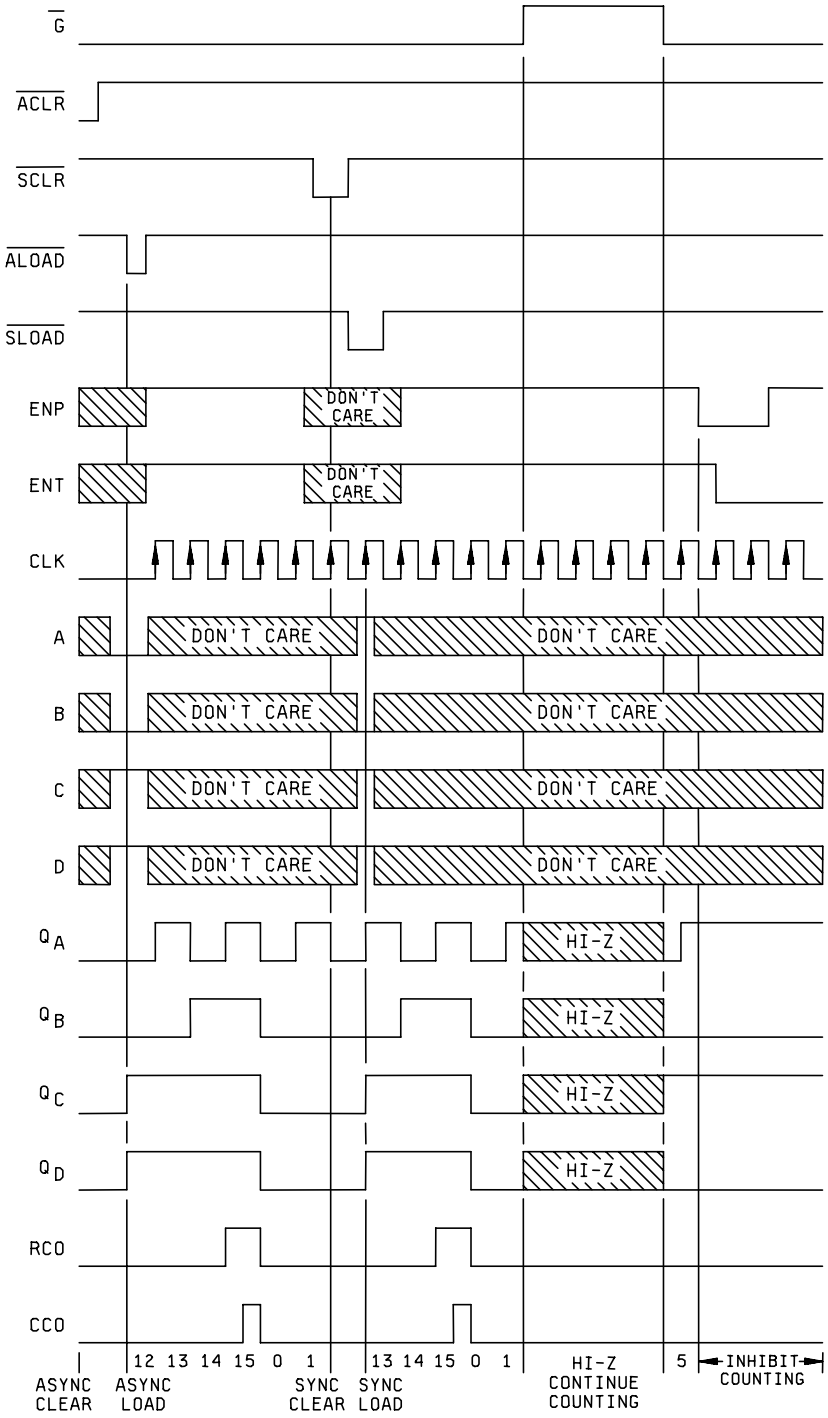


FIGURE 4. Counting sequences - Continued.

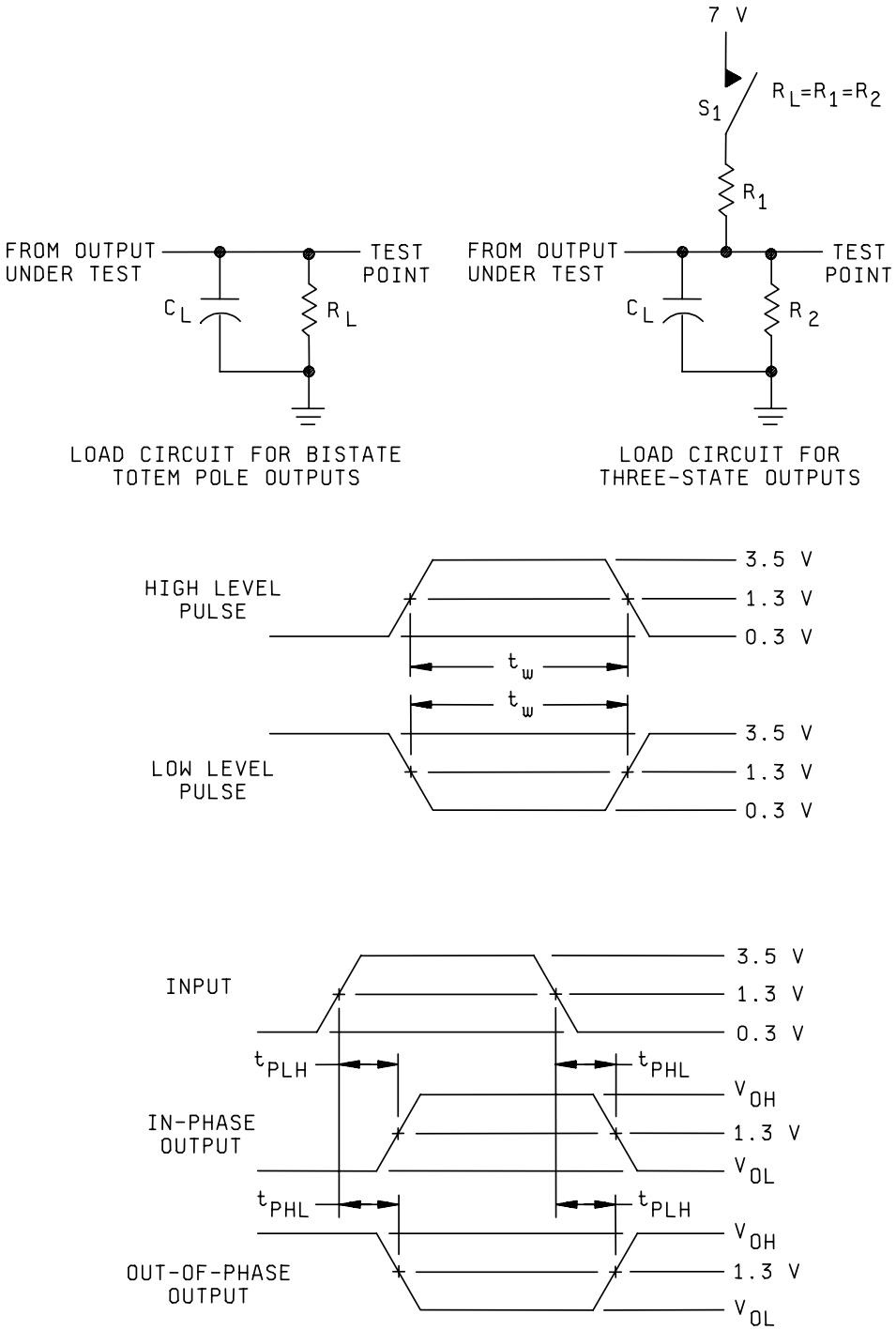
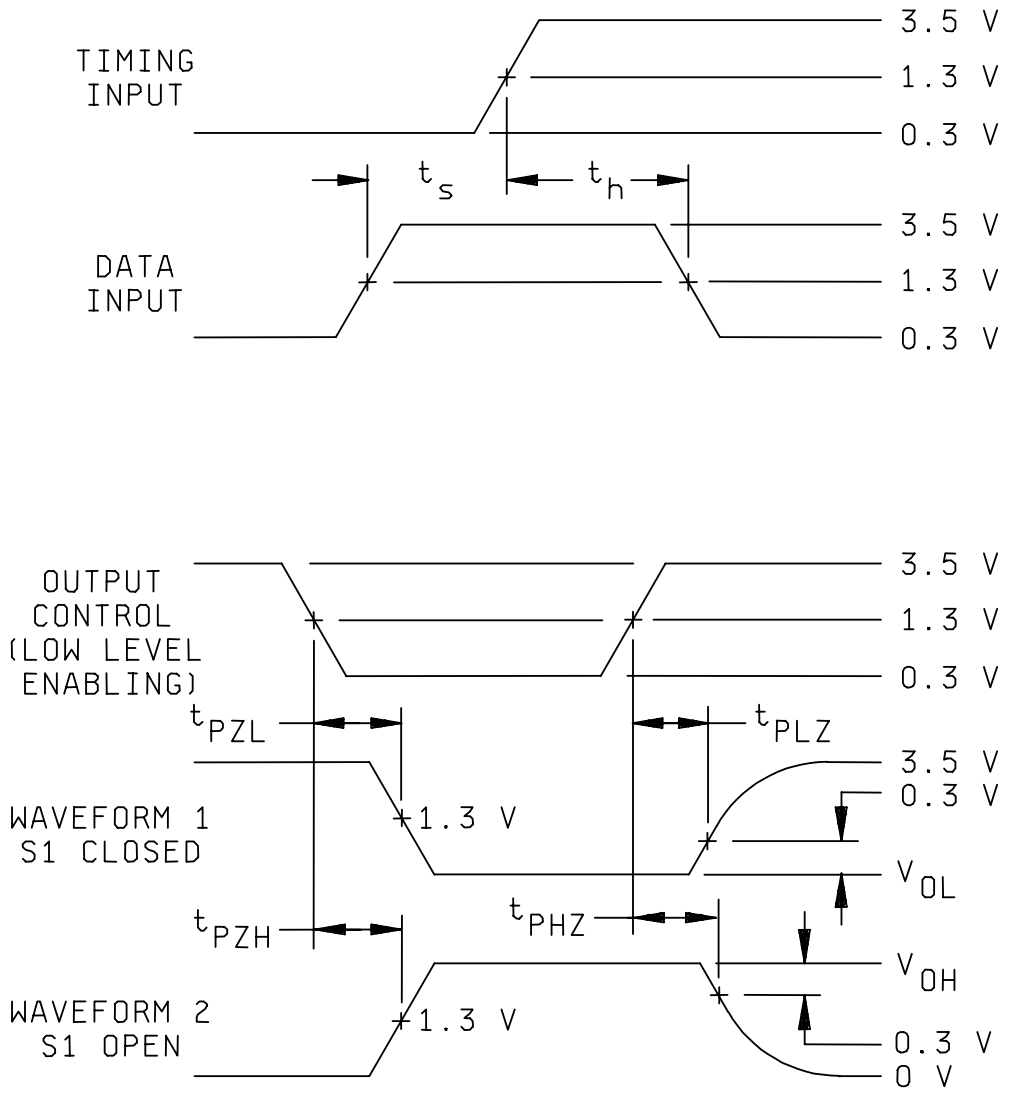


FIGURE 5. Test circuits and switching waveforms.



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
THREE STATE OUTPUTS

NOTES:
1. C_L includes probe and jig capacitance.
2. All inputs have the following characteristics: PRR ≤ 10 MHz, duty cycle = 50 percent, $t_r = t_f = 3$ ns ±1 ns.
3. The output are measured one at a time with one input transition per measurement.
4. Waveform 1 is for an output with internal conditions such that the output is low when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. When measuring propagation delay times of three-state outputs, switch S1 is open.

FIGURE 5. Test circuits and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-07-21

Approved sources of supply for SMD 83022 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
8302201EA	01295	SNJ54ALS161BJ	M38510/38001BEA
8302201FA	01295	SNJ54ALS161BW	M38510/38001BFA
83022012A	01295	SNJ54ALS161BFK	M38510/38001B2A
8302202EA	01295	SNJ54ALS163BJ	M38510/38002BEA
8302202FA	01295	SNJ54ALS163BW	M38510/38002BFA
83022022A	01295	SNJ54ALS163BFK	M38510/38002B2A
8302203RA	3/	SNJ54ALS561AJ	M38510/38004BRA
8302203SA	3/	SNJ54ALS561AW	M38510/38004BSA
83022032A	3/	SNJ54ALS561AFK	M38510/38004B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, Tx 75243 POC U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493