REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Change V_{IL} to 0.7 V. Change minimum clock pulse width, V_{OH2} test conditions, F_{MAX}, and propagation delays. Delete min limits from I_{IL} and propagation delays. Convert to military drawing format.	86-12-10	N. A. Hauck
D	Change clock pulse width to read 22 ns for all cases for device 01. Correct V_{IC} = 1.5 V to -1.5 V. Delete I_{OZH} and I_{OZL} tests. Change t_{PLH2} = 20 ns to 21 ns. For truth tables, clear mode, delete the third row for both devices. For logic diagram delete inversion circle for clear input amplifier and add inversion circles for both pairs of amplifiers on S1 and S0.	87-05-04	N. A. Hauck
E	Changes in accordance with NOR 5962-R082-92. -pn	92-07-06	Monica L. Poelking
F	Changes in accordance with NOR 5962-R051-96. -tmh	96-02-02	Monica L. Poelking
G	Update to reflect latest changes in format and requirements. Editorial changes throughout. -les	02-10-09	Raymond Monnin
H	Update to reflect latest changes in format and requirements. Correct paragraph in 3.5. Editorial changes throughout. –les	05-07-21	Raymond Monnin
J	Update drawing to current MIL-PRF-38535 requirements. - jt	16-01-11	Charles F. Saffle
K	Update drawing to latest MIL-PRF-38535 requirements. -jt	20-10-01	James R. Eschmeyer

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

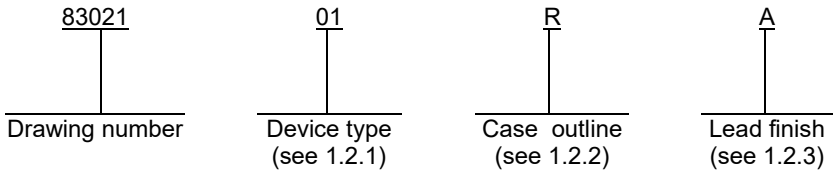
REV																			
SHEET																			
REV																			
SHEET																			
REV STATUS				REV			K	K	K	K	K	K	K	K	K	K	K	K		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A	PREPARED BY Greg A. Pitz	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/Landandmaritime**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Michael A. Frye APPROVED BY Nelson A. Hauck DRAWING APPROVAL DATE 84-02-17 REVISION LEVEL K	MICROCIRCUIT, DIGITAL, ADVANCED LOW-POWER SCHOTTKY TTL, SHIFT REGISTER, MONOLITHIC SILICON SIZE A / CAGE CODE **14933** / **83021** SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS299	8-bit bi-directional universal shift/storage register with three-state outputs and asynchronous clear
02	54ALS323	8-bit bi-directional universal shift/storage register and three-state outputs with synchronous clear

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5V dc at -18 mA to +7.0 V dc
I/O Ports	5.5 V dc maximum
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/	220 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R, S, and 2	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum clock pulse width (t_w) :	
Device type 01:	
Case R	22 ns
Case S and 2	22 ns
Device type 02:	
Cases R, S, and 2	20 ns
Minimum clear pulse width:	
Device type 01	12 ns
Minimum clear inactive state pulse width:	
Device type 01	15 ns
Minimum clear pulse data setup time:	
Device type 02:	
Low (active)	25 ns
High (inactive)	18 ns
Minimum setup time at select (S0, S1)	25 ns
Minimum setup time:	
High level data (SL, SR, A - H)	18 ns
Low level data (SL, SR, A - H)	15 ns
Minimum hold time (S0, S1, SL, SR, A - H):	
Device type 01	0 ns
Device type 02	1 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage (Q outputs)	V_{OH1}	V_{CC} = 4.5 V, V_{IN} = 0.7 or 2.0 V,	I_{OH} = -1.0 mA	1, 2, 3	All	2.4		V
High level output voltage (All other outputs)	V_{OH2}		I_{OH} = -0.4 mA			2.5		
Low-level output voltage (QA-QH)	V_{OL1}	V_{CC} = 4.5 V, V_{IN} = 0.7 or 2.0 V,	I_{OL} = 12 mA	1, 2, 3	All		0.4	V
Low-level output voltage (QA' or QH')	V_{OL2}		I_{OL} = 4 mA	1, 2, 3	All		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA	T_C = +25°C	1	All		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V,	All others	1, 2, 3	All		-200	µA
			$\overline{G}1$, $\overline{G}2$, CLK, CLR				-100	
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3	All		20	µA
High level input current (A-H)	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		100	µA
High level input current (Any other)	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 7.0 V		1, 2, 3	All		100	µA
Output current 1/	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V	QA-QH	1, 2, 3	All	-20	-112	mA
			QA', QH'	1, 2, 3	All	-15	-70	
Supply current, outputs high	I_{CCH}	V_{CC} = 5.5 V, V_{IN} = 5.0 V		1, 2, 3	All		28	mA
Supply current, outputs low	I_{CCL}	V_{CC} = 5.5 V, V_{IN} = 0 V		1, 2, 3	All		38	mA
Supply current outputs disabled	I_{CCZ}	V_{CC} = 5.5 V, V_{IN} = 5.0 V		1, 2, 3	All		40	mA
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V		9, 10, 11	All	17		MHz
Propagation delay time, clock QA-QH	t_{PLH1}	V_{CC} = 5.0 V,		9, 10, 11	All		19	ns
	t_{PHL1}	C_L = 50 pF ± 10%,		9, 10, 11	All		25	ns
Propagation delay time, clock QA'-QH'	t_{PLH2}	R_L = 500Ω ± 5%		9, 10, 11	All		21	ns
	t_{PHL2}			9, 10, 11	All		25	ns
Propagation delay time, high to low, clear to QA-QH	t_{PHL3}			9, 10, 11	01		29	ns
Propagation delay time, high to low, clear to QA'-QH'	t_{PHL4}			9, 10, 11	01		29	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable time, G to QA-QH	t_{PZH1}	V_{CC} = 5.0 V,	9, 10, 11	01		22	ns
	t_{PZL1}	C_L = 50 pF ± 10%,	9, 10, 11	01		27	ns
Enable time, S0 to QA-QH	t_{PZH3}	R_L = 500Ω ± 5%	9, 10, 11	01		27	ns
	t_{PZL3}		9, 10, 11	01		27	ns
Enable time, S1 to QA-QH	t_{PZH4}		9, 10, 11	01		27	ns
	t_{PZL4}		9, 10, 11	01		27	ns
Disable time, G to QA-QH	t_{PHZ1}		9, 10, 11	01		15	ns
	t_{PLZ1}		9, 10, 11	01		38	ns
Disable time, S0 to QA-QH	t_{PHZ3}		9, 10, 11	01		18	ns
	t_{PLZ3}		9, 10, 11	01		34	ns
Disable time, S1 to QA-QH	t_{PHZ4}		9, 10, 11	01		18	ns
	t_{PLZ4}		9, 10, 11	01		34	ns
Functional test		See 4.3.1c	7	01			

1/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Device types	01, 02	01, 02
Case outlines	R, S	2
Terminal number	Terminal symbols	
1	S0	S0
2	$\overline{G}$ 1	$\overline{G}$ 1
3	$\overline{G}$ 2	$\overline{G}$ 2
4	G/QG	G/QG
5	E/QE	E/QE
6	C/QC	C/QC
7	A/QA	A/QA
8	QA'	QA'
9	$\overline{CLR}$	$\overline{CLR}$
10	GND	GND
11	SR	SR
12	CLK	CLK
13	B/QB	B/QB
14	D/QD	D/QD
15	F/QF	F/QF
16	H/QH	H/QH
17	QH'	QH'
18	SL	SL
19	S1	S1
20	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Device type 01

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL 1/		CLOCK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
		S1	SQ	$\overline{G}1$	$\overline{G}2$		SL	SR										
CLEAR	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QAO	QBO	QCO	QDO	QEO	QFO	QGO	QHO	QAO	QHO
	H	X	X	L	L	L	X	X	QAO	QBO	QCO	QDO	QEO	QFO	QGO	QHO	QAO	QHO
SHIFT RIGHT	H	L	H	L	L	↑	X	H	H	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	H	QG_n
	H	L	H	L	L	↑	X	L	L	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	L	QG_n
SHIFT LEFT	H	H	L	L	L	↑	H	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	H	QB_n	H
	H	H	L	L	L	↑	L	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	L	QB_n	L
LOAD	H	H	H	X	X	↑	X	X	A	B	C	D	E	F	G	H	A	H

1/ When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however sequential operation or clearing of the register is not affected.

Device type 02

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL 1/		CLOCK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
		S1	SQ	$\overline{G}1$	$\overline{G}2$		SL	SR										
CLEAR	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QAO	QBO	QCO	QDO	QEO	QFO	QGO	QHO	QAO	QHO
	H	X	X	L	L	L	X	X	QAO	QBO	QCO	QDO	QEO	QFO	QGO	QHO	QAO	QHO
SHIFT RIGHT	H	L	H	L	L	↑	X	H	H	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	H	QG_n
	H	L	H	L	L	↑	X	L	L	QA_n	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	L	QG_n
SHIFT LEFT	H	H	L	L	L	↑	H	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	H	QB_n	H
	H	H	L	L	L	↑	L	X	QB_n	QC_n	QD_n	QE_n	QF_n	QG_n	QH_n	L	QB_n	L
LOAD	H	H	H	X	X	↑	X	X	A	B	C	D	E	F	G	H	A	H

1/ When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however sequential operation or clearing of the register is not affected.

FIGURE 2. Truth tables.

Device type 01

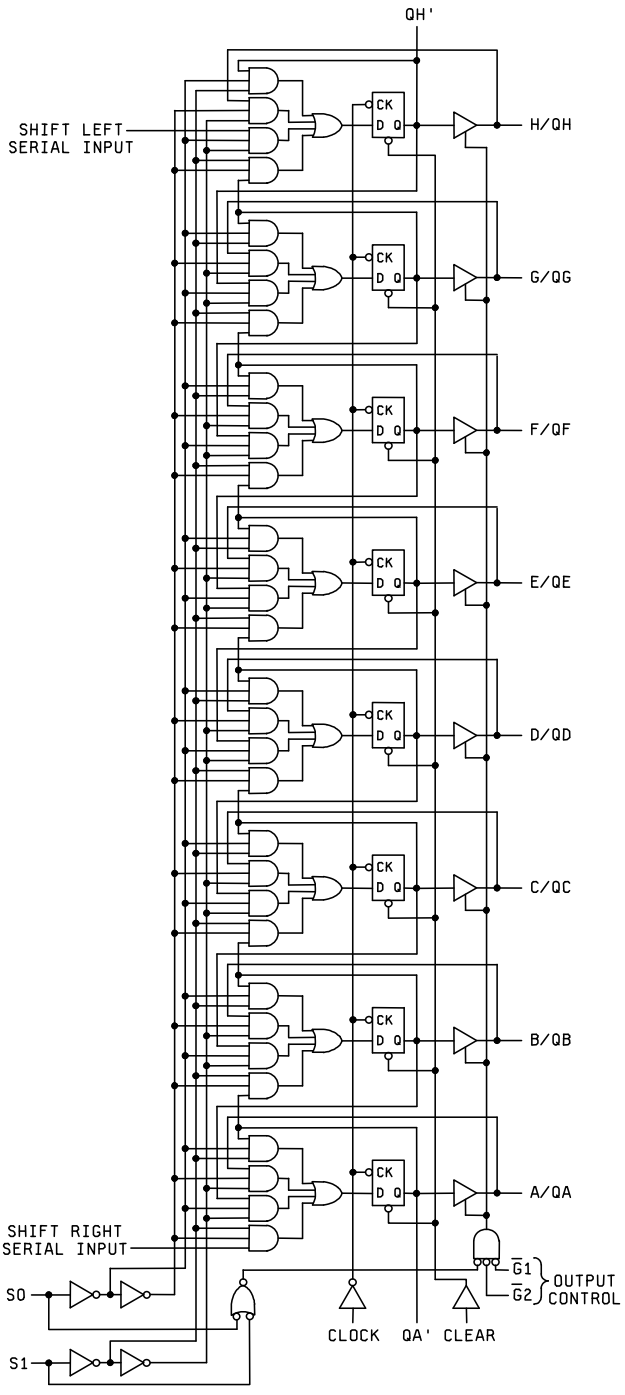


FIGURE 3. Logic diagrams.

Device type 02

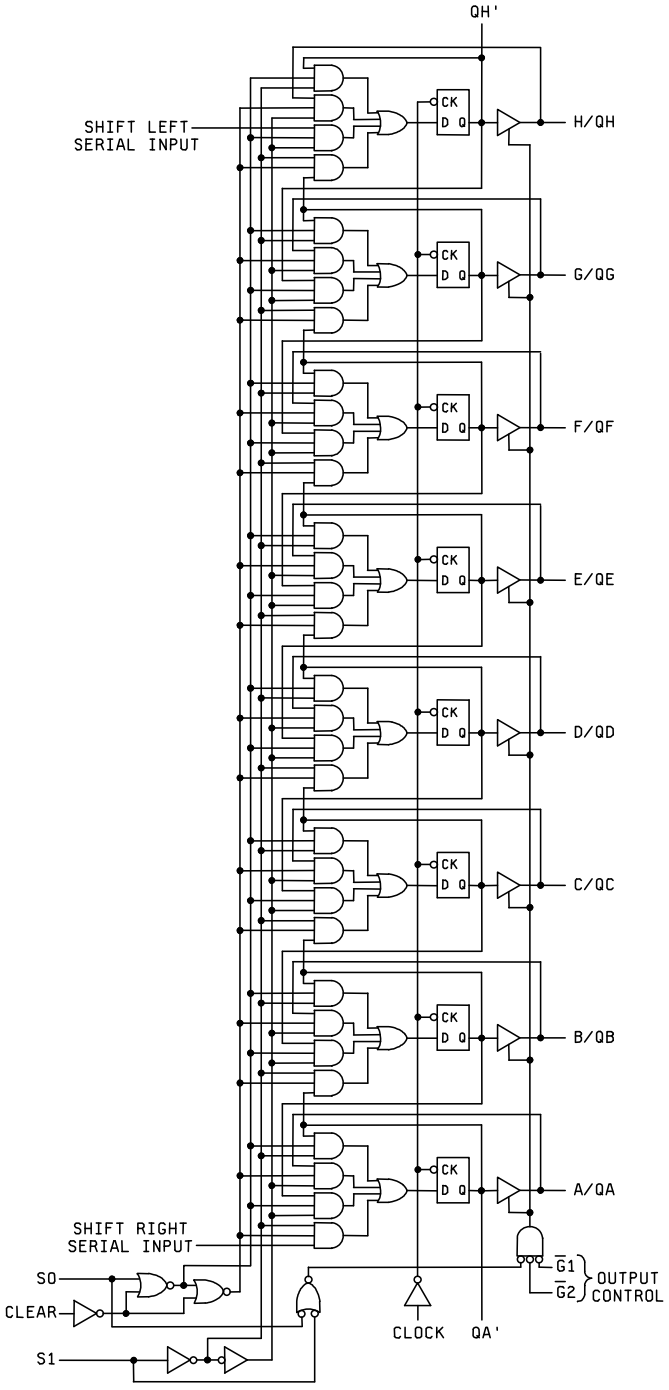


FIGURE 3. Logic diagrams - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-10-01

Approved sources of supply for SMD 83021 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
8302101RA	01295	SNJ54ALS299J	M38510/37601BRA
8302101SA	01295	SNJ54ALS299W	M38510/37601BSA
83021012A	01295	SNJ54ALS299FK	M38510/37601B2A
8302102RA	01295	SNJ54ALS323J	M38510/37602BRA
8302102SA	01295	SNJ54ALS323W	M38510/37602BSA
83021022A	3/	SNJ54ALS323FK	M38510/37602B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243