NOTICE OF REVISION (NOR)

This revision described below has been authorized for the document listed.

1. DATE (YYMMDD): 95-04-13

Form Approved OMB No. 0704-0188

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2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME (First, Middle Initial, Last)

b. ADDRESS (Street, City, State, Zip Code)
Defense Electronics Supply Center
1507 Wilmington Pike
Dayton, OH 45444-5765

5. CAGE CODE: 67268

6. NOR NO.: 5962-R115-95

7. CAGE CODE: 67268

8. DOCUMENT NO.: 83013

9. TITLE OF DOCUMENT
MICROCIRCUIT, DIGITAL, CMOS, 8-BIT MICROPROCESSOR, CPU, MONOLITHIC SILICON

10. REVISION LETTER
a. CURRENT: C
b. NEW: D

11. ECP NO.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "x".
Revisions description column; add "Changes in accordance with NOR 5962-R115-95".
Revisions date column; add "95-04-13".
Revision level block; add "D".
Rev status of sheets; For sheets 1, 5, and 7, change to "D".

Sheet 5: Table I: Address setup time t_{SAD}, device type 01: delete "45 ns minimum" and substitute "105 ns minimum".
Revision level block; change to "D".

Sheet 7: Table I: XIN to clock falling t_{XCF}, device type 01: delete "15 ns minimum" and substitute "5 ns minimum".
Table I: XIN to clock rising t_{XCR}, device type 01: delete "15 ns minimum" and substitute "5 ns minimum".
Revision level block; change to "D".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)

X	(1) Existing document supplemented by the NOR may be used in manufacture.
	(2) Revised document must be received before manufacturer may incorporate this change.
	(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT: DESC-ELDC

c. TYPED NAME (First, Middle Initial, Last): Monica L. Poelking

d. TITLE: Chief, Custom Microelectronics Branch

e. SIGNATURE: Monica L. Poelking

f. DATE SIGNED (YYMMDD): 95-04-13

15a. ACTIVITY ACCOMPLISHING REVISION: DESC-ELDC

b. REVISION COMPLETED (Signature): Larry T. Gauder

c. DATE SIGNED (YYMMDD): 95-04-13

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Change electrical performance characteristics. Add footnote to figure 3. Change drawing CAGE code to 67268. Change f_{max} for device type 02 to 3.5 Mhz. Editorial changes throughout.	1989 Sept 6	W. Heckman

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	C	C	C	C	C															
SHEET	15	16	17	18	19															

REV STATUS OF SHEETS																
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
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DRAWING APPROVAL DATE
4 November 1983

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 8-BIT
MICROPROCESSOR, CPU, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**83013**

SHEET 1 OF 19

* US GOVERNMENT PRINTING OFFICE: 1987--748-129/60912
5962-E1264
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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

83013	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	f_{max}
01	NSC800	8 bit micro processor	2.5 MHz
02	NSC800-35	8 Bit microprocessor	3.5 MHz

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
QD-5	(40-lead, 2.096" x .620" x .225") dual-in-line package
ZC-5	(44-terminal, .662" x .662" x .120") square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range . . . . . +3 V dc to +7 V dc
Voltage on any pin with respect to ground . . . . . -0.3 V dc to V_{CC} +0.3 V dc
Storage temperature range . . . . . -65°C to +150°C
Maximum power dissipation (P_D):
Case Q . . . . . 1 W
Case Z . . . . . 500 mW
Lead temperature (soldering, 10 seconds) . . . . . +300°C
Junction temperature (T_J) . . . . . +150°C
Thermal resistance, junction to case (O_{JC}) . . . . . See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Case operating temperature range (T_C) . . . . . -55°C to +125°C
Operating supply voltage range (V_{CC}) . . . . . +4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})(logic inputs):
V_{CC} at 4.5 V . . . . . 3.6 V dc to 4.5 V dc
V_{CC} at 5.5 V . . . . . 4.4 V dc to 5.5 V dc
Maximum low level input voltage (V_{IL})(logic inputs):
V_{CC} at 4.5 V . . . . . 0 V dc to 0.9 V dc
V_{CC} at 5.5 V . . . . . 0 V dc to 1.1 V dc

Frequency of operation (f_{max}), V_{CC} at 5 V:
Device type 01 . . . . . 0.5 MHz to 2.5 MHz
Device type 02 . . . . . 0.5 MHz to 3.5 MHz
Clock cycle time (t_{CYC}):
Device type 01 . . . . . 400 ns minimum
Device type 02 . . . . . 300 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Logical "1" input voltage	V_{IH}	V_{CC} = 4.5 V	1, 2, 3	3.6	4.5	V
		V_{CC} = 5.5 V	1, 2, 3	4.4	5.5	V
Logical "0" input voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3	0	0.9	V
		V_{CC} = 5.5 V	1, 2, 3	0	1.1	V
Logical "1" output voltage	V_{OH}	4.5 V $\le V_{CC} \le$ 5.5 V, I_{OUT} = -1 mA	1, 2, 3	2.4		V
		V_{CC} = 4.5 V, I_{OUT} = -10 µA	1, 2, 3	4.0		V
		V_{CC} = 5.5 V, I_{OUT} = -10 µA	1, 2, 3	5.0		V
Logical "0" output voltage	V_{OL}	4.5 V $\le V_{CC} \le$ 5.5 V, I_{OUT} = 2 mA	1, 2, 3	0	0.4	V
		4.5 V $\le V_{CC} \le$ 5.5 V, I_{OUT} = 10 µA	1, 2, 3	0	0.1	V
Logical "0" input current	I_{IL}	V_{CC} = 4.5 V, O $\le V_{IL} \le$ 0.9 V	1, 2, 3		-10	µA
		V_{CC} = 5.5 V, 0 $\le V_{IL} \le$ 1.1 V	1, 2, 3		-10	µA
Logical "1" input current	I_{IH}	V_{CC} = 4.5 V, 3.6 V $\le V_{IH} \le$ 4.5 V	1, 2, 3		10	µA
		V_{CC} = 5.5 V, 4.4 V $\le V_{IH} \le$ 5.5 V	1, 2, 3		10	µA
Logical "0" output current	I_{OL}	4.5 V $\le V_{CC} \le$ 5.5 V, V_{OL} = 0	1, 2, 3		-10	µA
Logical "1" output current	I_{OH}	V_{CC} = 4.5 V, V_{OH} = 4.5 V	1, 2, 3		10	µA
		V_{CC} = 5.5 V, V_{OH} = 5.5 V	1, 2, 3		10	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0, f_{XIN} = 7 MHz (no load) for device type 02	1, 2, 3		21	mA
		V_{CC} = 5.5 V, I_{OUT} = 0, f_{XIN} = 5 MHz (no load) for device type 01	1, 2, 3		15	mA
Input capacitance	C_{IN}	$T_C = +25^\circ C$, see 4.3.1c	4		14	pF
Output capacitance	C_{OUT}	$T_C = +25^\circ C$, see 4.3.1c	4		20	pF
Functional tests		See 4.3.1d	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Period at X_{IN} and X_{OUT}	t_x	4.5 V ≤ V_{CC} ≤ 5.5 V C_L = 100 pF See figure 3	01	9, 10, 11	0.2	1/ 3.33	µs
			02	9, 10, 11	.142	1/ 3.33	µs
Clock cycle time	t_{CYC}		01	9, 10, 11	0.4	1/ 6.66	µs
			02	9, 10, 11	0.284	1/ 6.66	µs
Address setup time	t_{SAD}		01	9, 10, 11	45		ns
			02		45		
Address hold time	t_{HAD}		01	9, 10, 11	60		ns
			02		35		
Read access time opcode fetch 2/	t_{ACCOP}		01	9, 10, 11		490	ns
			02			340	
ALE to valid data (memory read) 2/	$t_{ACC(MR)}$		01	9, 10, 11		620	ns
			02	9, 10, 11		405	
Write data setup time	t_{SWD}		01	9, 10, 11	75		ns
			02		35		
Write data hold time	t_{HWD}		01	9, 10, 11	100		ns
			02		85		
ALE width	t_{WALE}		01	9, 10, 11	130		ns
			02		115		
Write strobe width 2/	t_{WWR}		01	9, 10, 11	370		ns
			02		250		
Refresh strobe width	t_{WRFSH}		01	9, 10, 11	725		ns
			02		450		
Wait input width	t_{WWAIT}		01	9, 10, 11	250		ns
			02		195		
Read strobe width during opcode fetch 2/ 3/	t_{WRD}		01	9, 10, 11	360		ns
			02		210		
Address hold time during opcode fetch	t_{HADH1}		All	9, 10, 11	0 1/		ns
Address hold time during memory or I/O read/write	t_{HADH2}		01	9, 10, 11	1/ 100		ns
			02		70 1/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Falling edge of ALE to leading edge of read strobe	t_{DAR}	$4.5\ V \le V_{CC} \le 5.5\ V$ $C_L = 100\ pF$ See figure 3	01	9, 10, 11	160	250	ns
			02		100	180	
Falling edge of ALE to leading edge of WR	t_{DAW}		01	9, 10, 11	350	420	ns
			02		225	300	
Falling edge of ALE to wait input valid	t_{DWAIT}		01	9, 10, 11		250	ns
			02			170	
Falling edge of ALE to input valid 2/ 4/ 5/	t_{D1}		01	9, 10, 11		475	ns
			02			285	
Input width 5/	t_{W1}		01	9, 10, 11	200		ns
			02		140		
Falling edge of ALE to interrupt acknowledge strobe	t_{DAI}		01	9, 10, 11	160		ns
			02		95		
Interrupt acknowledge strobe width 2/ 6/	t_{WINTA}		01	9, 10, 11	400		ns
			02		225		
Falling edge of ALE to falling edge of bus acknowledge 2/ 4/	t_{DBACK1}		01	9, 10, 11	975		ns
			02		635		
Rising edge of bus request to falling edge of bus acknowledge	t_{DBACK2}		01		200	700	ns
			02		140	540	
Rising edge of power save to falling edge of ALE	t_{DPA}		01	9, 10, 11	200	760	ns
			02		140	580	
ALE setup time	t_{SALE}		01	9, 10, 11	70		ns
			02		55		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

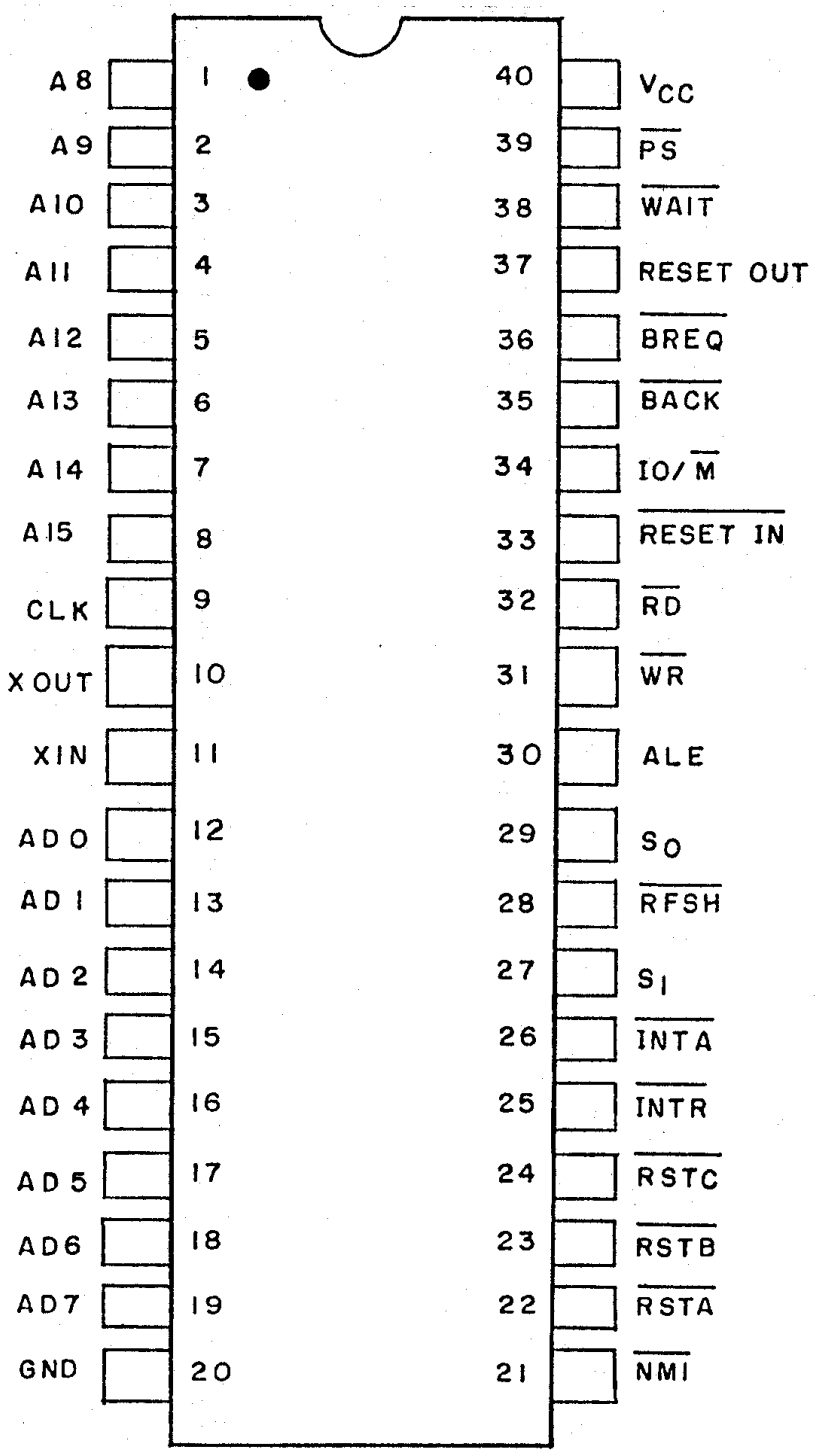
Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Clock rise time 7/	t_R	8/ 9/	01	9, 10, 11		110	ns
			02	9, 10, 11		90	
Clock fall time 7/	t_F	See figure 3	01	9, 10, 11		60	ns
			02	9, 10, 11		55	
Clock low time 10/	t_L		01	9, 10, 11	150		ns
			02	9, 10, 11	90		
Clock high time 10/	t_H		01	9, 10, 11	145		ns
			02	9, 10, 11	85		
$\overline{BREQ}$ setup time	t_{BRS}		01	9, 10, 11	50		ns
			02	9, 10, 11	50		
Clock falling to ALE falling	t_{CAF}		01	9, 10, 11	0	65	ns
			02	9, 10, 11	0	60	
Clock falling to ALE rising	t_{CAR}		01	9, 10, 11	0	100	ns
			02	9, 10, 11	0	90	
Clock rising to read rising	t_{CRD}		01	9, 10, 11		90	ns
			02	9, 10, 11		90	
Clock rising to refresh falling	t_{CRF}		01	9, 10, 11		70	ns
			02	9, 10, 11		70	
Interrupt setup time	t_{INS}		01	9, 10, 11	50		ns
			02	9, 10, 11	50		
$\overline{RFSH}$ rising to ALE falling	t_{RFLF}		01	9, 10, 11	50		ns
			02	9, 10, 11	45		
$\overline{RD}$ rising to ALE rising (memory read)	$t_{RL(MR)}$		01	9, 10, 11	100		ns
			02	9, 10, 11	50		
$\overline{WR}$ rising to ALE rising	t_{WL}		01	9, 10, 11	130		ns
			02	9, 10, 11	70		
$\overline{WAIT}$ setup time	t_{WS}		01	9, 10, 11	70		ns
			02	9, 10, 11	60		
X_{IN} to clock falling	t_{XCF}		01	9, 10, 11	15	95	ns
			02	9, 10, 11	5	90	
X_{IN} to clock rising	t_{XCR}		01	9, 10, 11	15	85	ns
			02	9, 10, 11	5	90	
$\overline{BACK}$ falling to clock falling	t_{BACL}		01	9, 10, 11	125		ns
			02	9, 10, 11	70		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

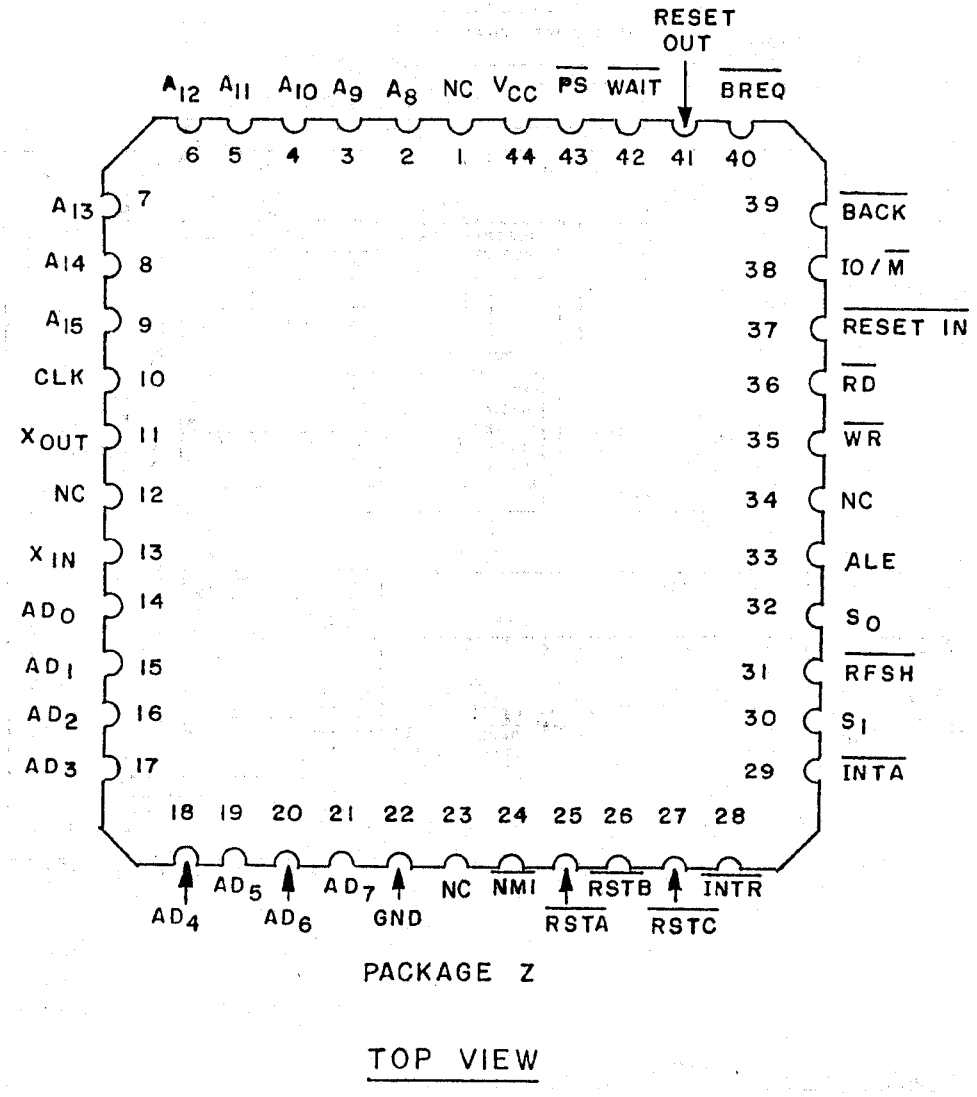
Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Address float after RD falling	t_{AFR}	1/	01	9, 10, 11		0	ns
			02	9, 10, 11		0	
$\overline{BACK}$ rising to bus enable	t_{BABE}	See figure 3	01	9, 10, 11		400	ns
			02	9, 10, 11		300	
$\overline{BACK}$ falling to bus float	t_{BABF}		01	9, 10, 11		50	ns
			02	9, 10, 11		50	
$\overline{BREQ}$ hold time	t_{BRH}		01	9, 10, 11	0		ns
			02	9, 10, 11	0		
Address hold time during memory or IO, RD and WR	$t_{H(ADH)2}$		01	9, 10, 11	100		ns
			02	9, 10, 11	70		
Width of NMI input	t_{NMI}		01	9, 10, 11	30		ns
			02	9, 10, 11	20		
Data hold after read	t_{RDH}		01	9, 10, 11	0		ns
			02	9, 10, 11	0		
Wait hold time	t_{WH}		01	9, 10, 11	0		ns
			02	9, 10, 11	0		
Interrupt hold time	t_{INH}		01	9, 10, 11	0		ns
			02	9, 10, 11	0		

1/ Guaranteed to the limits specified in table I, if not tested.
2/ Add t_{CYC} for each WAIT state.
3/ Add $t_{CYC/2}$ for memory read cycles.
4/ Add t_{CYC} for each opcode fetch cycle.
5/ Applies to INTR, NMI, RSTA, RSTB, RSTC, PS, and BREQ.
6/ Add 2 t_{CYC} for first INTA of each interrupt response string.
7/ Measured from 10% to 90%.
8/ t_{CYC} = 300 ns for device type 02.
9/ t_{CYC} = 400 ns for device type 01.
10/ 50% duty cycle, square wave input on X_{IN}.



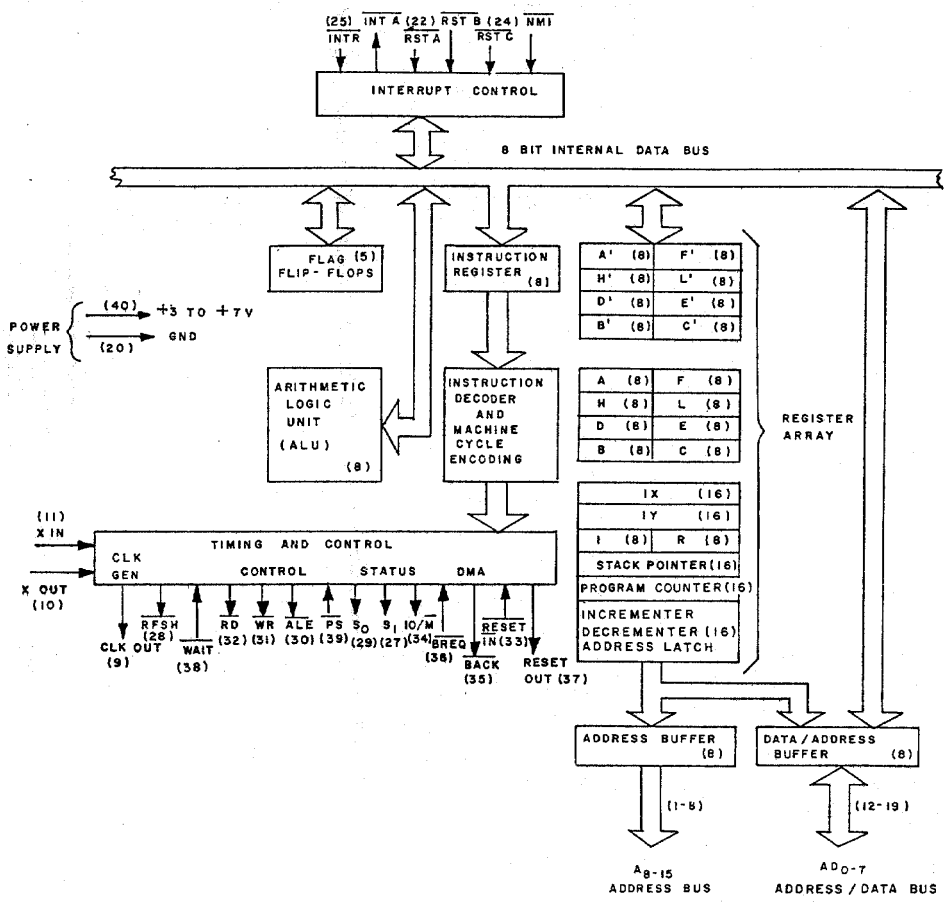
PACKAGE Q

FIGURE 1. Terminal connections.



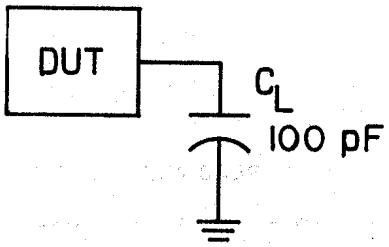
NC = No Connection

FIGURE 1. Terminal connections - Continued.



NOTE: Applicable pinout numbers are included within parentheses (referenced to package Q).

FIGURE 2. Logic diagram.



TEST CIRCUIT

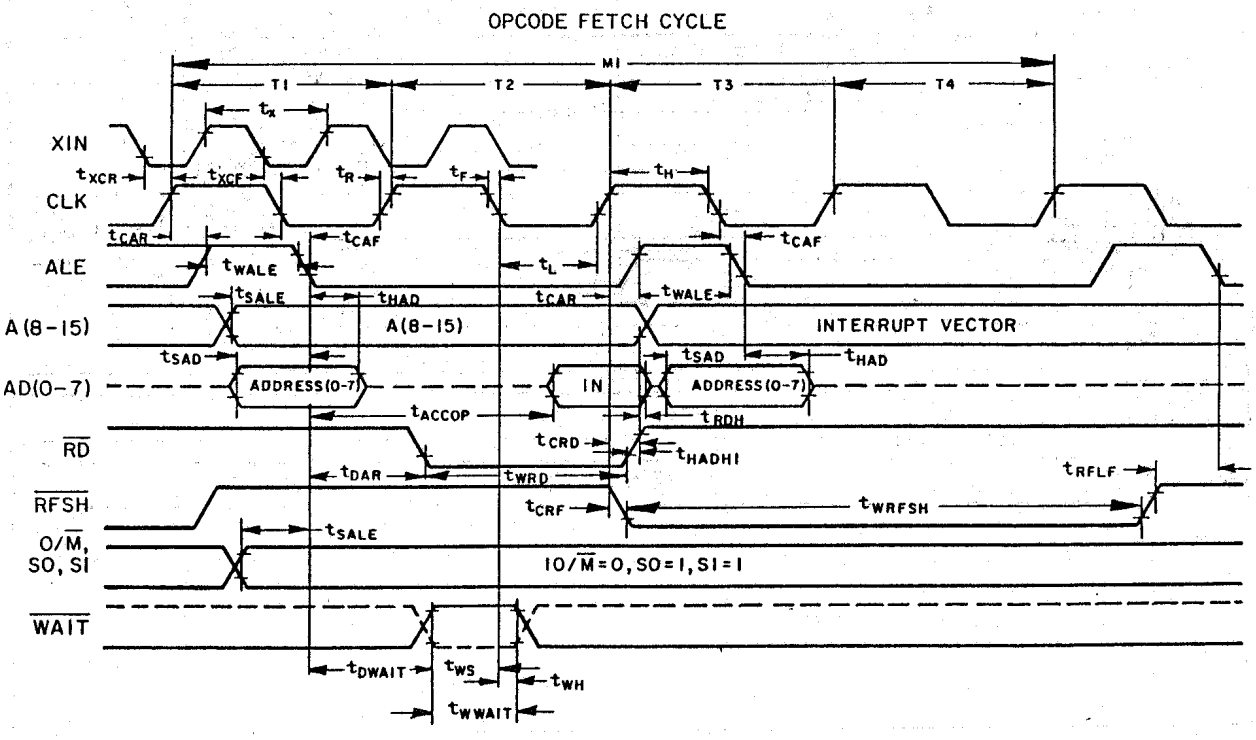


FIGURE 3. Test circuit and timing waveforms.

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		REVISION LEVEL C	SHEET 12

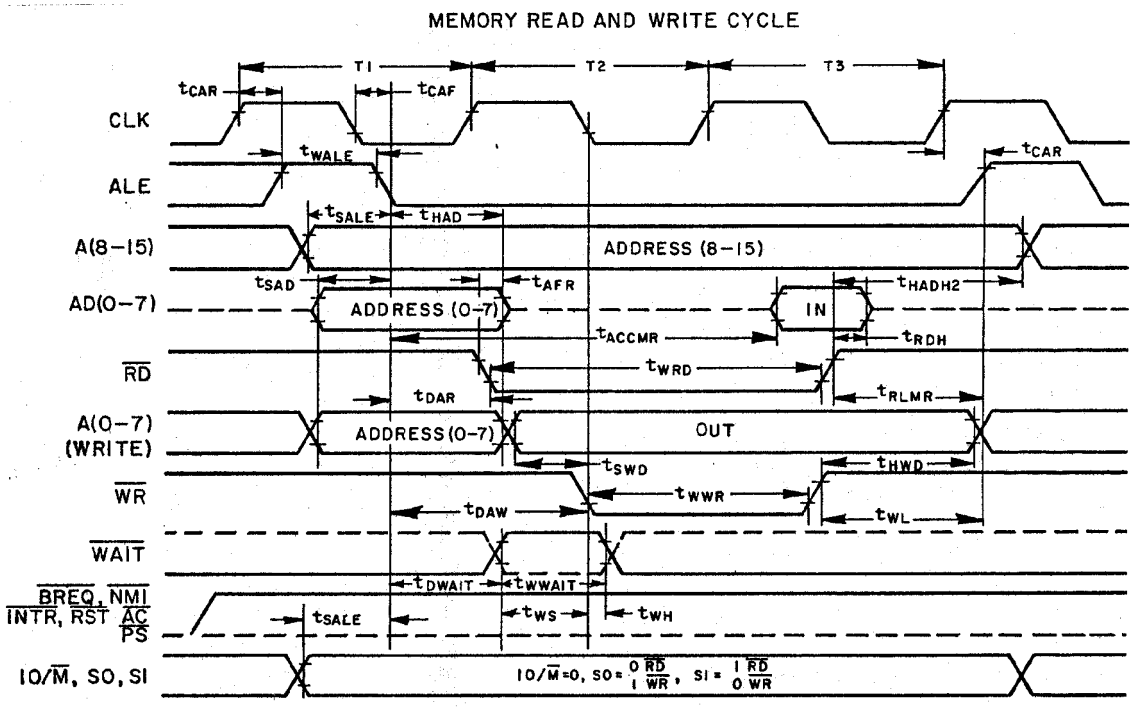
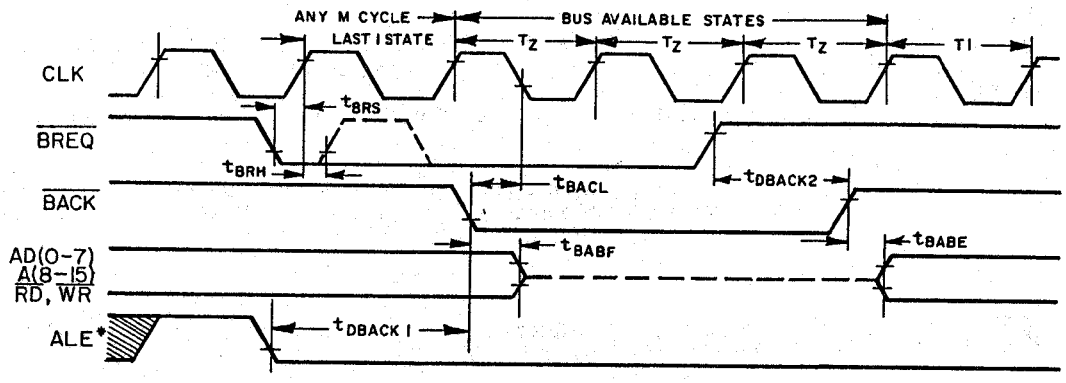


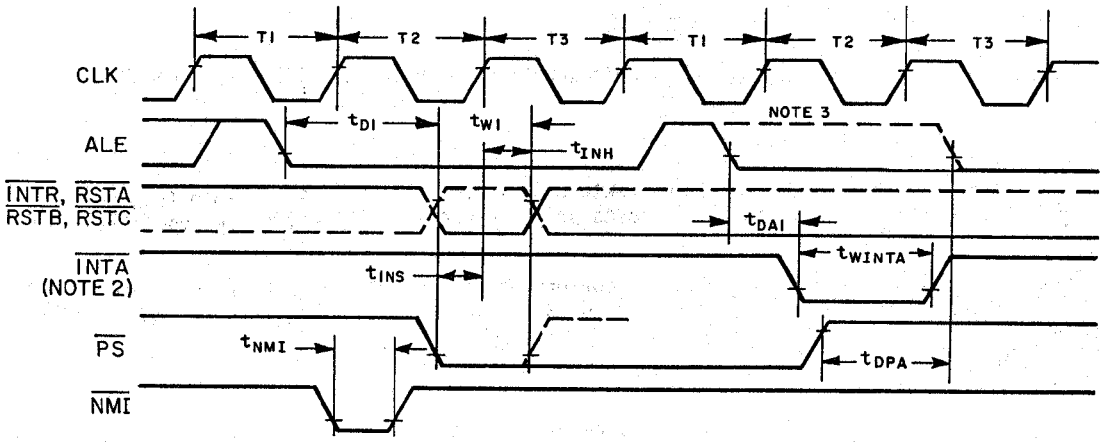
FIGURE 3. Test circuit and timing waveforms - Continued.

BUS ACKNOWLEDGE CYCLE



*Waveform not drawn to proportion. Use only for specifying test points.

INTERRUPT-POWER SAVE CYCLE



NOTES:

1. This t state is the last t state of the last M cycle of any instruction.
2. Response to INTR input.
3. Response to PS input.
4. Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

FIGURE 3. Test circuit and timing waveforms - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D, using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = 125^\circ C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 functional testing shall include verification of instruction set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D, using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = 125^\circ C$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (method 5005)	1, 2, 3
Group D end-point electrical parameters (method 5005)	1
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional descriptions for this device shall be as follows:

SYSTEM DEFINITIONS

Symbol	Function
$\overline{\text{RESET IN}}$	Reset input: Active low. Sets A(8-15) and AD(0-7) to three-state (high impedance). Clears the contents of PC, I and R registers, disables interrupts, and causes a reset output to be activated.
$\overline{\text{BREQ}}$	Bus request: Active low. Used when another device isrequesting the system bus. BREQ is recognized at the endof the current machine cycle, then A(8-15), AD(0-7), IO/M, RD and WR are set to the high impedance mode and the request is acknowledged via the BACK output signal.
$\overline{\text{NMI}}$	Nonmaskable interrupt: Active low. The nonmaskable interrupt, generated by the peripheral device(s), is the highest priority interrupt request line. Input is only recognized at the end of the current instruction. Its execution is independent of the interrupt enable flip-flop. NMI execution involves saving the PC on the stack and automatic branching to restart address X'0066 in memory.
$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, RSTC	Restart interrupts A, B, C: Active low. Restarts generated by the peripherals are recognized at the end of the current instruction if their respective interrupt enable bits (andIFF1/IFF2) are set. Execution is identical to NMI except interrupts are enable for the following restart addresses:

NAME	RESTART ADDRESS (X')
$\overline{\text{RSTA}}$	003C
$\overline{\text{RSTB}}$	0034
RSTC	002C

The order of priority is fixed (highest first) as follows:

1)$\overline{\text{RSTA}}$, 2)$\overline{\text{RSTB}}$, 3)$\overline{\text{RSTC}}$

Symbol	Function
$\overline{\text{INTR}}$	Interrupt request: Active low. An interrupt request input generated by a peripheral device is recognized at the end of the current instruction provided that the interrupt enable and master interrupt enable bits are set. INTR is the lowest priority interrupt request input. Under program control, INTR can be executed in three distinct modes in conjunction with the INTA output.
$\overline{\text{WAIT}}$	Wait: Active low. When set low during $\overline{\text{RD}}$ or $\overline{\text{WR}}$, the CPU extends its machine cycle in increments of t (wait) states. The wait machine cycle continues until the WAIT input returns high.
$\overline{\text{PS}}$	Power save: Active low. $\overline{\text{PS}}$ is sampled at the end of the current instruction cycle. When PS is low, the CPU stops executing at the end of current instruction and keeps itself in the low-power mode. Normal operation resumes when PS is returned high.
$\overline{\text{BACK}}$	Bus acknowledge: Active low. $\overline{\text{BACK}}$ indicates to the bus requesting device that the CPU bus and its control signals are in the three-state mode. The requesting device may then take control of the bus and its control signals.
A(8-15)	Address bits 8-15: Active high. These are the most significant 8 bits of the memory address bus, or of the input/output address. During a BREQ/BACK cycle, the A(8-15) bus is in the three-state mode.
RESET OUT	Reset out: Active high. When RESET OUT is high, it indicates the CPU is being reset. The signal is normally used to reset the peripheral devices.
IO/$\overline{\text{M}}$	Input/output/memory: An active high on the IO/$\overline{\text{M}}$ output signifies that the current machine cycle is relative to an input/output device. An active low on the IO/M output signifies that the current machine cycle is relative to memory. It is three-state during BREQ/BACK cycles.
$\overline{\text{RFSH}}$	Refresh: Active low. The refresh output indicates that the dynamic RAM refresh cycle is in progress. RFSH goes low during T3 and T4 states of all M1 cycles.
ALE	Address latch enable: ALE is active only during the T1 state of M cycles and T3 state of M1 cycles. The high to low transition of ALE indicates that a valid memory/IO/refresh address is available on the AD(0-7) lines.
$\overline{\text{RD}}$	Read strobe: Active low. On the trailing edge of the $\overline{\text{RD}}$ strobe, data are input to the CPU via the AD(0-7) lines. The RD line is in the three-state mode during BREQ/BACK cycles.
$\overline{\text{WR}}$	Write strobe: While the $\overline{\text{WR}}$ line is low, valid data are output by theCPU on the AD(0-7) lines. The WR line is in the three-state mode during BREQ/BACK cyles.
CLK	Clock: CLK is an output provided for use as a system clock. The CLK output is a square wave at one half the input frequency.

Symbol Function

$\overline{\text{INTA}}$ — Interrupt acknowledge: Active low. The interrupt acknowledge output is activated in the M1 cycle (S) immediately followingthe state in which the INTR input is recognized. (Output is normally used to gate the interrupt response vector from the peripheral controller onto the AD(0-7) lines.) It is used intwo of the three interrupt modes. In mode 0, an instructionis gated onto the AD(0-7) line during INTA. In mode 2, a singleinterrupt response vector is gated onto the data bus.

S0,S1 — Status. Bus status outputs indicate encoded information regardingthe ensuing M cycle as follows:

S1	S0	STATE
0	0	HALT
0	1	WRITE
1	0	READ
1	1	(OPCODE) FETCH

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
8301301QX	27014	NSC8OOD/883B
8301301ZX	27014	NSC8OOE/883B
8301302QX	27014	NSC8OOD-35/883
8301302ZX	27014	NSC8OOE-35/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, CA 95051