

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
J	Deleted reference to checkerboard pattern in 3.2.2.1. Deleted footnote reference to how subgroups 7 and 8 are verified in table II. Added footnote 2 to device types 11RX, 12RX, 13RX, and 14RX. Removed reference to case outline Y in 6.6, previously replaced with case outline S. Editorial changes throughout.	89-12-04	M. A. Frye
K	Changes in accordance with NOR 5962-R220-96	96-09-13	William Johnson
L	Boilerplate update, part of 5 year review. REDRAWN ksr	05-06-14	Raymond Monnin
M	Updated boilerplate paragraphs as part of a 5 year review. ksr	10-11-10	Charles F. Saffle
N	Update drawing to reflect current MIL-PRF-38535 requirements. – llb	17-12-13	Charles F. Saffle

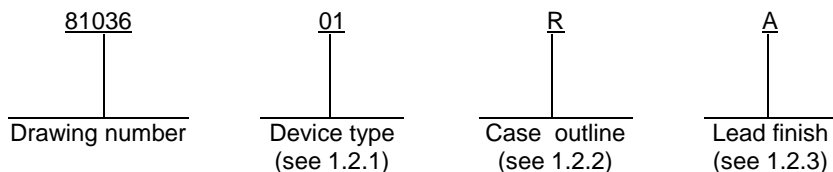


REV																				
SHEET																				
REV	N	N	N	N	N	N														
SHEET	15	16	17	18	19	20														
REV STATUS OF SHEETS	REV			N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	14		
PMIC N/A	PREPARED BY James Jamison						DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.dla.mil/landandmaritime													
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles Reusing																			
	APPROVED BY Michael A. Frye						MICROCIRCUIT, MEMORY, DIGITAL, BIPOLAR, PROGRAMMABLE LOGIC, MONOLITHIC SILICON													
	DRAWING APPROVAL DATE 82-07-22																			
	REVISION LEVEL N						SIZE A	CAGE CODE 67268	81036											
						SHEET						1 OF 20								

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01, 07, 11	PAL16L8, L8A, L8A-2	16-input 8-output AND-OR invert gate array
02, 08, 12	PAL16R8, R8A, R8A-2	16-input 8-output registered AND-OR gate array
03, 09, 13	PAL16R6, R6A, R6A-2	16-input 6-output registered AND-OR gate array
04, 10, 14	PAL16R4, R4A, R4A-2	16-input 4-output registered AND-OR gate array
05	PAL16X4	16-input 4-output registered AND-OR exclusive OR gate array
06	PAL16A4	16-input 4-output registered and-carry-or exclusive OR gate array

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	Flat package <u>1/</u>
2	CQCC1-N20	20	Square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (platinum-silicide)	-0.5 to +7.0 V dc
Supply voltage (titanium-tungsten)	-0.5 to +12.0 V dc
Input voltage range	-0.5 to +5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{jc}) <u>2/</u>	See MIL-STD-1835
Output voltage applied	-0.5 V to V_{cc} maximum dc <u>3/</u>
Output sink current	100 mA
Maximum power dissipation (P_D) <u>4/</u>	
Device types 01, 02, 03, 04, 05, and 06	2.0 W
Device types 07, 08, 09, and 10	1.0 W
Device types 11, 12, 13, and 145 W
Maximum junction temperature (T_J)	+175°C

- 1/ Outline letter Y was removed along with corresponding case outline, figure 1 (herein), and replaced with outline letter S with corresponding case outline F-9 (MIL-STD-1835).
- 2/ Heat sinking is recommended to reduce the junction temperature.
- 3/ Except during programming.
- 4/ Must withstand the added PD due to short circuit test (e.g., los).

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1.4 Recommended operating conditions.

Supply voltage	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc
Case operating temperature range (T _c).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of fuses shall be programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of fuses programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

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3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.2.4 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer's QM plan, the "QD" certification mark shall be used in place of the "Q" or "QML" certification mark. (For QD Product only.)

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10. Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _I = -18 mA	All	1, 2, 3		-1.5	V
High level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, I _{OH} = -2 mA	1-10	1, 2, 3	2.4		V
			11-14		2.3		
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, I _{OL} = 12 mA	All	1, 2, 3		0.5	V
High level input voltage	V _{IH}	<u>1/</u>	All	1, 2, 3	2		V
Low level input voltage	V _{IL}	<u>1/</u>	All	1, 2, 3		0.8	V
High level input current	I _{IH}	V _{CC} = 5.5 V, V _I = 2.4 V <u>2/</u>	All	1, 2, 3		40	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V <u>2/</u>	All	1, 2, 3		-0.25	mA
Output short circuit current	I _{OS}	V _{CC} = 5.5 V, V _O = 0.5 V <u>3/</u>	All	1, 2, 3	-30	-250	mA
Input Current	I _I	V _{CC} = 5.5 V, V _I = 5.5 V	All	1, 2, 3		1	mA
Off-state output current	I _{OZL}	V _{CC} = 5.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, V _O = 0.4 V <u>2/</u>	All	1, 2, 3		-100	μA
Off-state output current	I _{OZH}	V _{CC} = 5.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, V _O = W.4 V <u>2/</u>	All	1, 2, 3		100	μA
Supply current	I _{CC}	V _{CC} = 5.5 V	01-04, 07- 10	1, 2, 31		185	mA
			5			225	
			6			240	
			11			105	
			12-14			95	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions T _C = -55°C to +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay data input to output	t _{PHL}	V _{CC} = 5.0 V, C _L = 50 pF ±10% R ₁ = 390Ω, R ₂ = 750Ω	01, 03, 04, 05, 06	9, 10, 11		45	ns
			07, 09, 10			30	
			11, 13, 14			50	
Propagation delay data input to output	t _{PLH}		01, 03, 04, 05, 06	9, 10, 11		45	ns
			07, 09, 10			30	
			11, 13, 14			50	
Propagation delay output high impedance to output high <u>1/</u>	t _{PZH}		01, 03, 04, 05, 06, 11, 13, 14	9, 10, 11		45	ns
			07, 09, 10			30	
Propagation delay output high impedance to output low	t _{PZL}		01, 03, 04, 05, 06, 11, 13, 14	9, 10, 11		45	ns
		07, 09, 10			30		
Propagation delay output high to output high impedance <u>1/</u>	t _{PHZ}	01, 03, 04, 05, 06, 11, 13, 14	9, 10, 11		45	ns	
		07, 09, 10			30		
Propagation delay output low to output high impedance	t _{PLZ}	01, 03, 04, 05, 06, 11, 13, 14	9, 10, 11		45	ns	
		07, 09, 10			30		
Propagation delay high impedance to output high (pin 11 to output enable) <u>1/</u> , <u>4/</u>	t _{PZH}	02, 03, 04, 05, 06, 08, 09, 10, 12, 13, 14	9, 10, 11		25	ns	
Propagation delay high impedance to output low (pin 11 to output enable) <u>4/</u>	t _{PZL}	02, 03, 04, 05, 06, 08, 09, 10, 12, 13, 14	9, 10, 11		25	ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions T _C = -55°C to +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay output high to high impedance (pin 11 to output disable) <u>1/ 4/</u>	t _{PHZ}	V _{CC} = 5.0 V, C _L = 50 pF ±10% R ₁ = 390Ω, R ₂ = 750Ω	02, 03, 04, 05, 06, 08, 09, 10, 12, 13, 14	9, 10, 11		25	ns
Propagation delay output low to high impedance (pin 11 to output disable) <u>4/</u>	t _{PLZ}		02, 03, 04, 05, 06, 08, 09, 10, 12, 13, 14	9, 10, 11		25	ns
Clock pulse width	t _{P(CL)}		02, 03, 04, 05, 06, 12, 13, 14	9, 10, 11	25		ns
			08, 09, 10		20		
Setup time	t _{SU}		02, 03, 04	9, 10, 11	45		ns
			05, 06		55		
		08, 09, 10	30				
		12, 13, 14	50				
Hold time	t _H	02, 03, 04, 08, 09, 10, 12, 13, 14	9, 10, 11	0		ns	
Maximum clock frequency <u>5/</u>	f _{MAX}	02, 03, 04, 12, 13, 14	9, 10, 11	14		Mhz	
		05, 06		12			
		08, 09, 10		20			

1/ Not tested directly, but guaranteed.

2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZX}.

3/ Only one output shorted at a time.

4/ Test applies only to register outputs. Output disable times may be tested with C_L = 5 pF.

5/ Tested only initially and after any design or process changes.

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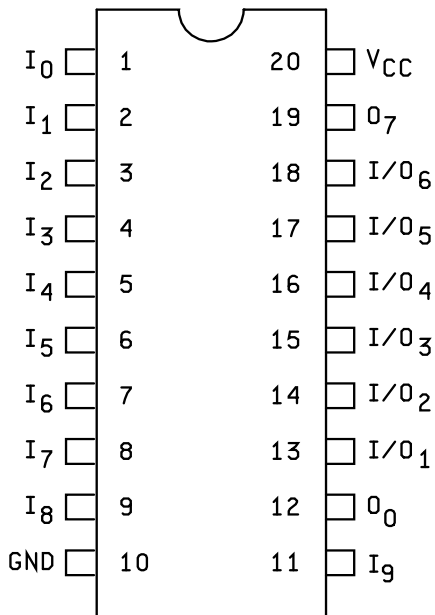
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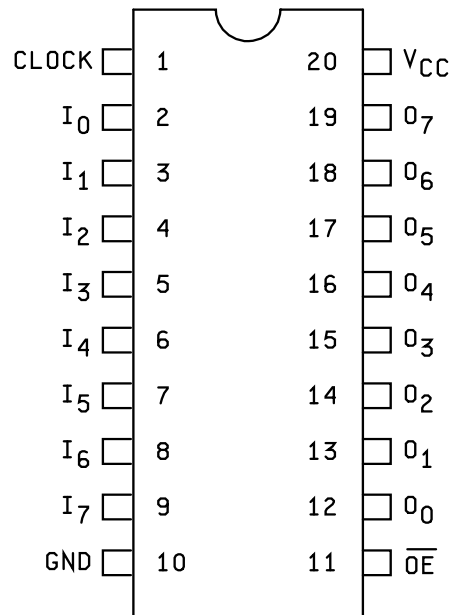
DEVICE TYPES 01,07, AND 11

CASE R AND S



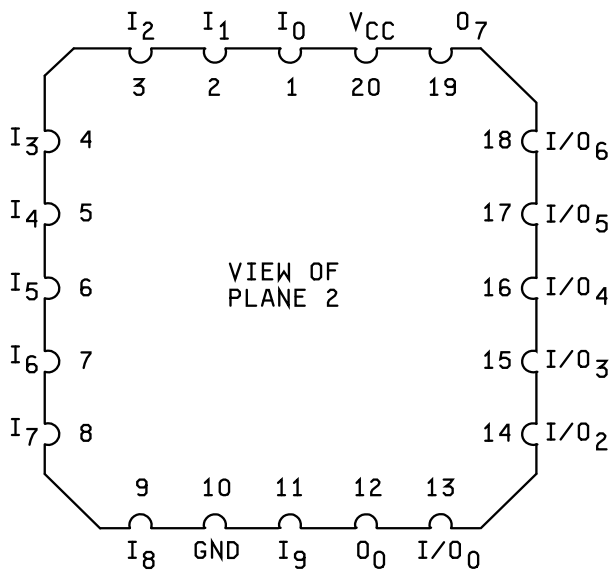
DEVICE TYPES 02,08, AND 12

CASE R AND S



DEVICE TYPES 01,07, AND 11

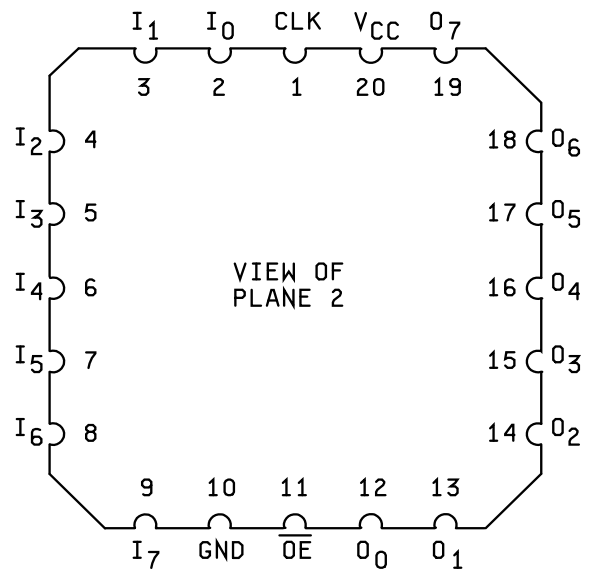
CASE 2



OPTION A WITH ACTIVE
TERMINALS ON PLANE 1.

DEVICE TYPES 02,08, AND 12

CASE 2



OPTION A WITH ACTIVE
TERMINALS ON PLANE 1.

FIGURE 1. Terminal connections.

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SIZE
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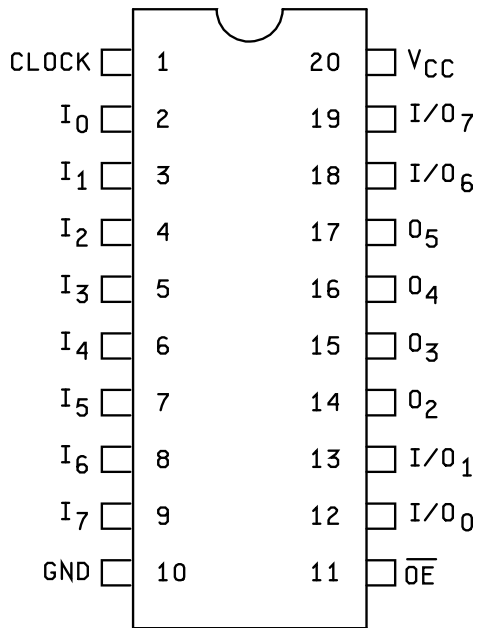
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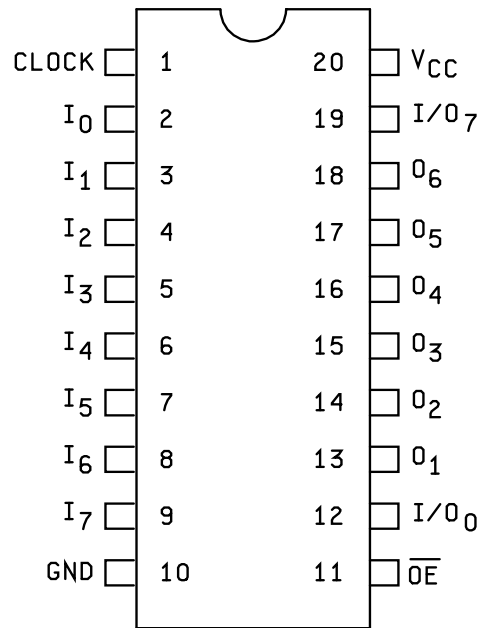
DEVICE TYPES 03,09, AND 13

CASE R AND S



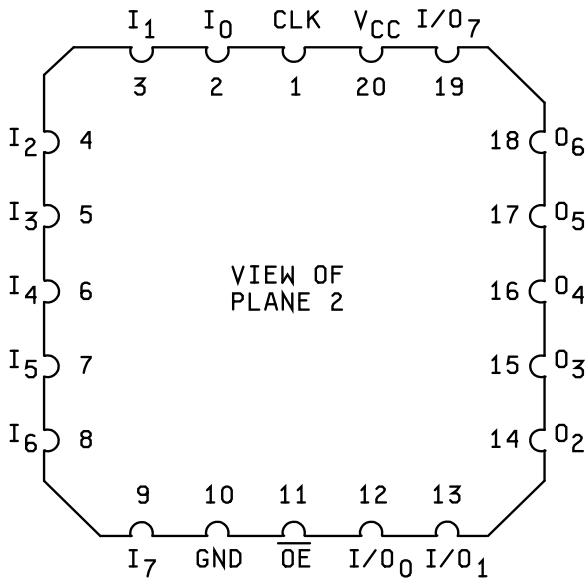
DEVICE TYPES 04,10, AND 14

CASE R AND S



DEVICE TYPES 03,09, AND 13

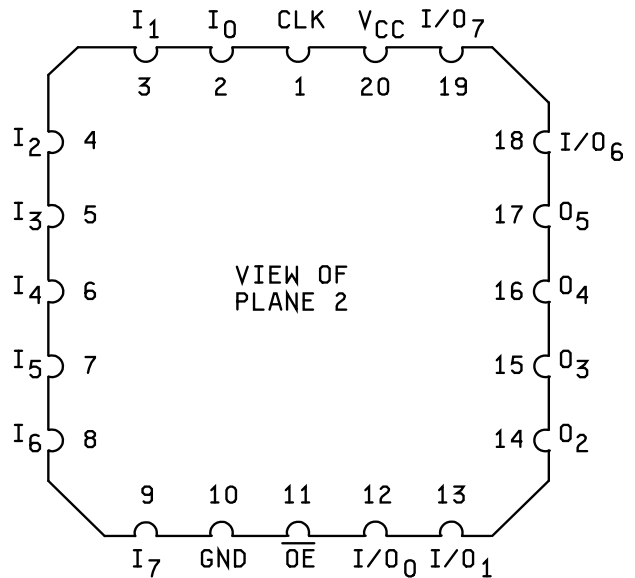
CASE 2



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

DEVICE TYPES 04,10, AND 14

CASE 2



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

FIGURE 1. Terminal Connections - Continued.

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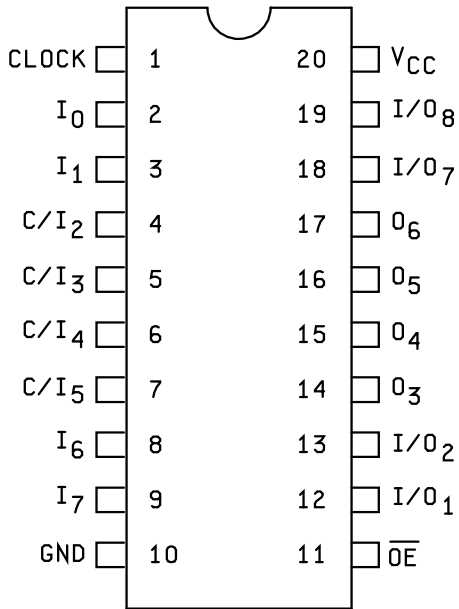
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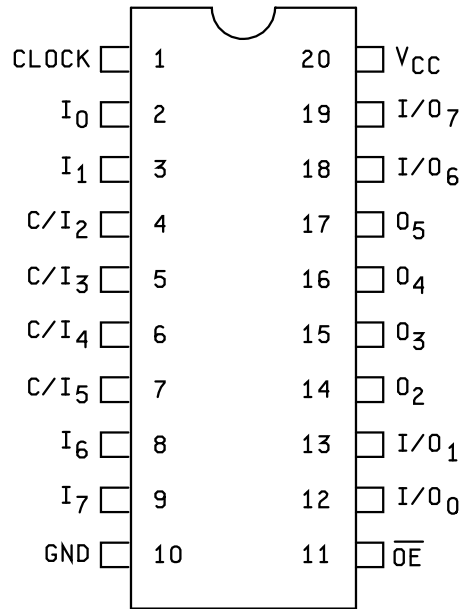
DEVICE TYPE 05

CASE R



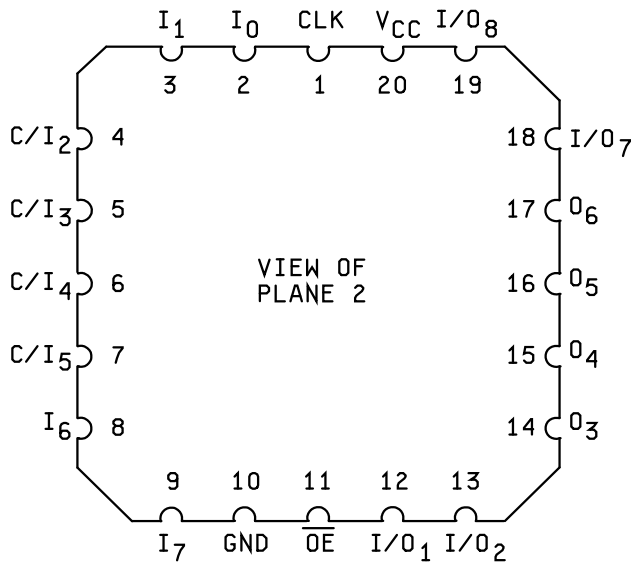
DEVICE TYPE 06

CASE R



DEVICE TYPES 05

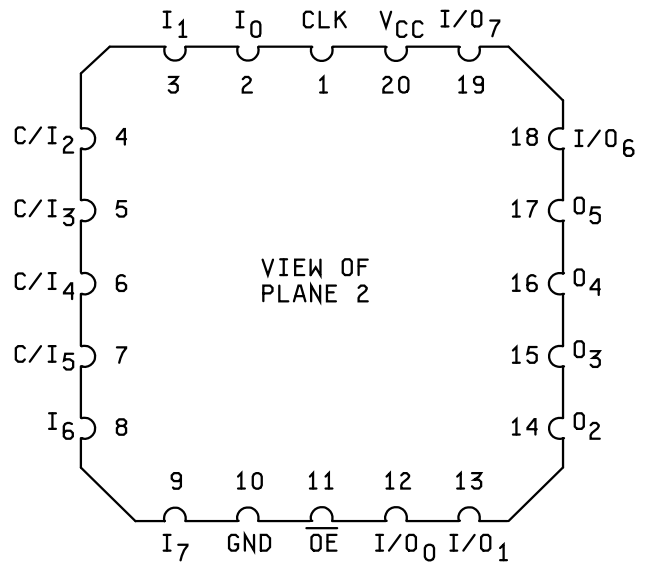
CASE 2



OPTION A WITH ACTIVE
TERMINALS ON PLANE 1.

DEVICE TYPES 06

CASE 2



OPTION A WITH ACTIVE
TERMINALS ON PLANE 1.

FIGURE 1. Terminal Connections - Continued.

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Device types 01 through 14

TRUTH TABLE																				
ADDRESS												OUTPUT LEVEL								
CLK	\overline{OE}	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀	DEVICE
--	--	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	01,07,11
CLK	L	--	--	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	02,08,12
CLK	L	--	--	X	X	X	X	X	X	X	X	Z	H	H	H	H	H	H	Z	03,09,13
CLK	L	--	--	X	X	X	X	X	X	X	X	Z	Z	H	H	H	H	Z	Z	04,05,06,10, 14

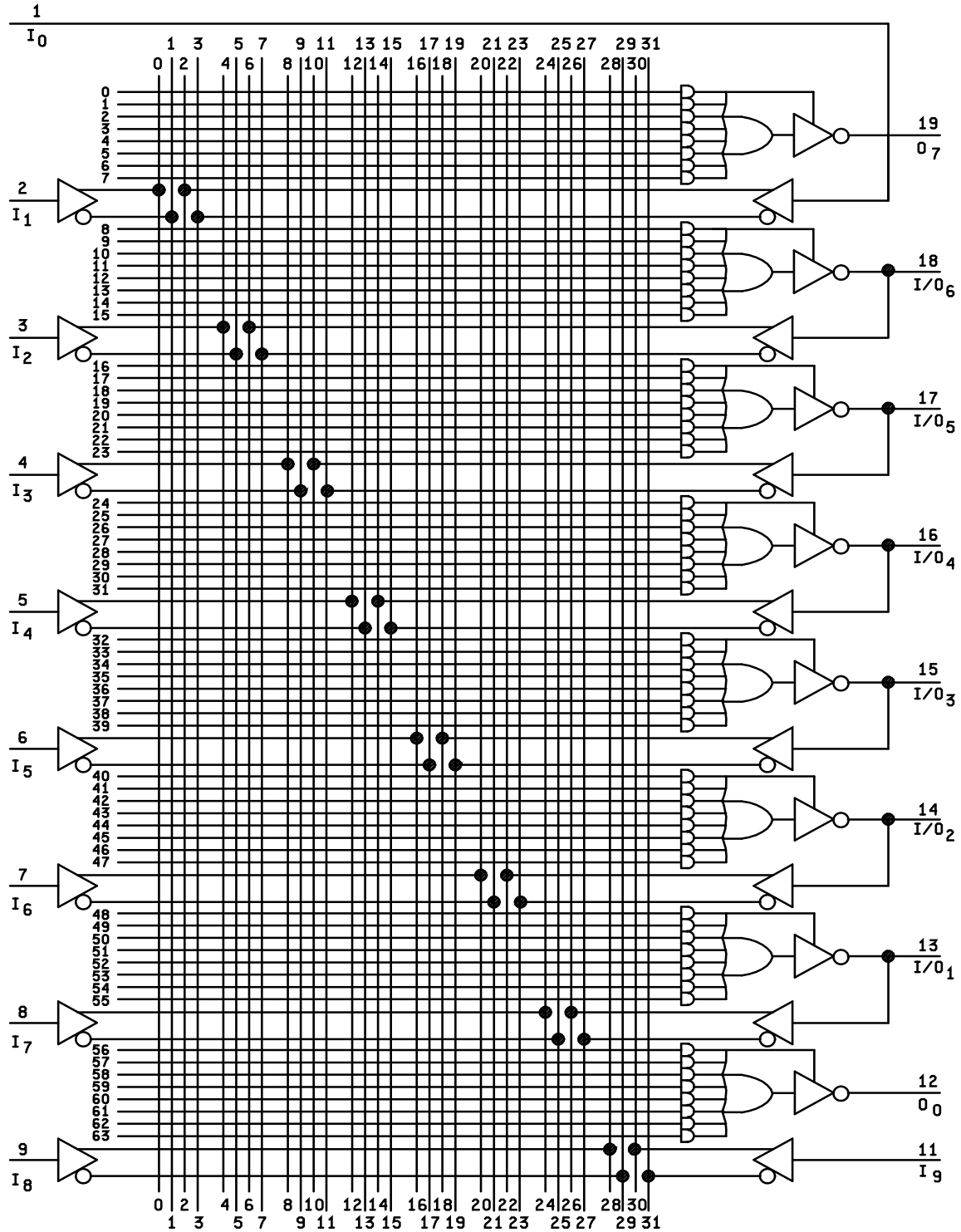
NOTES:

1. Z = tristate
2. Clock (pin 1) - low to high transition required to obtain valid data after last address transition.
3. Enable (pin 11) - must be low to enable output.

FIGURE 2. Truth table (unprogrammed).

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DEVICE TYPES 01, 07, AND 11



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram.

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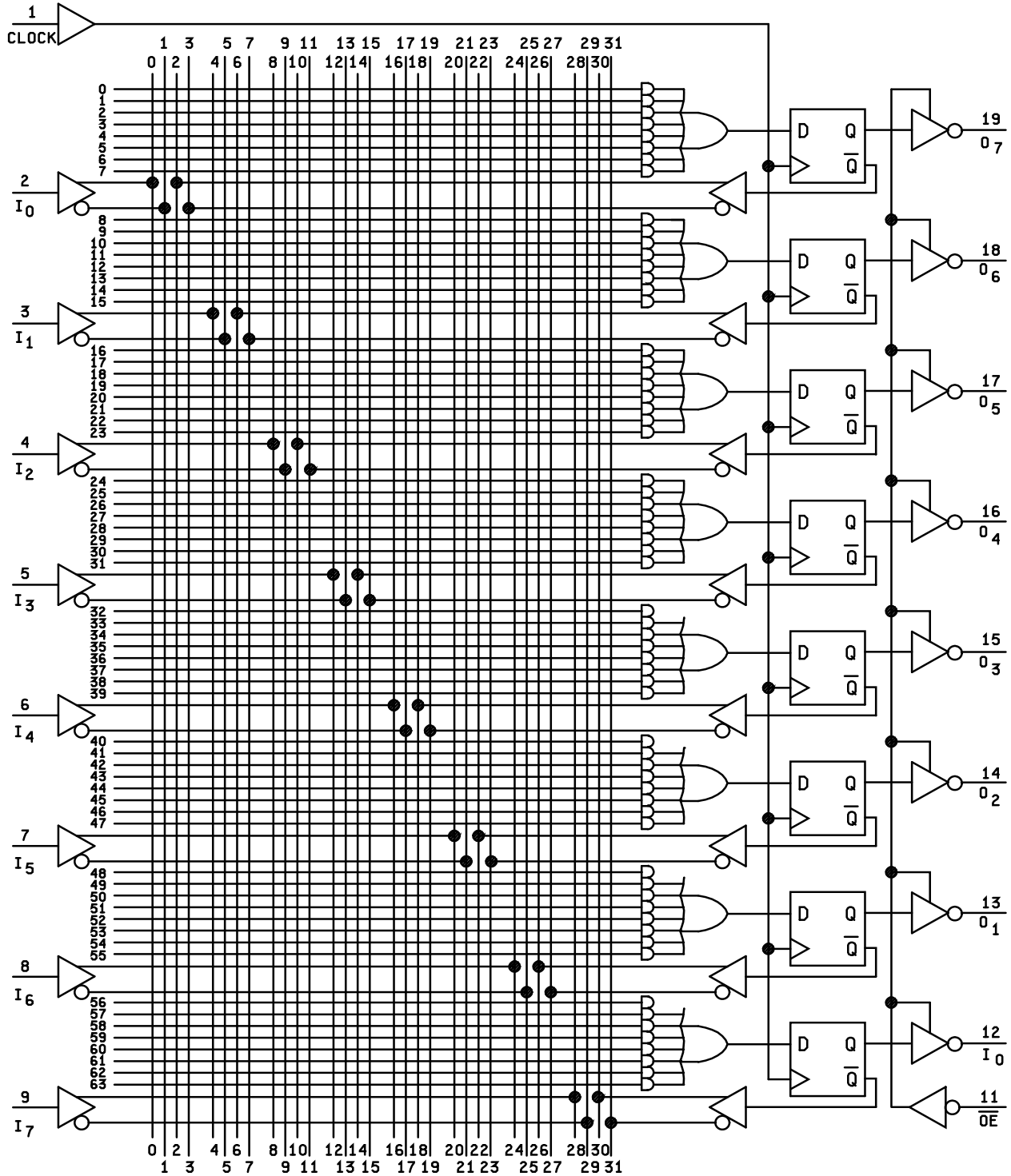
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DEVICE TYPES 02,08, AND 12



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

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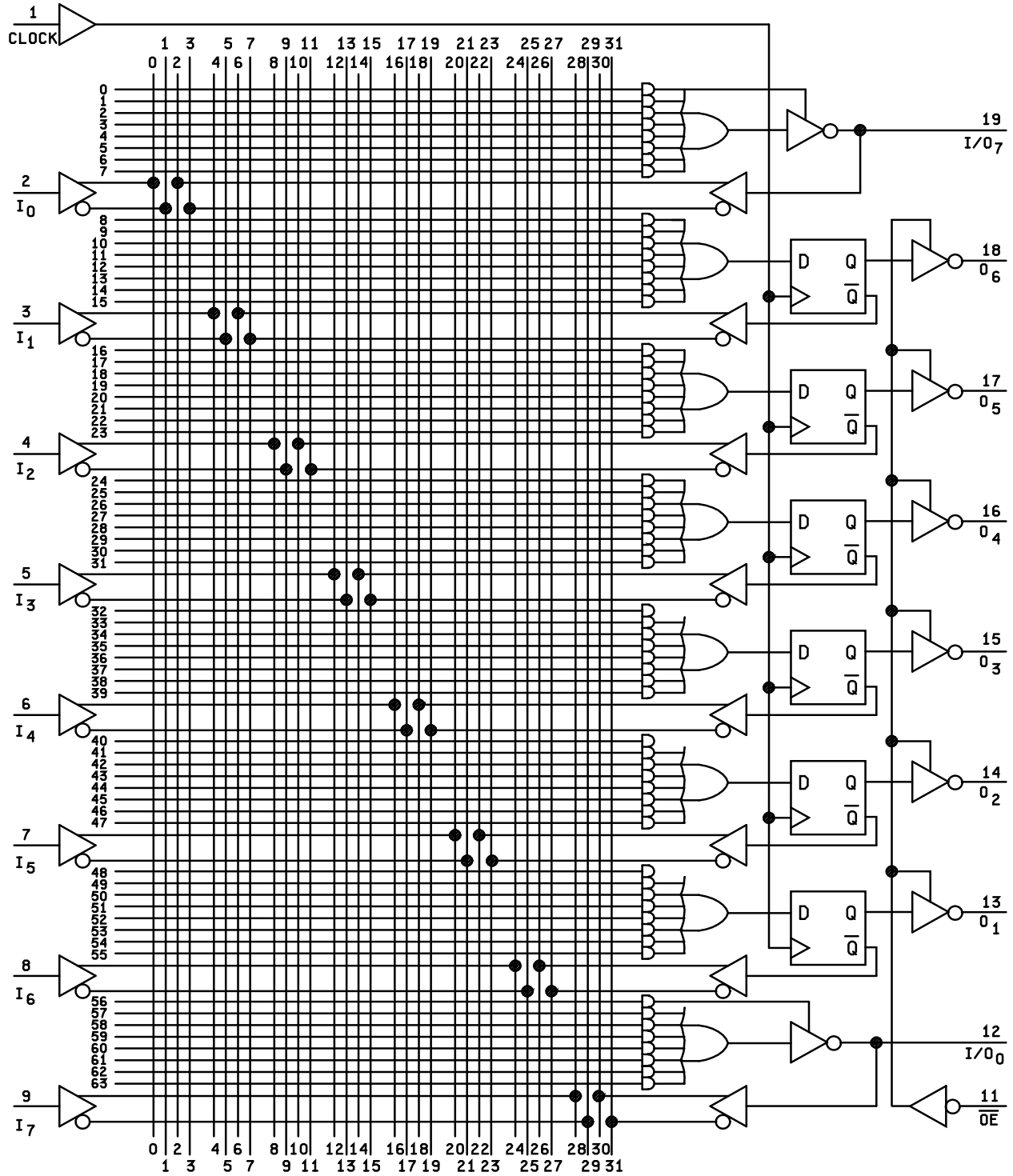
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DEVICE TYPES 03,09, AND 13



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

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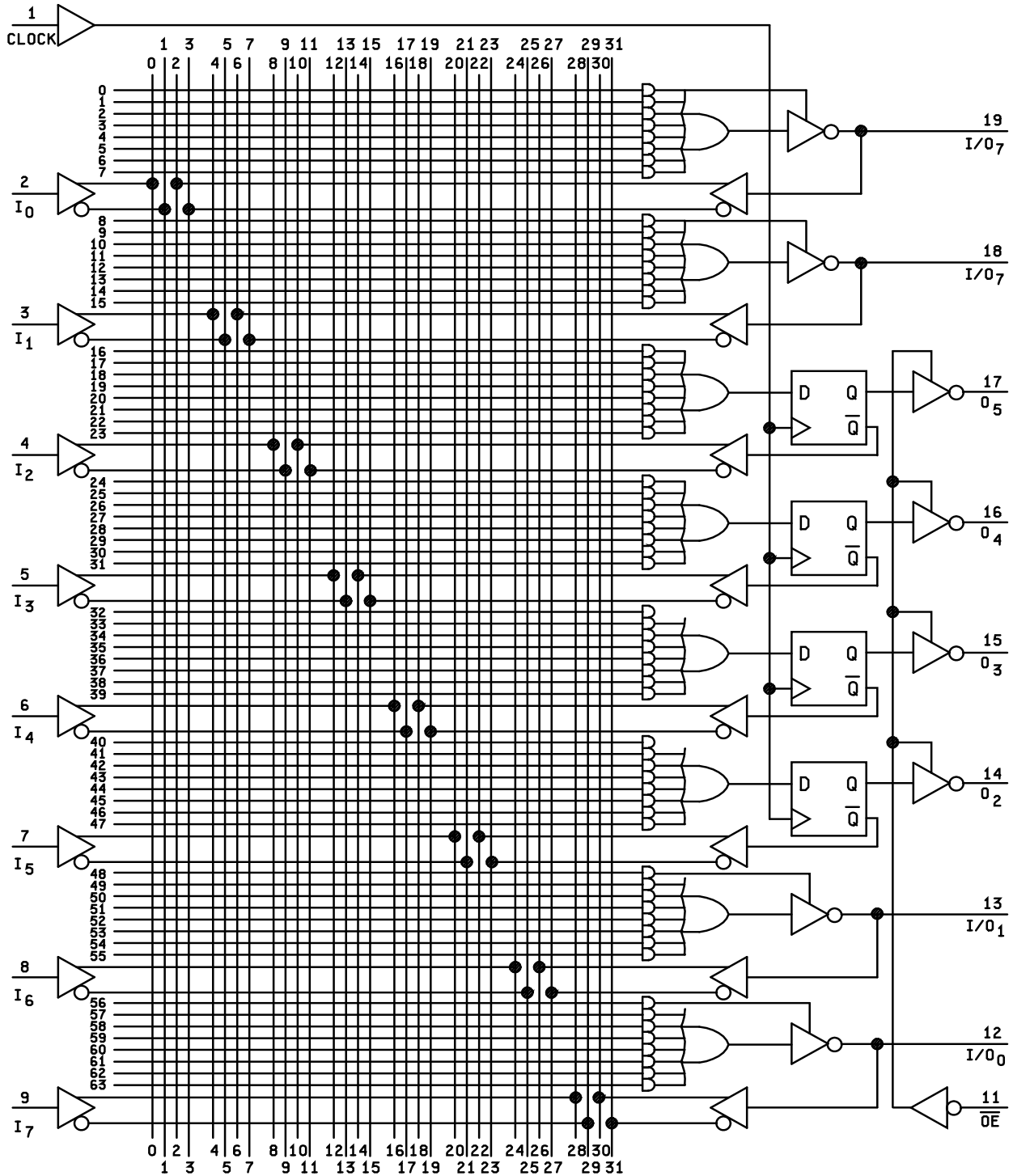
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DEVICE TYPES 04, 10, AND 14



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

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DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

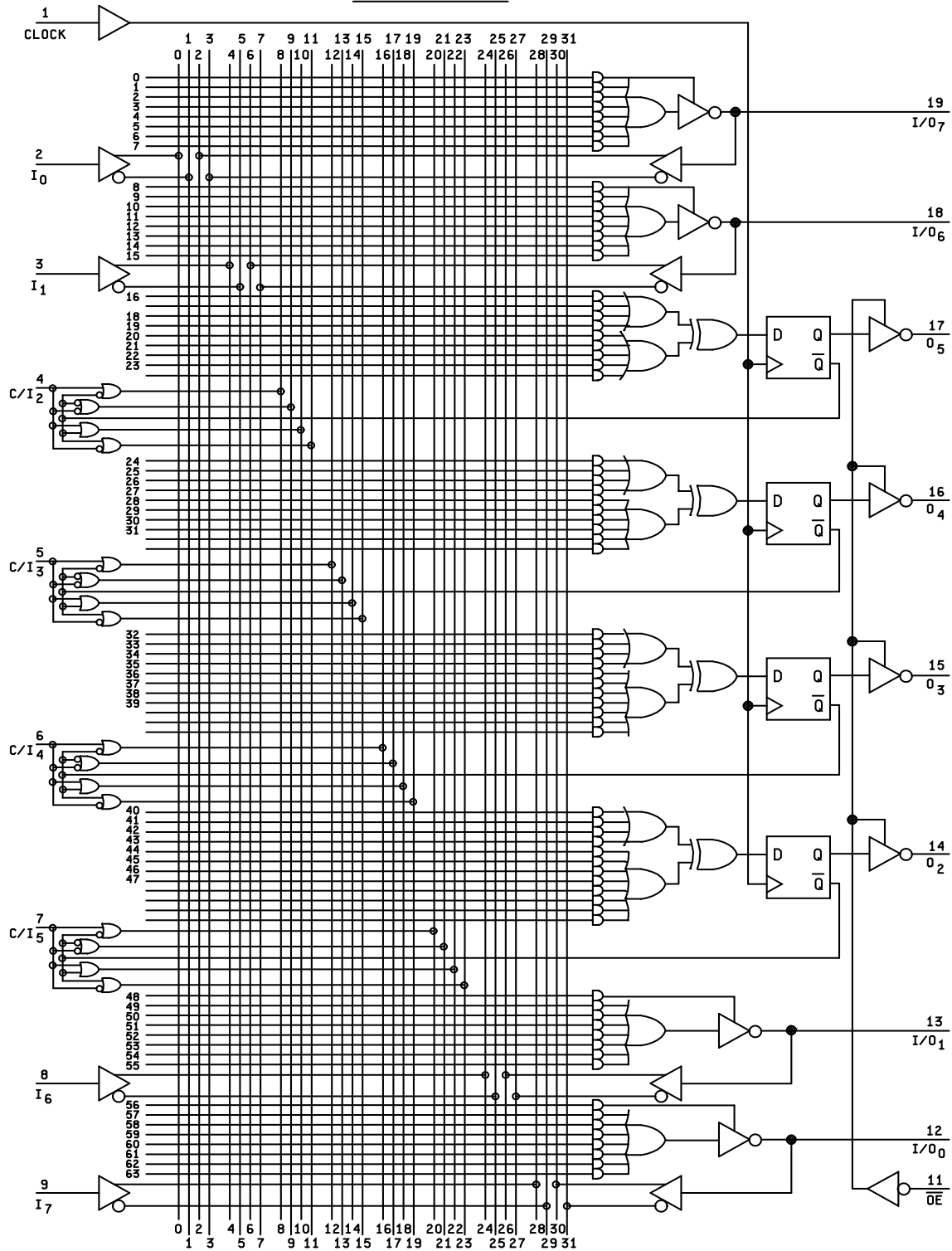
SIZE
A

81036

REVISION LEVEL
N

SHEET
15

DEVICE TYPE 05



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

**STANDARD
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME
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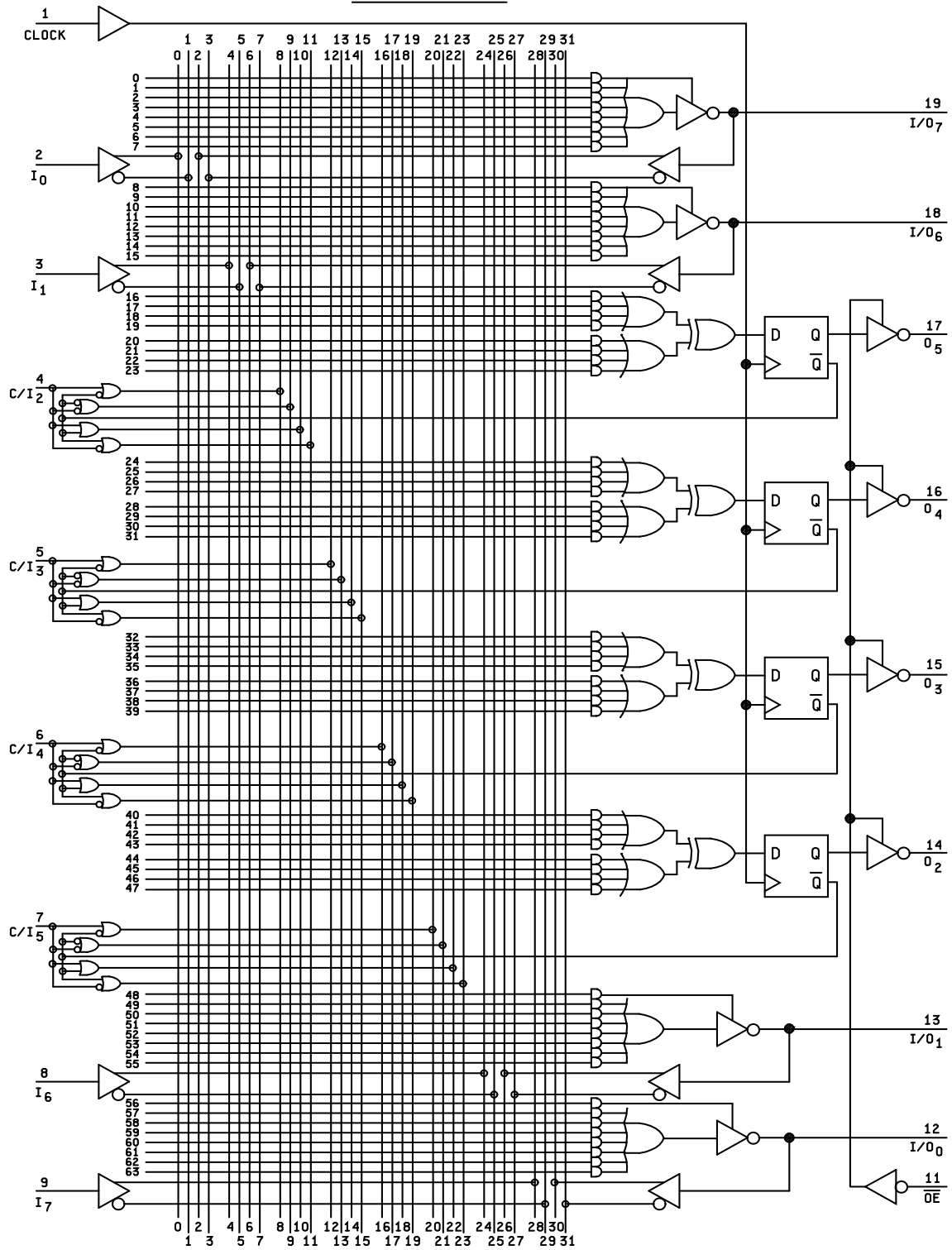
SIZE
A

81036

REVISION LEVEL
N

SHEET
16

DEVICE TYPE 06



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

**STANDARD
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME
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SIZE
A

81036

REVISION LEVEL
N

SHEET
17

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9
Groups C and D end-point electrical parameters (method 5005)	1
Additional electrical subgroups for group C periodic inspections	10, 11

1/ * Indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall include verification of the truth table.
- d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroup 9. Either of two techniques is acceptable:
 - (1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroup 9, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.
 - (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroup 9. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowable.

Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-12-13

Approved sources of supply for SMD 81036 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: <https://landandmaritimeapps.dla.mil/programs/smcr/>

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /	Reference military specification part number
8103601RA <u>3</u> /	<u>4</u> / <u>4</u> / <u>4</u> /	AMPAL16L8/BRA PAL16L8J/883	M38510/50401BRA
81036012A	<u>4</u> / <u>4</u> /	AMPAL16L8/B2A	M38510/50401B2A
8103602RA <u>3</u> /	<u>4</u> / <u>4</u> / <u>4</u> /	AMPAL16R8/BRA PAL16R8J/883	M38510/50402BRA
81036022A	<u>4</u> / <u>4</u> /	AMPAL16R8/B2A	M38510/50402B2A
8103603RA <u>3</u> /	<u>4</u> / <u>4</u> / <u>4</u> /	AMPAL16R6/BRA PAL16R6J/883	M38510/50403BRA
81036032A	<u>4</u> / <u>4</u> /	AMPAL16R6/B2A	M38510/50403B2A
8103604RA <u>3</u> /	<u>4</u> / <u>4</u> / <u>4</u> /	AMPAL16R4/BRA PAL16R4J/883	M38510/50404BRA
81036042A	<u>4</u> / <u>4</u> /	AMPAL16R4/B2A	M38510/50404B2A
8103605RA	<u>4</u> / <u>4</u> /	PAL16X4MJ883B	M38510/50405BRA
81036052A	<u>4</u> / <u>4</u> /	PAL16X4ML883B	M38510/50405B2A
8103606RA	<u>4</u> / <u>4</u> /	PAL16A4MJ883B	M38510/50406BRA
81036062A	<u>4</u> / <u>4</u> /	PAL16A4ML883B	M38510/50406B2A
8103607RA <u>3</u> /	<u>4</u> / <u>4</u> / 01295 <u>4</u> / <u>4</u> /	PAL16L8AMJ/883B AMPAL16L8A/BRA PAL16L8AMJB PAL16L8AJ/883	M38510/50401BRA
81036072A	<u>4</u> / <u>4</u> / 01295	PAL16L8AML/883B AMPAL16L8A/B2A PAL16L8AMFKB	M38510/50401B2A
8103607SA	<u>4</u> / <u>4</u> / 01295	PAL16L8AMW/883B AMPAL16L8A/BSA PAL16L8AMWB	
8103608RA <u>3</u> /	<u>4</u> / <u>4</u> / 01295 <u>4</u> / <u>4</u> /	PAL16R8AMJ/883B AMPAL16R8A/BRA PAL16R8AMJB PAL16R8AJ/883	M38510/50402BRA
81036082A	<u>4</u> / <u>4</u> / 01295	PAL16R8AML/883B AMPAL16R8A/B2A PAL16R8AMFKB	M38510/50402B2A

See footnotes at end of listing.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 17-12-13

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /	Reference military specification part number
8103608SA	<u>4</u> / <u>4</u> / <u>4</u> /	PAL16R8AMW/883B AMPAL16R8A/BSA PAL16R8AMWB	
8103609RA <u>3</u> /	<u>4</u> / <u>4</u> / 01295 <u>4</u> /	PAL16R6AMJ/883B AMPAL16R6A/BRA PAL16R6AMJB PAL16R6AJ/883	M38510/50403BRA
81036092A	<u>4</u> / <u>4</u> / 01295	PAL16R6AML/883B AMPAL16R6A/B2A PAL16R6AMFKB	M38510/50403B2A
8103609SA	<u>4</u> / <u>4</u> / <u>4</u> /	PAL16R6AMW/883B AMPAL16R6A/BSA PAL16R6AMWB	
8103610RA <u>3</u> /	<u>4</u> / <u>4</u> / 01295 <u>4</u> /	PAL16R4AMJ/883B AMPAL16R4A/BRA PAL16R4AMJB PAL16R4AJ/883	M38510/50404BRA
81036102A	<u>4</u> / <u>4</u> / 01295	PAL16R4AML/883B AMPAL16R4A/B2A PAL16R4AMFKB	M38510/50404B2A
8103610SA	<u>4</u> / <u>4</u> / 01295	PAL16R4AMW/883B AMPAL16R4A/BSA PAL16R4AMWB	
8103611RA	<u>4</u> / 01295 <u>4</u> /	PAL16L8A-2MJ/883B PAL16L8A-2MJB AMPAL16L8L/BRA	M38510/50407BRA
81036112A	<u>4</u> / 01295 <u>4</u> /	PAL16L8A-2ML/883B PAL16L8A-2MFKB AMPAL16L8L/B2A	M38510/50407B2A
8103611SA	<u>4</u> / <u>4</u> / <u>4</u> /	PAL16L8A-2MW/883B AMPAL16L8L/BSA PAL16L8A-2MWB	
8103612RA	<u>4</u> / <u>4</u> / <u>4</u> /	PAL16R8A-2MJ/883B PAL16R8A-2MJB AMPAL16R8L/BRA	M38510/50408BRX
81036122A	<u>4</u> / <u>4</u> / <u>4</u> /	PAL16R8A-2ML/883B PAL16R8A-2MFKB AMPAL16R8L/B2A	M38510/50408B2A
8103612SA	<u>4</u> / <u>4</u> / <u>4</u> /	PAL16R8A-2MW/883B AMPAL16R8L/BSA PAL16R8A-2MWB	
8103613RA <u>3</u> /	<u>4</u> / <u>4</u> / <u>4</u> /	PAL16R6A-2MJ/883B PAL16R6A-2MJB AMPAL16R6L/BRA	M38510/50409BRA

See footnotes at end of listing.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 17-12-13

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification part number
81036132A	<u>4/</u> <u>4/</u> <u>4/</u>	PAL16R6A-2ML/883B PAL16R6A-2MFKB AMPAL16R6L/B2A	M38510/50409B2A
8103613SA	<u>4/</u> <u>4/</u> <u>4/</u>	PAL16R6A-2MW/883B AMPAL16R6L/BSA PAL16R6A-2MWB	
8103614RA <u>3/</u>	<u>4/</u> 01295 <u>4/</u>	PAL16R4A-2MJ/883B PAL16R4A-2MJB AMPAL16R4L/BRA	M38510/50410BRA
81036142A	<u>4/</u> 01295 <u>4/</u>	PAL16R4A-2ML/883B PAL16R4A-2MFKB AMPAL16R4L/B2A	M38510/50410B2A
8103614SA	<u>4/</u> <u>4/</u> <u>4/</u>	PAL16R4A-2MW/883B AMPAL16R4L/BSA PAL16R4A-2MWB	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Inactive for new design for the R case outline only. Use applicable QML M38510 device.

4/ Not available from an approved source of supply.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>	<u>Fusible link</u>
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Ln P.O. Box 660199 Dallas, TX 75243	Titanium-tungsten

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.