REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, minimum pulse width changed to 30 ns @ -55°C, +125°C.	84-09-04	N. A. Hauck
B	Add vendor CAGE 27014. Inactivate device 01DX for new design. Delete vendor CAGE 07263. Editorial changes throughout.	86-03-03	M. A. Frye
C	Add vendor CAGE 18714. Delete vendor CAGE 31019 and 27014. Technical changes in 1.3 and table I. Change drawing CAGE code to 67268. Change to military drawing format. Editorial changes throughout.	89-06-07	M. A. Frye
D	Add vendor CAGE 27014. Change vendor CAGE 18714 to 34371. Add device type 02. Technical and editorial changes throughout.	92-02-06	M. A. Frye
E	Change I_{DD} for device type 01. Change input capacitance C_{IN}. Editorial changes throughout.	94-12-12	Monica L. Poelking
F	Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak	06-10-16	Thomas M. Hess
G	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	13-11-22	Thomas M. Hess
H	Update boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - TTM	20-12-21	Muhammad A. Akbar

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			H	H	H	H	H	H	H	H	H	H	H	H		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Herbert L. Baker

CHECKED BY
Darrell Hill

APPROVED BY
C. R. Jackson

DRAWING APPROVAL DATE
82-02-24

REVISION LEVEL
H

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, MONOSTABLE/ASTABLE MULTIVIBRATOR, MONOLITHIC SILICON

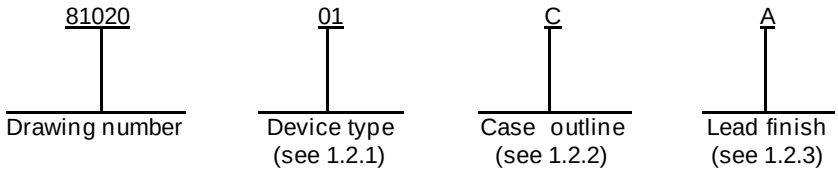
SIZE	CAGE CODE	
A	**14933**	**81020**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4047B	Monostable/Astable multivibrator
02	4047B	Monostable/Astable multivibrator

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}):
Device type 01 ..... -0.5 V dc to +20 V dc
Device type 02 ..... -0.5 V dc to +18 V dc
Input voltage range (V_{IN}) ..... -0.5 V dc to V_{DD} + 0.5 V dc
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW 2/
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}):
Device type 01 ..... +3.0 V dc to +18 V dc
Device type 02 ..... +3.0 V dc to +15 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C to 200 mW.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
Quiescent supply current	I_{DD}	V_{IN} = 0.0 V or V_{DD} 1/	01	5 V	1, 3		1.0	µA
					2		30	
			02		1, 3		5.0	
					2		150	
		V_{IN} = 0.0 V or V_{DD} 1/	01	10 V	1, 3		2.0	
					2		60	
			02		1, 3		10	
					2		300	
		V_{IN} = 0.0 V or V_{DD} 1/	01	15 V	1, 3		4.0	
					2		120	
			02		1, 3		20	
					2		600	
		V_{IN} = 0.0 V or V_{DD} 2/	01	20 V	1, 3		20	
					2		600	
			02		1, 3		100	
					2		3000	
Low level output voltage	V_{OL}	V_{IN} = 0.0 V or V_{DD} 1/ I_{OL} = +1µA	All	5 V	1, 2, 3		0.05	V
		V_{IN} = 0.0 V or V_{DD} 1/ I_{OL} = +1µA	All	10 V	1, 2, 3		0.05	
		V_{IN} = 0.0 V or V_{DD} I_{OL} = +1µA	All	15 V	1, 2, 3		0.05	
High level output voltage	V_{OH}	V_{IN} = 0.0 V or V_{DD} 1/ I_{OH} = -1µA	All	5 V	1, 2, 3	4.95		V
		V_{IN} = 0.0 V or V_{DD} 1/ I_{OH} = -1µA	All	10 V	1, 2, 3	9.95		
		V_{IN} = 0.0 V or V_{DD} I_{OH} = -1µA	All	15 V	1, 2, 3	14.95		
Low level input voltage	V_{IL}	V_O = 0.5 V or 4.5 V	All	5 V	1, 2, 3		1.5	V
		V_O = 1.0 V or 9.0 V 1/	All	10 V	1, 2, 3		3.0	
		V_O = 1.5 V or 13.5 V	All	15 V	1, 2, 3		4.0	
High level input voltage	V_{IH}	V_O = 0.5 V or 4.5 V	All	5 V	1, 2, 3	3.5		V
		V_O = 1.0 V or 9.0 V 1/	All	10 V	1, 2, 3	7.0		
		V_O = 1.5 V or 13.5 V	All	15 V	1, 2, 3	11		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
Input current	I_{IN} 2/	V_{IN} = 0.0 V or V_{DD}	All	20 V	1, 3		±0.1	µA
					2		±1.0	
Low level output current	I_{OL} 3/	V_O = 0.4 V	All	5 V	1	0.51		mA
					2	0.36		
					3	0.64		
		V_O = 0.5 V	All	10 V	1	1.3		
					2	0.9		
					3	1.6		
		V_O = 1.5 V	All	15 V	1	3.4		
					2	2.4		
					3	4.2		
High level output current	I_{OH} 3/	V_O = 4.6 V	All	5 V	1	-0.51		mA
					2	-0.36		
					3	-0.64		
		V_O = 2.5 V	01	5 V	1	-1.6		
					2	-1.15		
					3	-2.0		
		V_O = 9.5 V	All	10 V	1	-1.3		
					2	-0.9		
					3	-1.60		
		V_O = 13.5 V	All	15 V	1	-3.4		
					2	-2.4		
					3	-4.2		
Input capacitance	C_{IN}	V_{IN} = 0.0 V, T_C = +25°C See 4.3.1c	01		4		7.7	pF
			02				7.5	
Functional test		See 4.3.1d	All		7, 8			
Pulse width (any input)	t_w 1/	R_L = 200 kΩ C_L = 50 pF minimum $t_r = t_f$ = 20 ns	01	5 V	9	1000		ns
					10, 11	1500		
			02		9	1000		
					10, 11	1500		
			01	10 V	9	230		
					10, 11	311		
			02		9	400		
					10, 11	400		
			01	15 V	9	160		
					10, 11	225		
			02		9	320		
					10, 11	320		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
Transition time	t_{THL}, t_{TLH}	R_L = 200 kΩ C_L = 50 pF minimum $t_r = t_f$ = 20 ns	01	5 V	9	10	200	ns
					10, 11	15	300	
			02		9	10	200	
					10, 11	15	300	
			01	10 V 1/	9	2.0	100	
					10, 11	2.0	150	
			02		9	2.0	100	
					10, 11	2.0	150	
			01	15 V 1/	9	2.0	80	
					10, 11	2.0	120	
			02		9	2.0	80	
					10, 11	2.0	120	
Propagation delay time, ASTABLE to OSC out, $\overline{\text{ASTABLE}}$ to OSC out	t_{PHL1}, t_{PLH1}	R_L = 200 kΩ C_L = 50 pF minimum $t_r = t_f$ = 20 ns	01	5 V	9	20	400	ns
					10, 11	30	600	
			02		9	20	400	
					10, 11	30	600	
			01	10 V 1/	9	2.0	200	
					10, 11	2.0	270	
			02		9	2.0	200	
					10, 11	2.0	280	
			01	15 V 1/	9	2.0	160	
					10, 11	2.0	216	
			02		9	2.0	160	
					10, 11	2.0	225	
Propagation delay time, ASTABLE to Q, ASTABLE to $\overline{Q}$, $\overline{\text{ASTABLE}}$ to Q, $\overline{\text{ASTABLE}}$ to $\overline{Q}$	t_{PHL2}, t_{PLH2}	R_L = 200 kΩ C_L = 50 pF minimum $t_r = t_f$ = 20 ns	01	5 V	9	45	900	ns
					10, 11	68	1350	
			02		9	45	900	
					10, 11	68	1350	
			01	10 V 1/	9	2.0	350	
					10, 11	2.0	473	
			02		9	2.0	500	
					10, 11	2.0	700	
			01	15 V 1/	9	2.0	250	
					10, 11	2.0	338	
			02		9	2.0	400	
					10, 11	2.0	560	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay time, +TRIGGER to Q, + TRIGGER to $\overline{Q}$, - TRIGGER to Q, - TRIGGER to $\overline{Q}$	t_{PHL3}, t_{PLH3}	R_L = 200 kΩ C_L = 50 pF minimum $t_r = t_f$ = 20 ns	01	5 V	9	60	1200	ns
					10, 11	90	1800	
			02		9	60	1200	
					10, 11	90	1800	
			01	10 V 1/	9	2.0	450	
					10, 11	2.0	608	
			02		9	2.0	600	
					10, 11	2.0	840	
			01	15 V 1/	9	2.0	300	
					10, 11	2.0	405	
			02		9	2.0	480	
					10, 11	2.0	670	
Propagation delay time, RETRIGGER to Q, RETRIGGER to $\overline{Q}$	t_{PHL4}, t_{PLH4}	R_L = 200 kΩ C_L = 50 pF minimum $t_r = t_f$ = 20 ns	01	5 V	9	30	600	ns
					10, 11	45	900	
			02		9	30	600	
					10, 11	45	900	
			01	10 V 1/	9	2.0	300	
					10, 11	2.0	405	
			02		9	2.0	300	
					10, 11	2.0	420	
			01	15 V 1/	9	2.0	200	
					10, 11	2.0	270	
			02		9	2.0	250	
					10, 11	2.0	350	
Propagation delay time, EXTERNAL RESET to Q, EXTERNAL RESET to $\overline{Q}$	t_{PHL5}, t_{PLH5}	R_L = 200 kΩ C_L = 50 pF minimum $t_r = t_f$ = 20 ns	01	5 V	9	30	600	ns
					10, 11	45	900	
			02		9	30	600	
					10, 11	45	900	
			01	10 V 1/	9	2.0	200	
					10, 11	2.0	270	
			02		9	2.0	250	
					10, 11	2.0	350	
			01	15 V 1/	9	2.0	140	
					10, 11	2.0	189	
			02		9	2.0	200	
					10, 11	2.0	280	

1/ Guaranteed, if not tested, to the specified limits in table I.

2/ At T_C = -55°C, test is performed with V_{DD} = 18 V.

3/ The I_{OL} and I_{OH} tests are tested 100 percent at T_C = +25°C and are guaranteed, if not tested, for T_C = -55°C and T_C = +125°C.

Device types	01 and 02
Case outlines	C and D
Terminal number	Terminal symbol
1	C
2	R
3	R C COMMON
4	$\overline{\text{ASTABLE}}$
5	ASTABLE
6	-TRIGGER
7	V_{SS}
8	+TRIGGER
9	EXT. RESET
10	Q
11	$\overline{Q}$
12	RETRIGGER
13	OSC OUT
14	V_{DD}

FIGURE 1. Terminal connections.

Inputs						Function
ASTABLE	$\overline{\text{ASTABLE}}$	+TRIGGER	-TRIGGER	RETRIGGER	RESET	
1	X	0	1	0	0	Astable multivibrator (free running)
X	0	0	1	0	0	Astable multivibrator (free running)
⎍	1	0	1	0	0	Astable multivibrator (true gating)
0	⎍	0	1	0	0	Astable multivibrator (compliment gating)
0	1	⎍	0	0	0	Monostable multivibrator (positive-edge triggering)
0	1	1	⎍	0	0	Monostable multivibrator (negative-edge triggering)
0	1	⎍	0	⎍	0	Monostable multivibrator (retriggering)
X	X	X	X	X	1	Reset

FIGURE 2. Truth table.

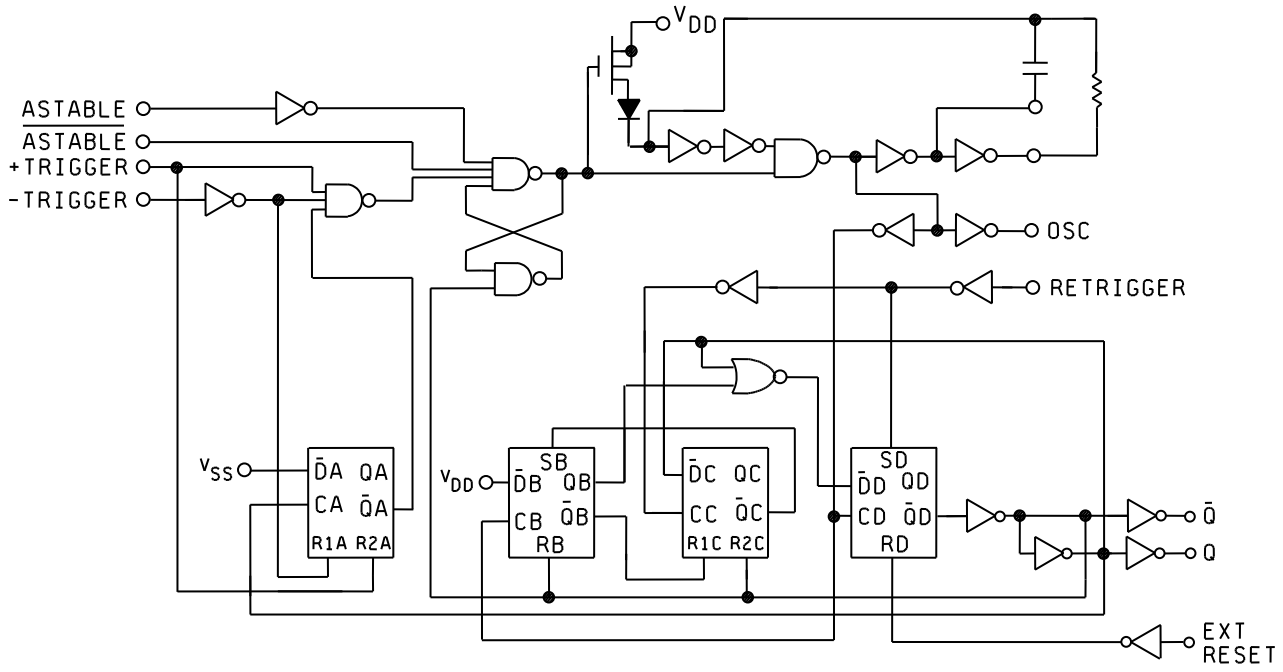


FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and ground at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 tests shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-12-21

Approved sources of supply for SMD 81020 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8102001CA	01295	CD4047BF3A
8102001DA	3/	BCL4047BF/883
8102002CA	3/	CD4047BMJ/883
8102002DA	3/	CD4047BMW/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243