REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Add device type 02, 14035B. Delete vendor CAGE 31019. Add vendors CAGE 04713 and 34371. Technical changes in 1.3, 1.4, tables I and II. Add figures 3 and 4. Editorial changes throughout. - mbk	90-08-10	Michael A. Frye
E	Changes IAW NOR 5962-R012-93. – wlm	92-11-12	Monica L. Poelking
F	Update boilerplate to MIL-PRF-38535 requirements. – jak	01-05-17	Thomas M. Hess
G	Made change to paragraph 3.5. Update boilerplate to MIL-PRF-38535 requirements. – LTG	05-01-13	Thomas M. Hess
H	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	11-07-26	Thomas M. Hess
J	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	18-07-25	Thomas M. Hess
K	Update boilerplate paragraphs and drawing to current MIL-PRF-38535 requirements. –RDC	24-08-20	Muhammad A. Akbar

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			K	K	K	K	K	K	K	K	K	K	K	K	K	K
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
82-02-22

REVISION LEVEL
K

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS 4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**81017**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

81017	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4035B	4-bit parallel-in/parallel-out shift register
02	14035B	4-bit parallel-in/parallel-out shift register

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD}) ..... -0.5 V dc to +20.0 V dc
Input voltage range ..... -0.5 V dc to V_{DD} +0.5 V dc
DC input current ..... ± 10 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW 4/
Lead temperature (soldering, 10 seconds) ..... +265°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to ground.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C to 200 mW.

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) ..... +3.0 V dc to +18.0 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

Minimum setup time, J/$\overline{K}$ inputs, (t_{s1}):

T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 220 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01 ..... 286 ns
T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 500 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 750 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 01 ..... 80 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 01 ..... 104 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 200 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 300 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 01 ..... 60 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 01 ..... 78 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 150 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 225 ns

Minimum setup time, parallel-in lines, (t_{s2}):

T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 140 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01 ..... 182 ns
T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 500 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 750 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 01 ..... 50 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 01 ..... 65 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 200 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 300 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 01 ..... 40 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 01 ..... 52 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 150 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 225 ns

Minimum clock pulse width, (t_{w1}):

T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 200 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01 ..... 260 ns
T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 335 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 502 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 01 ..... 90 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 01 ..... 117 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 165 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 245 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 01 ..... 60 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 01 ..... 78 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 125 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 185 ns

1.4 Recommended operating conditions – Continued.

Minimum RESET pulse width, (t_{w2}):

T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 250 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01 ..... 325 ns
T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 400 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 600 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 01 ..... 110 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 01 ..... 143 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 175 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 262 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 01 ..... 80 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 01 ..... 140 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 130 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 195 ns

Maximum input clock frequency, (f_{MAX}):

T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 2.0 MHz
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01 ..... 2.6 MHz
T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 1.2 MHz
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 1.8 MHz
T_C = +25°C, V_{DD} = 10 V dc, device type 01 ..... 6.0 MHz
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 01 ..... 7.8 MHz
T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 2.0 MHz
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 1.5 MHz
T_C = +25°C, V_{DD} = 15 V dc, device type 01 ..... 8.0 MHz
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 01 ..... 10.4 MHz
T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 3.0 MHz
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 2.25 MHz

Input rise or fall times, (t_r, t_f):

T_C = +25°C, V_{DD} = 5 V dc ..... 15.0 µs
T_C = -55°C, +125°C, V_{DD} = 5 V dc ..... 15.0 µs
T_C = +25°C, V_{DD} = 10 V dc ..... 15.0 µs
T_C = -55°C, +125°C, V_{DD} = 10 V dc ..... 15.0 µs
T_C = +25°C, V_{DD} = 15 V dc ..... 15.0 µs
T_C = -55°C, +125°C, V_{DD} = 15 V dc ..... 15.0 µs

Minimum reset removal time, (t_{rem}):

T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 80 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 120 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 30 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 45 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 25 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 37 ns

Minimum hold time, clock to J-$\overline{K}$ (t_{h1}):

T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 40 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 60 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 30 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 45 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 25 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 37 ns

1.4 Recommended operating conditions – Continued.

Minimum hold time, clock to parallel-in, (t_{h2}):

T_C = +25°C, V_{DD} = 5 V dc, device type 02	90 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02	135 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02	40 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02	60 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02	40 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02	60 ns

Minimum hold time, clock to parallel/serial (t_{h3}):

T_C = +25°C, V_{DD} = 5 V dc, device type 02	30 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02	45 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02	20 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02	30 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02	20 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02	30 ns

Minimum setup time, clock to parallel/serial input (t_{s3}):

T_C = +25°C, V_{DD} = 5 V dc, device type 02	500 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02	750 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02	200 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02	300 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02	150 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02	225 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Quiescent supply current	I_{DD}	V_{IN} = 0.0 V or V_{DD} V_{DD} = 5.0 V 1/		All	1, 3		5.0	µA
					2		150.0	
		V_{IN} = 0.0 V or V_{DD} V_{DD} = 10.0 V 1/		All	1, 3		10.0	
					2		300.0	
		V_{IN} = 0.0 V or V_{DD} V_{DD} = 15.0 V 1/		All	1, 3		20.0	
					2		600.0	
		V_{IN} = 0.0 V or V_{DD} V_{DD} = 20.0 V 2/		All	1, 3		100.0	
					2		3000.0	
Low-level output voltage	V_{OL}	V_{IN} = 0.0 V or V_{DD} I_{OL} = +1 µA	V_{DD} = 5.0 V 3/	All	1, 2, 3		0.05	V
			V_{DD} = 10.0 V 3/	All	1, 2, 3		0.05	
			V_{DD} = 15.0 V	All	1, 2, 3		0.05	
High-level output voltage	V_{OH}	V_{IN} = 0.0 V or V_{DD} I_{OH} = -1 µA	V_{DD} = 5.0 V 3/	All	1, 2, 3	4.95		V
			V_{DD} = 10.0 V 3/	All	1, 2, 3	9.95		
			V_{DD} = 15.0 V	All	1, 2, 3	14.95		
Low-level input voltage	V_{IL}	V_{DD} = 5.0 V V_O = 0.5 V or 4.5 V		All	1, 2, 3		1.5	V
		V_{DD} = 10.0 V V_O = 1.0 V or 9.0 V 3/		All	1, 2, 3		3.0	
		V_{DD} = 15.0 V V_O = 1.5 V or 13.5 V		All	1, 2, 3		4.0	
High-level input voltage	V_{IH}	V_{DD} = 5.0 V V_O = 0.5 V or 4.5 V		All	1, 2, 3	3.5		V
		V_{DD} = 10.0 V V_O = 1.0 V or 9.0 V 3/		All	1, 2, 3	7.0		
		V_{DD} = 15.0 V V_O = 1.5 V or 13.5 V		All	1, 2, 3	11.0		
Low-level output current	I_{OL}	V_{DD} 5.0 V 4/ V_O = 0.4 V V_{IN} = 0.0 V or V_{DD}		All	1	0.51		mA
					2	0.36		
					3	0.64		
		V_{DD} 10.0 V 1/ V_O = 0.5 V V_{IN} = 0.0 V or V_{DD}		All	1	1.3		
					2	0.9		
					3	1.6		
		V_{DD} 15.0 V 1/ V_O = 1.5 V V_{IN} = 0.0 V or V_{DD}		All	1	3.4		
					2	2.4		
					3	4.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High-level output current	I_{OH}	V_{DD} 5.0 V 4/ V_O = 4.6 V V_{IN} = 0.0 V or V_{DD}		All	1	-0.51		mA
					2	-0.36		
					3	-0.64		
		V_{DD} 5.0 V 4/ V_O = 2.5 V V_{IN} = 0.0 V or V_{DD}		02	1	-1.6		
					2	-1.15		
					3	-2.0		
		V_{DD} 10.0 V 1/ V_O = 9.5 V V_{IN} = 0.0 V or V_{DD}		All	1	-1.3		
					2	-0.9		
					3	-1.6		
		V_{DD} 15.0 V 1/ V_O = 13.5 V V_{IN} = 0.0 V or V_{DD}		All	1	-3.4		
					2	-2.4		
					3	-4.2		
Input current	I_{IN}	V_{DD} = 18.0 V V_{IN} = 0.0 V or V_{DD}		01	1, 3		±0.1	µA
					2		±1.0	
		V_{DD} 15.0 V V_{IN} = 0.0 V or V_{DD}		02	1, 3		±0.1	
					2		±1.0	
Input capacitance	C_{IN}	V_{IN} = 0.0 V, T_C = +25°C, See 4.3.1c		All	4		7.5	pF
Functional tests		See 4.3.1d		All	7, 8			
Propagation delay time, CLOCK to Qn outputs	t_{PHL1}, t_{PLH1}	C_L = 50 pF R_L = 200 kΩ $t_r = t_f$ = 20 ns See figure 4	V_{DD} = 5.0 V	01	9	2.0	500.0	ns
					10, 11	2.0	650.0	
				02	9	25.0	600.0	
					10, 11 3/	38.0	900.0	
			V_{DD} = 10.0 V 3/	01	9	2.0	200.0	
					10, 11	2.0	260.0	
				02	9	2.0	260.0	
					10, 11	2.0	390.0	
			V_{DD} = 15.0 V 3/	01	9	2.0	150.0	
					10, 11	2.0	195.0	
				02	9	2.0	190.0	
					10, 11	2.0	285.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay time, RESET to Qn outputs	t_{PHL2}, t_{PLH2}	C_L = 50 pF R_L = 200 kΩ $t_r = t_f$ = 20 ns See figure 4	V_{DD} = 5.0 V	01	9	2.0	460.0	ns
					10, 11	2.0	598.0	
				02	9	25.0	600.0	
					10, 11	38.0	900.0	
			V_{DD} = 10.0 V 3/	01	9	2.0	200.0	
					10, 11	2.0	260.0	
				02	9	2.0	260.0	
					10, 11	2.0	390.0	
			V_{DD} = 15.0 V 3/	01	9	2.0	160.0	
					10, 11	2.0	208.0	
				02	9	2.0	190.0	
					10, 11	2.0	285.0	
Output transition time	t_{THL}, t_{TLH}		V_{DD} = 5.0 V	01	9	2.0	200.0	ns
					10, 11	2.0	260.0	
				02	9	10.0	200.0	
					10, 11	15.0	300.0	
			V_{DD} = 10.0 V 3/	01	9	2.0	100.0	
					10, 11	2.0	130.0	
				02	9	2.0	100.0	
					10, 11	2.0	150.0	
			V_{DD} = 15.0 V 3/	01	9	2.0	80.0	
					10, 11	2.0	104.0	
				02	9	2.0	80.0	
					10, 11	2.0	120.0	

1/ Guaranteed, if not tested, to the specified limits for device type 01.

2/ This test performed at -55°C with V_{DD} = 18 V.

3/ Guaranteed, if not tested, to the specified limits.

4/ Guaranteed, if not tested, at +125°C and -55°C for device type 01.

Device types	01 and 02
Case outlines	E, F
Terminal number	Terminal symbol
1	Q1
2	TRUE/COMPLIMENT
3	$\overline{K}$
4	J
5	RESET
6	CLOCK
7	PARALLEL/SERIALCONTROL
8	V_{SS}
9	PARALLEL INPUT-1
10	PARALLEL INPUT-2
11	PARALLEL INPUT-3
12	PARALLEL INPUT-4
13	Q4
14	Q3
15	Q2
16	V_{DD}

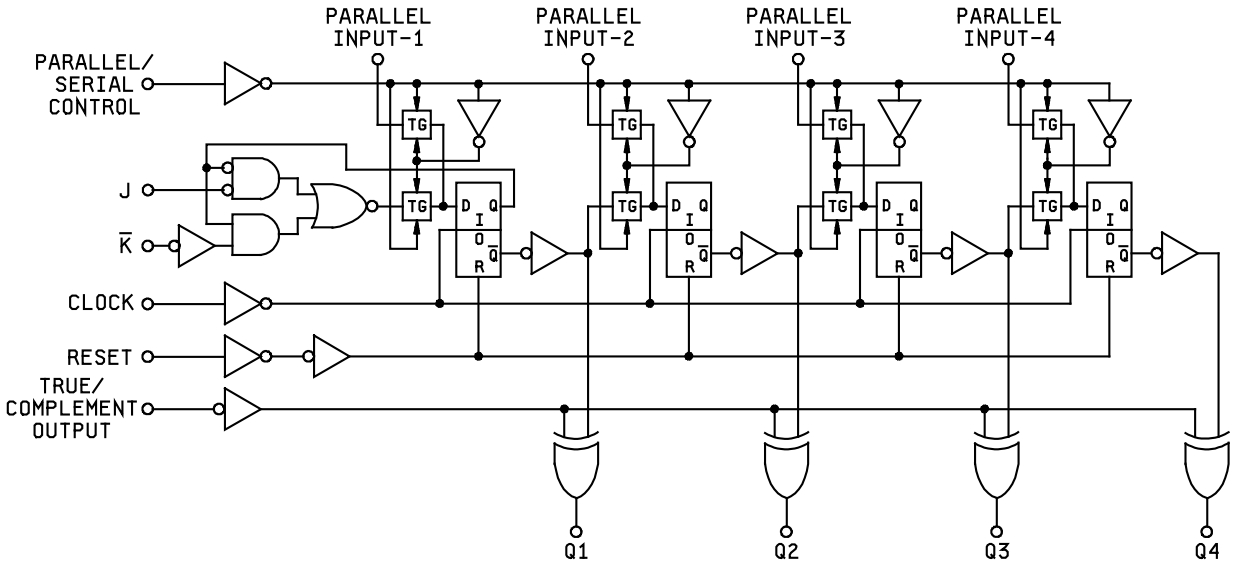
FIGURE 1. Terminal connections.

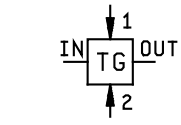
Device types 01 and 02

CLOCK	tn –1 (Inputs)				tn (Outputs)
	J	$\overline{K}$	RESET	Qn - 1	Qn
↑	L	X	L	L	L
↑	H	X	L	L	H
↑	X	L	L	H	L
↑	H	L	L	Qn – 1	$\overline{Qn-1}$ Toggle Mode
↑	X	H	L	H	H
↓	X	X	L	Qn – 1	Qn – 1
X	X	X	H	X	L

Parallel/serial = L = Serial mode
Parallel/serial = H = Parallel input mode
True/complement = H = True outputs
True/complement = L = Complement outputs
H = High level voltage
L = Low voltage level
X = Irrelevant
↑ = Low-to-high clock transition
↓ = High-to-low clock transition

FIGURE 2. Truth table.

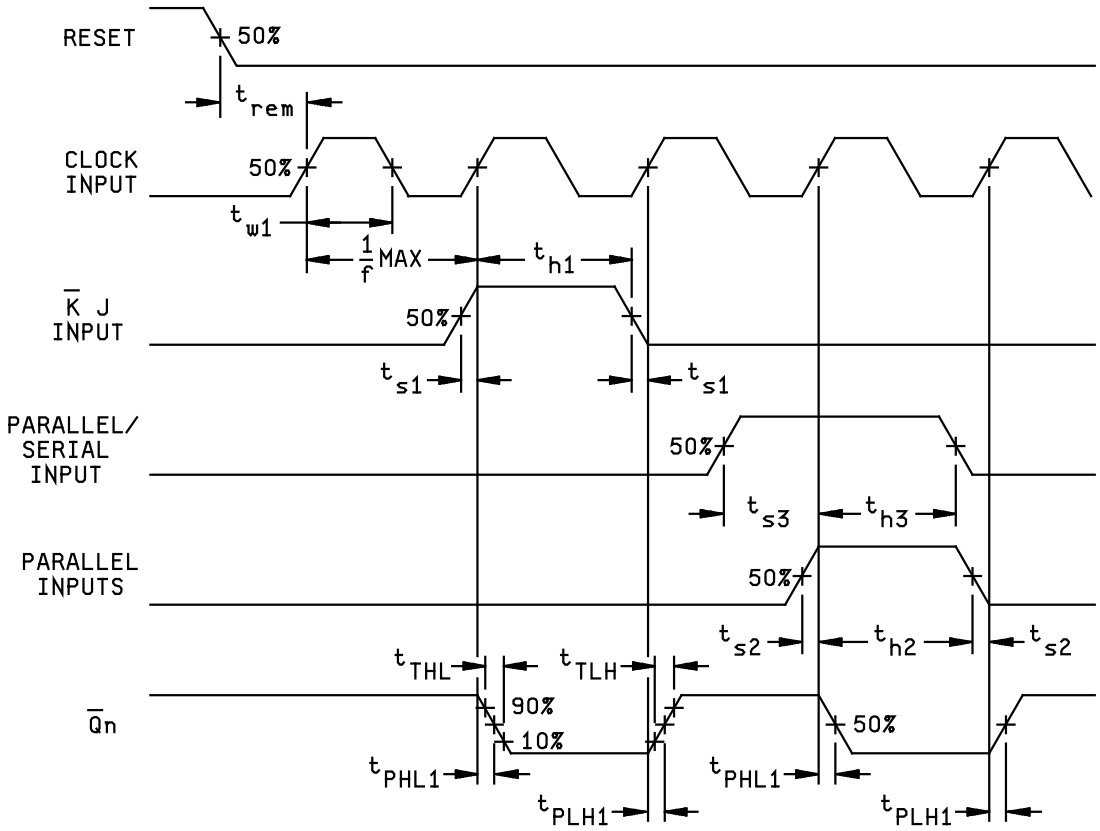




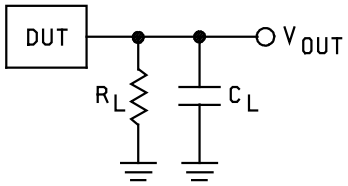
DETAIL
TRANSMISSION GATE

NOTES:
1. Parallel/serial = 0 = serial mode
2. True/compliment = 1 = true outputs
3. TG = transmission gate
4. Input to output is (see detail: Transmission gate):
   a. A bidirectional low impedance when control input 1 is low and control input 2 is high.
   b. An open circuit when control input 1 is high and control 2 is low.

FIGURE 3. Logic diagram.



TRUE/COMPLEMENT INPUT LOW



NOTES
1. C_L = 50 pF
2. R_L = 200 kΩ
3. Data rise and fall time (t_r, t_f) = 20 ns

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1, 2, 3, 7, 8, 9 1/
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11 2/
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and V_{SS} or GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal or email communication.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on thi0591s drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-08-20

Approved sources of supply for SMD 81017 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8101701EA	01295	CD4035BF3A
8101701FA	3/	CD4035B
8101702EA	3/	14035B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Inc. 12500 TI Blvd Dallas, TX 75243