REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Remove vendor FSCM 04713. Editorial changes throughout.	84-03-19	N. A. Hauck
B	Add vendor FSCM 27014. Device 01FX inactive for new design. Editorial changes throughout.	86-03-03	N. A. Hauck
C	Convert to military drawing format. Device 01FX inactive for new design. Add I_{OH} and I_{OL} to table I and delete minimum limits for t_r. Editorial changes throughout.	86-06-09	N. A. Hauck
D	Add device type 02 and vendor CAGE 34371. Delete vendor CAGE 31019. Changes to 1.3, 1.4, table I, and table II. Change in military drawing format. Change drawing CAGE code to 67268. Editorial changes throughout.	90-06-26	Monica Poelking
E	Technical changes in 1.4 and table I. Editorial changes throughout.	92-04-07	M. A. Frye
F	Update boilerplate to MIL-PRF-38535 requirements. - LTG	06-08-24	Thomas M. Hess
G	Update cage code information and boilerplate paragraphs throughout as required by the MIL-PRF-38535. - MAA	14-02-24	Thomas M. Hess
H	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. – TTM	21-09-24	Muhammad A. Akbar

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN CHANGED.
CURRENT CAGE CODE IS 67268

REV																			
SHEET																			
REV	H																		
SHEET	15																		

REV STATUS OF SHEETS															
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
81-07-01

REVISION LEVEL
H

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, PRESETTABLE BINARY/DECADE UP/DOWN COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**81016**

SHEET 1 OF 15

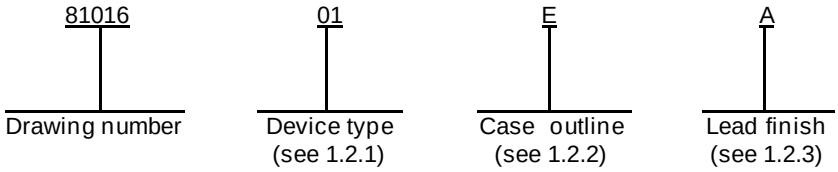
DSCC FORM 2233
APR 97

5962-E516-21

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4029B	Presettable binary/decade up/down counter
02	4029B	Presettable binary/decade up/down counter

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{DD}), device type 01 ..... -0.5 V dc to +18.0 V dc
Supply voltage range (V_{DD}), device type 02 ..... -0.5 V dc to +20.0 V dc
Input voltage range ..... -0.5 V dc to V_{DD} + 0.5 V dc
DC input current ..... ±10 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW 1/
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}), device type 01 ..... +3.0 V dc to +15.0 V dc
Supply voltage range (V_{DD}), device type 02 ..... +3.0 V dc to +18.0 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall time (t_r, t_f):
T_C = +25°C, V_{DD} = 5 V dc ..... 15.0 µs
T_C = -55°C, +125°C, V_{DD} = 5 V dc ..... 15.0 µs
T_C = +25°C, V_{DD} = 10 V dc ..... 10.0 µs
T_C = -55°C, +125°C, V_{DD} = 10 V dc ..... 15.0 µs
T_C = +25°C, V_{DD} = 15 V dc ..... 5.0 µs
T_C = -55°C, +125°C, V_{DD} = 15 V dc ..... 15.0 µs

1/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C to 200 mW.

1.4 Recommended operating conditions – Continued.

Minimum setup time, $\overline{\text{CARRY IN}}$ (t_{s1}):
- T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 360 ns
- T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 200 ns
- T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 300 ns
- T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 70 ns
- T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 105 ns
- T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 60 ns
- T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 90 ns

Minimum setup time, $\overline{\text{B/D}}$ or $\overline{\text{U/D}}$ (t_{s2}):
- T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 360 ns
- T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 340 ns
- T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 510 ns
- T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 140 ns
- T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 210 ns
- T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 100 ns
- T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 150 ns

Minimum clock pulse width (t_{w1}):
- T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 250 ns
- T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01 ..... 350 ns
- T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 180 ns
- T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 270 ns
- T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 90 ns
- T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 135 ns
- T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 60 ns
- T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 90 ns

Minimum PRESET ENABLE pulse width (t_{w2}):
- T_C = +25°C, V_{DD} = 5 V dc, device type 01 ..... 250 ns
- T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01 ..... 375 ns
- T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 130 ns
- T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 195 ns
- T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 70 ns
- T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 105 ns
- T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 50 ns
- T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 75 ns

Minimum hold time, $\overline{\text{CARRY IN}}$ (t_h):
- T_C = +25°C, V_{DD} = 5 V dc, device type 02 ..... 50 ns
- T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02 ..... 75 ns
- T_C = +25°C, V_{DD} = 10 V dc, device type 02 ..... 35 ns
- T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02 ..... 52 ns
- T_C = +25°C, V_{DD} = 15 V dc, device type 02 ..... 25 ns
- T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02 ..... 38 ns

1.4 Recommended operating conditions – Continued.

Maximum input clock frequency (f_{MAX}):

T_C = +25°C, V_{DD} = 5 V dc, device type 01	1.5 MHz
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01	2.0 MHz
T_C = +25°C, V_{DD} = 5 V dc, device type 02	2.0 MHz
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02	1.15 MHz
T_C = +25°C, V_{DD} = 10 V dc, device type 01	4.0 MHz
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 01	2.6 MHz
T_C = +25°C, V_{DD} = 15 V dc, device type 01	5.5 MHz
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 01	3.6 MHz

Minimum PRESET ENABLE removal time (t_{rem}):

T_C = +25°C, V_{DD} = 5 V dc, device type 01	450 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 01	700 ns
T_C = +25°C, V_{DD} = 5 V dc, device type 02	200 ns
T_C = -55°C, +125°C, V_{DD} = 5 V dc, device type 02	300 ns
T_C = +25°C, V_{DD} = 10 V dc, device type 02	110 ns
T_C = -55°C, +125°C, V_{DD} = 10 V dc, device type 02	165 ns
T_C = +25°C, V_{DD} = 15 V dc, device type 02	80 ns
T_C = -55°C, +125°C, V_{DD} = 15 V dc, device type 02	120 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Timing diagrams. The timing diagrams shall be as specified on figure 4.

3.2.6 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 and QML-38535 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Quiescent supply current	I_{DD}	V_{IN} = 0.0 V or V_{DD} V_{DD} = 5.0 V 1/		All	1, 3		5.0	µA
					2		150.0	
		V_{IN} = 0.0 V or V_{DD} V_{DD} = 10.0 V 2/		02	1, 3		10.0	
					2		300.0	
		V_{IN} = 0.0 V or V_{DD} V_{DD} = 15.0 V 1/		All	1, 3		20.0	
					2		600.0	
		V_{IN} = 0.0 V or V_{DD} V_{DD} = 20.0 V 3/		02	1, 3		100.0	
					2		3000.0	
Low-level output voltage	V_{OL}	V_{IN} = 0.0 V or V_{DD} $\lvert I_O \rvert$ < 1 µA	V_{DD} = 5.0 V 2/	All	1, 2, 3		0.05	V
			V_{DD} = 10.0 V 2/	02	1, 2, 3		0.05	
			V_{DD} = 15.0 V	All	1, 2, 3		0.05	
High-level output voltage	V_{OH}	V_{IN} = 0.0 V or V_{DD} $\lvert I_O \rvert$ < 1 µA	V_{DD} = 5.0 V 2/	All	1, 2, 3	4.95		V
			V_{DD} = 10.0 V 2/	02	1, 2, 3	9.95		
			V_{DD} = 15.0 V	All	1, 2, 3	14.95		
Low-level input voltage	V_{IL}	V_{DD} = 5.0 V V_O = 0.5 V or 4.5 V		All	1, 2, 3		1.5	V
		V_{DD} = 10.0 V V_O = 1.0 V or 9.0 V 2/		02	1, 2, 3		3.0	
		V_{DD} = 15.0 V V_O = 1.5 V or 13.5 V		All	1, 2, 3		4.0	
High-level input voltage	V_{IH}	V_{DD} = 5.0 V V_O = 0.5 V or 4.5 V		All	1, 2, 3	3.5		V
		V_{DD} = 10.0 V V_O = 1.0 V or 9.0 V 2/		02	1, 2, 3	7.0		
		V_{DD} = 15.0 V V_O = 1.5 V or 13.5 V		All	1, 2, 3	11.0		
Low-level output current	I_{OL}	V_{DD} = 5.0 V V_O = 0.4 V V_{IN} = 0.0 V or V_{DD}		All	1	0.51		mA
					2 1/	0.36		
					3 1/	0.64		
		V_{DD} = 10.0 V 2/ V_O = 0.5 V V_{IN} = 0.0 V or V_{DD}		02	1	1.3		
					2	0.9		
					3	1.6		
		V_{DD} = 15.0 V 2/ V_O = 1.5 V V_{IN} = 0.0 V or V_{DD}		All	1	3.4		
					2	2.4		
					3	4.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High-level output current	I_{OH}	V_{DD} = 5.0 V V_O = 4.6 V V_{IN} = 0.0 V or V_{DD}		All	1	-0.2		mA
					2	-0.14		
					3	-0.25		
		V_{DD} = 5.0 V V_O = 2.5 V V_{IN} = 0.0 V or V_{DD}		02	1	-1.6		
					2 2/	-1.15		
					3 2/	-2.0		
		V_{DD} = 10.0 V 2/ V_O = 9.5 V V_{IN} = 0.0 V or V_{DD}		02	1	-1.3		
					2	-0.9		
					3	-1.6		
		V_{DD} = 15.0 V 2/ V_O = 13.5 V V_{IN} = 0.0 V or V_{DD}		All	1	-1.5		
					2	-1.1		
					3	-1.8		
Input current	I_{IN}	V_{DD} = 15.0 V V_{IN} = 0.0 V or V_{DD}		01	1, 3		±0.1	µA
					2		±1.0	
		V_{DD} = 20.0 V 3/ V_{IN} = 0.0 V or V_{DD}		02	1, 3		±0.1	
					2		±1.0	
Input capacitance	C_{IN}	V_{IN} = 0.0 V, T_C = +25°C See 4.3.1c		All	4		7.5	pF
Functional tests		See 4.3.1d		All	7, 8			
Propagation delay time, CLOCK to Qn	t_{PHL1}, t_{PLH1}	C_L = 50 pF minimum R_L = 200 kΩ $t_r = t_f$ = 20 ns See figure 5 4/	V_{DD} = 5.0 V	01	9	20	450.0	ns
					10, 11	30	650.0	
				02	9	1.5	500.0	
					10, 11	1.5	750.0	
			V_{DD} = 10.0 V 2/	02	9	1.5	240.0	
					10, 11	1.5	360.0	
			V_{DD} = 15.0 V 2/	02	9	1.5	180.0	
					10, 11	1.5	270.0	
Propagation delay time, CLOCK to CARRY OUT	t_{PHL2}, t_{PLH2}		V_{DD} = 5.0 V	01	9	32	640.0	ns
					10, 11	48	960.0	
				02	9	1.5	560.0	
					10, 11	1.5	840.0	
			V_{DD} = 10.0 V 2/	02	9	1.5	260.0	
					10, 11	1.5	390.0	
			V_{DD} = 15.0 V 2/	02	9	1.5	190.0	
					10, 11	1.5	285.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay time, PRESET ENABLE to Qn	t_{PHL3}, t_{PLH3}	C_L = 50 pF minimum R_L = 200 kΩ $t_r = t_f$ = 20 ns See figure 5 4/	V_{DD} = 5.0 V	01	9	24	500.0	ns
					10, 11	36	750.0	
				02	9	1.5	470.0	
					10, 11	1.5	705.0	
			V_{DD} = 10.0 V 2/	02	9	1.5	200.0	
					10, 11	1.5	300.0	
			V_{DD} = 15.0 V 2/	02	9	1.5	160.0	
					10, 11	1.5	240.0	
Propagation delay time, PRESET ENABLE to CARRY OUT	t_{PHL4}, t_{PLH4}		V_{DD} = 5.0 V	01	9	40	800.0	ns
					10, 11	50	1200	
				02	9	1.5	640.0	
					10, 11	1.5	960.0	
			V_{DD} = 10.0 V 2/	02	9	1.5	290.0	
					10, 11	1.5	435.0	
			V_{DD} = 15.0 V 2/	02	9	1.5	210.0	
					10, 1	1.5	305.0	
Propagation delay time, CARRY IN to CARRY OUT	t_{PHL5}, t_{PLH5}		V_{DD} = 5.0 V	02	9	1.5	340.0	ns
					10, 11	1.5	510.0	
			V_{DD} = 10.0 V 2/	02	9	1.5	140.0	
					10, 11	1.5	210.0	
			V_{DD} = 15.0 V 2/	02	9	1.5	100.0	
					10, 11	1.5	150.0	
Output transition time, Qn or CARRY OUT	t_{THL}, t_{TLH}		V_{DD} = 5.0 V	01	9	10	225.0	ns
					10, 11	15	325.0	
				02	9	1.5	200.0	
					10, 11	1.5	300.0	
			V_{DD} = 10.0 V 2/	02	9	1.5	100.0	
					10, 11	1.5	150.0	
			V_{DD} = 15.0 V 2/	02	9	1.5	80.0	
					10, 11	1.5	120.0	

1/ Guaranteed, if not tested, to the specified limits for device type 02.

2/ Guaranteed, if not tested, to the specified limits.

3/ This test performed at -55°C with V_{DD} = 18 V.

4/ Propagation delay tests are performed on a one-input to one-output basis only for device type 02.

Device types	01 and 02
Case outlines	E and F
Terminal number	Terminal symbol
1	PRESET ENABLE
2	Q4
3	JAM 4
4	JAM 1
5	$\overline{\text{CARRY IN}}$
6	Q1
7	$\overline{\text{CARRY OUT}}$
8	V_{SS}
9	BINARY/$\overline{\text{DECADE}}$
10	$\overline{\text{UP/DOWN}}$
11	Q2
12	JAM 2
13	JAM 3
14	Q3
15	CLOCK
16	V_{DD}

FIGURE 1. Terminal connections.

Device types 01 and 02				
$\overline{\text{CARRY IN}}$	$\overline{\text{UP/DOWN}}$	PRESET ENABLE	BINARY/$\overline{\text{DECADE}}$	ACTION
H	X	L	X	No change
L	H	L	L	Count up ($\overline{\text{DECADE}}$)
L	H	L	H	Count up ($\overline{\text{BINARY}}$)
L	L	L	L	Count down (DECADE
L	L	L	H	Count down (BINARY)
X	X	H	X	PRESET

H = High voltage level
L = Low voltage level
X = Irrelevant

FIGURE 2. Truth table.

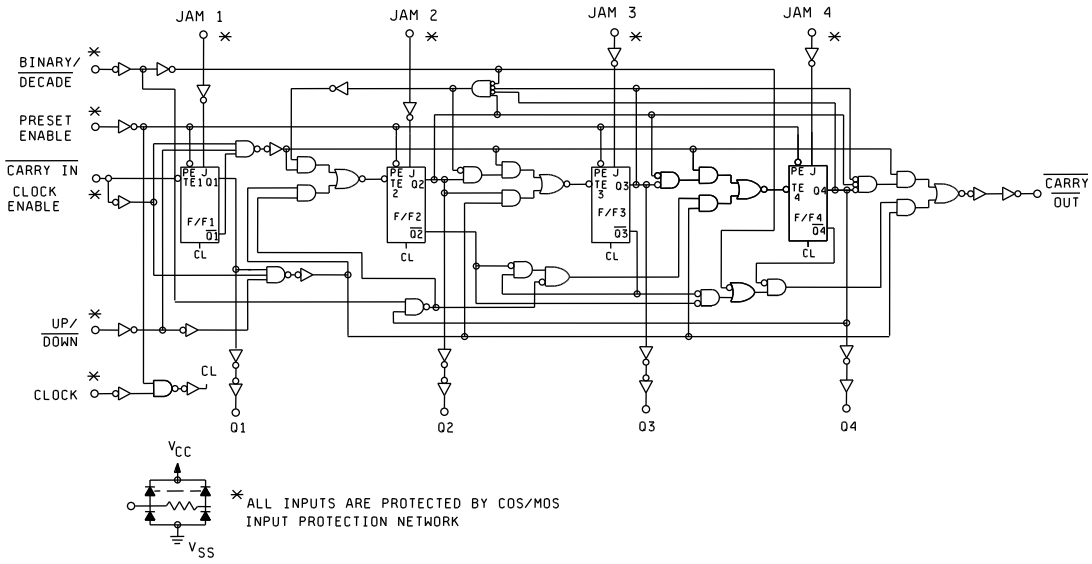


FIGURE 3. Logic diagram.

BINARY MODE

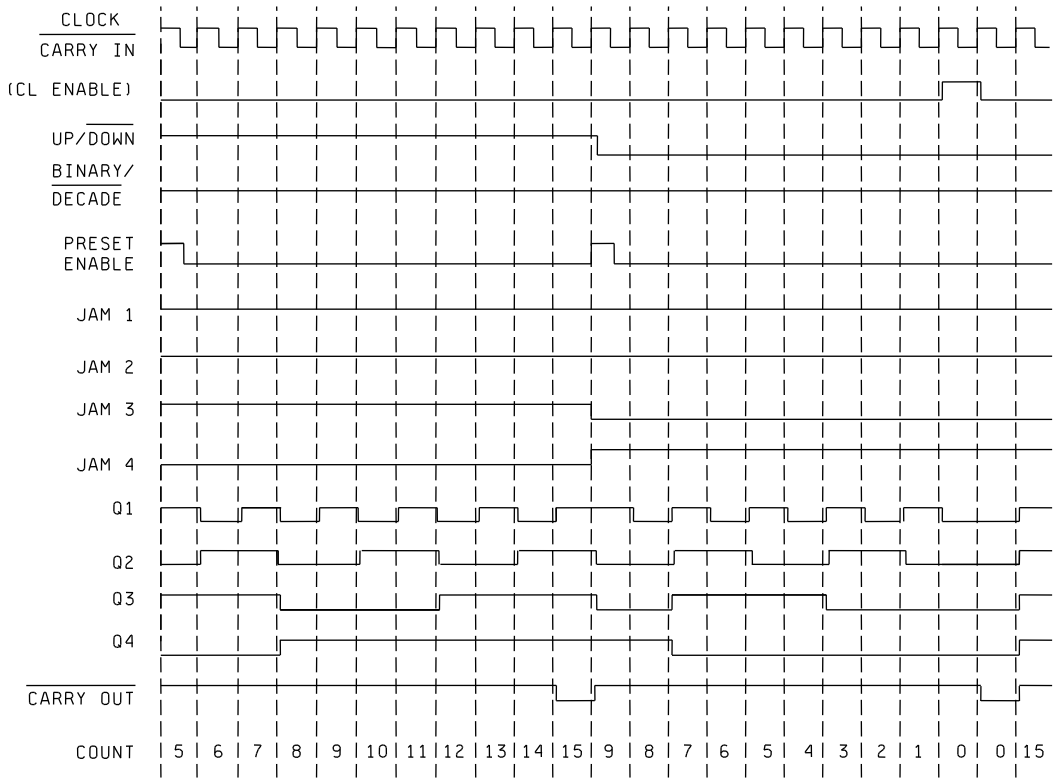


FIGURE 4. Timing diagrams.

DECADE MODE

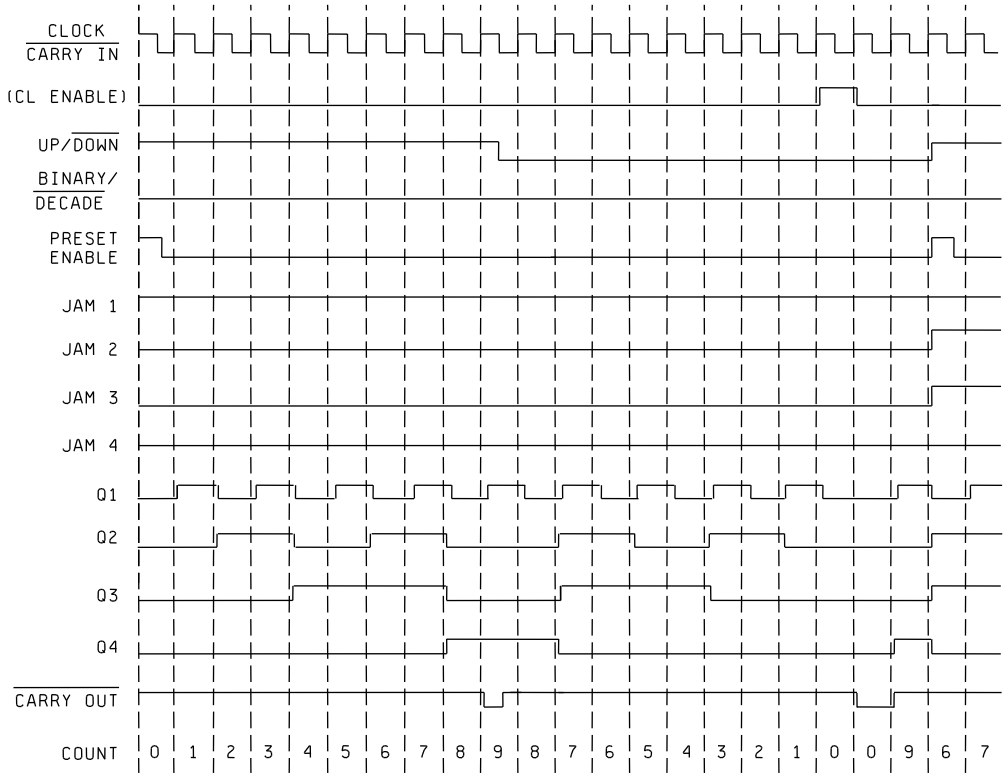
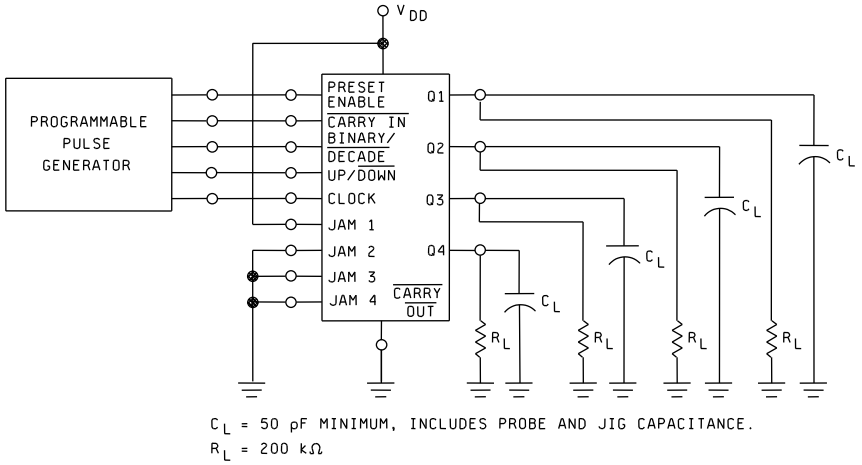


FIGURE 4. Timing diagrams – Continued.



C_L = 50 pF MINIMUM, INCLUDES PROBE AND JIG CAPACITANCE.
R_L = 200 kΩ

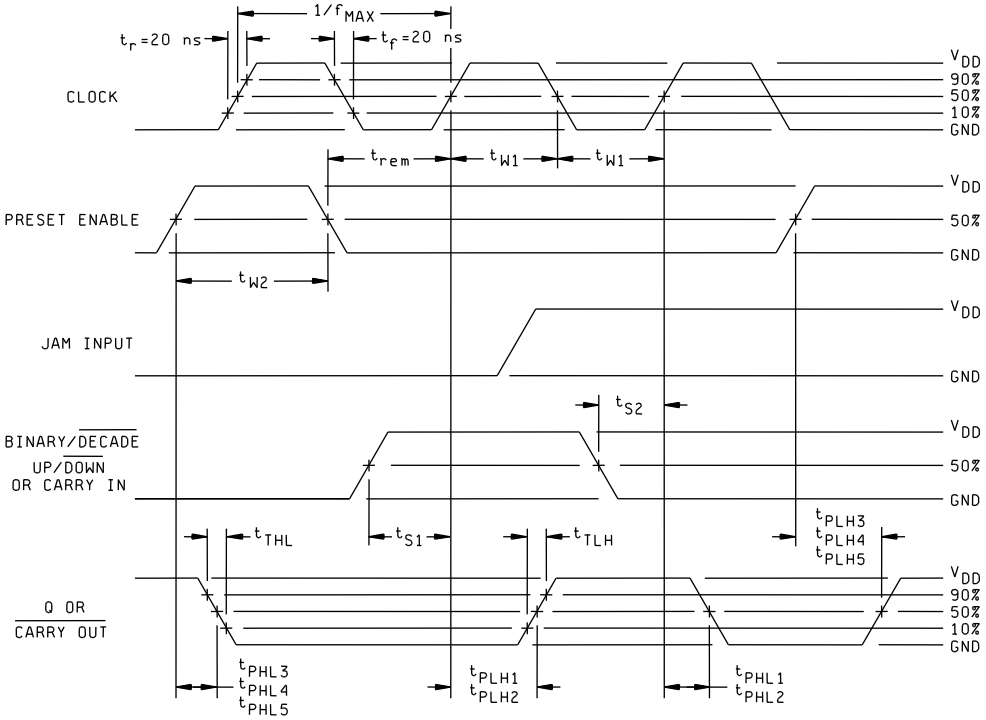


FIGURE 5. Test circuit and switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, and D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1, 2, 3, 7, 9 1/
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11 2/
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0591.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-09-24

Approved sources of supply for SMD 81016 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8101601EA	3/	CD4029B
8101601FA	3/	CD4029B
8101602EA	01295	CD4029BF3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243