REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
G	Delete vendor CAGE 34335. Convert to military drawing format. Delete minimum limits from propagation delays. Add logic diagram.	87-07-01	N. A. Hauck
H	Changes in accordance with NOR 5962-R277-97. -tn	97-04-14	Raymond Monnin
J	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	04-07-27	Raymond Monnin
K	Update drawing to current MIL-PRF-38535 requirements. -jt	17-02-03	Charles Saffle
L	Update drawing to latest MIL-PRF-38535 requirements. -jt	22-01-19	James R.Eschmeyer

CURRENT CAGE CODE 67268

The original first page of this drawing has been replaced.

REV																				
SHEET																				
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SHEET																				

REV STATUS	REV	L	L	L	L	L	L	L	L	L	L	L	L		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Monica L. Grosel

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
78-12-20

REVISION LEVEL
L

MICROCIRCUIT, DIGITAL, LOW POWER SCHOTTKY, TTL, SHIFT REGISTER MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**78024**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

78024	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54LS299	8-bit universal shift/storage register
02	25LS299	8-bit universal shift/storage register

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at –18 mA to +7.0 V dc
Storage temperature	-65°C to +150°C
Maximum power dissipation (P_D)	292 mW 1/
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R, S, and 2	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level output current (I_{OH}):	
Q_A through Q_H	-1 mA
$Q_{A'}$ or $Q_{H'}$	-0.4 mA
Low level output current (I_{OL}):	
Q_A through Q_H	12 mA
$Q_{A'}$ or $Q_{H'}$	4 mA
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum power dissipation is defined as V_{CC} X I_{CC}, and must withstand the added P_D due to short circuit test e.g., I_{OS}.

1.4 Recommended operating conditions – continued.

Select setup time:	
Device 01	35 ns minimum
Device 02	23 ns minimum
Data setup time: 2/	
Device 01	20 ns minimum
Device 02	23 ns minimum
Clear inactive state setup time:	
Device 01	20 ns minimum
Device 02	23 ns minimum
Select hold time 2/	10 ns minimum
Data hold time:	
Device 01	3 ns minimum
Device 02	9 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

2/ Data includes the two serial inputs and the eight input/output data lines.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level input voltage	V_{IH}			1, 2, 3	All	2		V
Low level input voltage	V_{IL}			1, 2, 3	All		0.7	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA, T_C = +25°C		1	All		-1.5	V
High level output voltage, Q_A through Q_H	V_{OH1}	V_{CC} = 4.5 V, V_{IL} = 0.7 V,	I_{OH} = -1 mA	1, 2, 3	All	2.4		V
High level output voltage $Q_{A'}$ or $Q_{H'}$	V_{OH2}	V_{IH} = 2 V	I_{OH} = -0.4 mA	1, 2, 3	All	2.5		V
Low level output voltage, Q_A through Q_H	V_{OL1}		I_{OL} = 12 mA	1, 2, 3	01		0.4	V
			I_{OL} = 8 mA	1, 2, 3	02		0.4	V
Low level output voltage, $Q_{A'}$ or $Q_{H'}$	V_{OL2}		I_{OL} = 4 mA	1, 2, 3	01		0.4	V
			I_{OL} = 4 mA	1, 2, 3	02		0.45	V
Off-state output current high level voltage applied, Q_A through Q_H	I_{OZH}	V_{CC} = 5.5 V, V_{IH} = 2 V, V_{OUT} = 2.7 V		1, 2, 3	All		40	µA
Off-state output current low level voltage applied, Q_A through Q_H	I_{OZL}	V_{CC} = 5.5 V, V_{IL} = 0.7 V, V_{OUT} = 0.4 V		1, 2, 3	All		-400	µA
Input current at maximum input voltage	I_I	V_{CC} = 5.5 V,	S0, S1 inputs; V_{IN} = 7 V	1, 2, 3	All		200	µA
			A through H inputs; V_{IN} = 5.5 V	1, 2, 3	All		100	µA
			All other inputs; V_{IN} = 7 V	1, 2, 3	All		100	µA
High level input current	I_{IH}	V_{CC} = 5.5 V,	A through H, S0, S1 inputs	1, 2, 3	All		40	µA
		V_{IN} = 2.7 V	All other inputs	1, 2, 3	All		20	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V,	S0, S1 inputs	1, 2, 3	All		-0.8	mA
		V_{IN} = 0.4 V	All other inputs	1, 2, 3	All		-0.4	mA
Short circuit output current 1/	I_{OS}	V_{CC} = 5.5 V,	Q_A through Q_H	1, 2, 3	All	-30	-130	mA
		V_{OUT} = 0.0 V	$Q_{A'}$ or $Q_{H'}$	1, 2, 3	All	-20	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V		1, 2, 3	All		60	mA
Functional tests		See 4.3.1c		7	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Maximum clock frequency	f_{MAX}		C_L = 50 pF ±10%	9	02	25		MHz
				10, 11		32		
Propagation delay, clock to $Q_{A'}$ or $Q_{H'}$	t_{PLH1} t_{PHL1}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	02		28	ns
				10, 11			38	
			C_L = 50 pF ±10%	9	02		33	ns
				10, 11			45	
Propagation delay, clear to $Q_{A'}$ or $Q_{H'}$	t_{PHL2}		C_L = 15 pF ±10%	9	02		35	ns
				10, 11			49	
			C_L = 50 pF ±10%	9	02		40	ns
				10, 11			56	
Propagation delay, clock to Q_A through Q_H	t_{PLH3} t_{PHL3}		C_L = 45 pF ±10%	9	02		35	ns
				10, 11			45	
			C_L = 50 pF ±10%	9	02		40	ns
				10, 11			52	
Maximum clock frequency	f_{MAX}		C_L = 50 pF ±10%	9	01	20		MHz
				10, 11		12		
Propagation delay, clock to $Q_{A'}$ or $Q_{H'}$	t_{PLH4}		C_L = 15 pF ±10%	9	01		33	ns
				10, 11			46	
			C_L = 50 pF ±10%	9	01		36	ns
				10, 11			50	
	t_{PHL4}		C_L = 15 pF ±10%	9	01		39	ns
				10, 11			55	
			C_L = 50 pF ±10%	9	01		42	ns
				10, 11			59	
Propagation delay, clear to $Q_{A'}$ or $Q_{H'}$	t_{PHL5}		C_L = 15 pF ±10%	9	01		40	ns
				10, 11			56	
			C_L = 50 pF ±10%	9	01		43	ns
				10, 11			60	
Propagation delay, clock to Q_A through Q_H	t_{PLH6}	V_{CC} = 5.0 V, R_L = 665Ω ±5% 2/	C_L = 45 pF ±10%	9	01		25	ns
				10, 11			35	
			C_L = 50 pF ±10%	9	01		26	ns
				10, 11			36	
	t_{PHL6}		C_L = 45 pF ±10%	9	01		39	ns
				10, 11			55	
			C_L = 50 pF ±10%	9	01		40	ns
				10, 11			56	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay, clear to Q_A to Q_H	t_{PHL7}	V_{CC} = 5.0 V, R_L = 665Ω ±5% 2/	C_L = 45 pF ±10%	9	01		40	ns
				10, 11			56	
Propagation delay, clear to Q_A to Q_H	t_{PHL8}		C_L = 45 pF ±10%	9	02		35	ns
				10, 11			49	
Propagation delay, $\overline{G}$ 1, $\overline{G}$ 2 to Q_A through Q_H	t_{PZH} t_{PZL}		C_L = 45 pF ±10%	9	All		35	ns
				10, 11			49	
Propagation delay, $\overline{G}$ 1, $\overline{G}$ 2 to Q_A through Q_H	t_{PHZ} t_{PLZ}		C_L = 5 pF ±10%	9	All		25	ns
				10, 11			35	

1/ Not more than one output should be shorted at a time and the duration of the short circuit condition should not exceed 1 second.

2/ Propagation delay time testing and maximum clock frequency testing may be performed using either C_L = 5 pF, C_L = 15 pF, C_L = 45 pF, or C_L = 50 pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50 pF load.

Device type	01	02
Case outlines	R, S, 2	R, S
Terminal number	Terminal symbol	
1	S0	S0
2	$\overline{G}$ 1	$\overline{G}$ 1
3	$\overline{G}$ 2	$\overline{G}$ 2
4	G/Q_G	DY_6
5	E/Q_E	DY_4
6	C/Q_C	DY_2
7	A/Q_A	DY_0
8	$Q_{A'}$	Q_0
9	CLR	CLR
10	GND	GND
11	SR	SR
12	CLK	CP
13	B/Q_B	DY_1
14	D/Q_D	DY_3
15	F/Q_F	DY_5
16	H/Q_H	DY_7
17	$Q_{H'}$	Q_7
18	SL	SL
19	S1	S1
20	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Device 01

Mode	Inputs								Inputs/outputs								Outputs	
	CLR	Function select		Output control		CLK	Serial											
		S1	S0	$\overline{G}$ 1†	$\overline{G}$ 2†		SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A	Q_H
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

† When one or both output controls are high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

L = Low ↑ = Transition low to high Z = High impedance
H = High X = Don't care

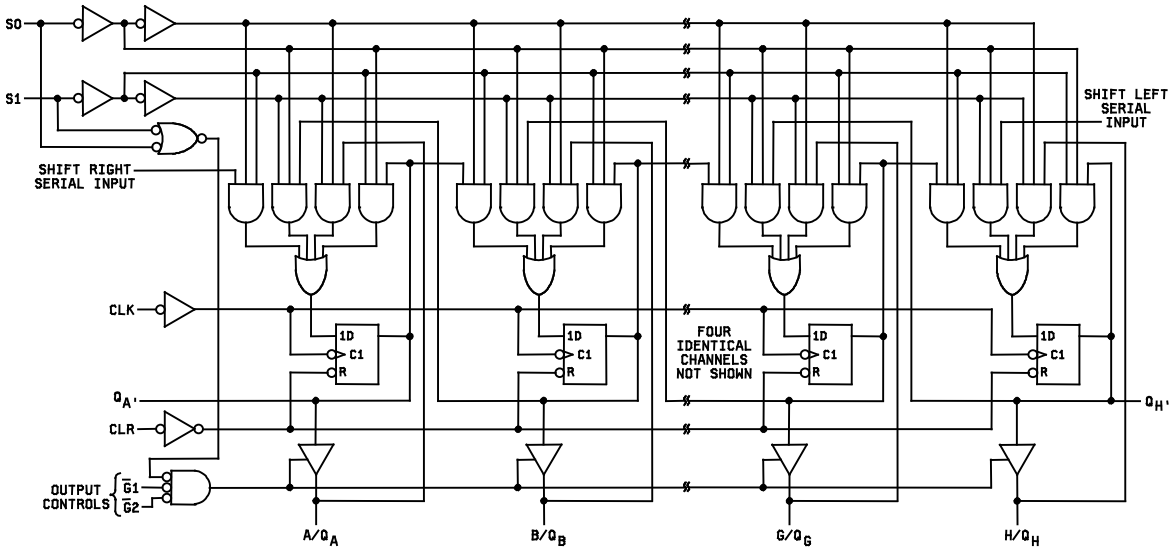
Device 02

Function		Inputs								Outputs		Inputs/outputs							
		SR	SL	CLR	CLK	S0	S1	$\overline{G}$ 1	$\overline{G}$ 2	Q_0	Q_7	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear		X	X	L	X	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output control		X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
M O D E	Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Load (note 2)	X	X	H	↑	H	H	L	L	A	H	A	B	C	D	E	F	G	H
	Shift Right	L	X	H	↑	H	L	L	L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Right	H	X	H	↑	H	L	L	L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Left	X	L	H	↑	L	H	L	L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
	Shift Left	X	H	H	↑	L	H	L	L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = Low ↑ = Transition low to high Z = High impedance
H = High X = Don't care NC = No change

Notes:
1. Either Low to observe outputs.
2. In this mode DY_1 are inputs.

FIGURE 2. Truth tables.



I/O PORTS NOT SHOWN:

C/Q_C	E/Q_E
D/Q_D	F/Q_F

FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-01-19

Approved sources of supply for SMD 78024 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https:/landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
7802401RA	01295	SNJ54LS299J
7802401SA	01295	SNJ54LS299W
78024012A	01295	SNJ54LS299FK
7802402RA	3/	AM25LS299DMB
7802402SA	3/	AM25LS299FMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243