REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Revised to military drawing format. Delete vendors, CAGE 07263, 27014 and 18324. Add note for no approved source available for packages A and B. Add LCC package, case outline 2. Table I, f_{MAX} (A to Q_A, C_L = 15 pF, 10 and 11); change 20 MHz to 19 MHz. (50 pF, 10 and 11); change 23 MHz to 18 MHz. (B to Q_B, C_L = 15 pF, 10 and 11); change from 11 MHz to 10 MHz. Change I_{IH3}, 200 µA to 80 µA. I_{IH4}, 200 µA to 400 µA, I_{IH5}, 80 µA to 160 µA, I_{IH6}, 400 µA to 800 µA. Add logic diagram. Change CAGE number to 67268.	87-10-05	R. P. Evans
D	Update to reflect latest changes in format and requirements. Editorial changes throughout. - les	03-04-07	Raymond Monnin
E	Change 3.5 marking paragraph to remove “5962”. Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-08-16	Thomas M. Hess

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
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REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY

Monica L. Grosel

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

D. A. Di Cenzo

APPROVED BY

Robert P. Evans

DRAWING APPROVAL DATE

76-11-24

REVISION LEVEL

E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, BIPOLAR LOW POWER SCHOTTKY TTL, COUNTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**76032**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

76032	01	C	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54LS90	Decade counter

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A	GDFP5-F14 or CDFP6-F14	14	Flat
B	GDFP4-F14	14	Flat
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/	85 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimim to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.4 mA, V_{IL} = 0.7 V, V_{IH} = 2.0 V		1, 2, 3	All	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, V_{IH} = 2.0 V		1, 2, 3	All		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1	All		-1.5	V
Input current at reset inputs	I_{IH1}	V_{CC} = 5.5 V, V_{IH} = 2.7 V		1, 2, 3	All		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IH} = 5.5 V		1, 2, 3	All		100	µA
	I_{IL1}	V_{CC} = 5.5 V, V_{IL} = 0.4 V		1, 2, 3	All		-400	µA
Input current at A input	I_{IH3}	V_{CC} = 5.5 V, V_{IH} = 2.7 V		1, 2, 3	All		80	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IH} = 5.5 V		1, 2, 3	All		400	µA
	I_{IL2}	V_{CC} = 5.5 V, V_{IL} = 0.4 V		1, 2, 3	All		-2.4	mA
Input current at B input	I_{IH5}	V_{CC} = 5.5 V, V_{IH} = 2.7 V		1, 2, 3	All		160	µA
	I_{IH6}	V_{CC} = 5.5 V, V_{IH} = 5.5 V		1, 2, 3	All		800	µA
	I_{IL3}	V_{CC} = 5.5 V, V_{IL} = 0.4 V		1, 2, 3	All		-3.2	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.0 V 1/		1, 2, 3	All	-15	-130	mA
Supply current	I_{CC}	V_{CC} = 5.5 V		1, 2, 3	All		15	mA
Functional tests		See 4.3.1c		7	All			
Maximum clock frequency from A to Q_A	f_{MAX1}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	All	32		MHz
				10, 11	All	19		MHz
			C_L = 50 pF ±10%	9	All	28		MHz
				10, 11	All	18		MHz
Maximum clock frequency from B to Q_B	f_{MAX2}		C_L = 15 pF ±10%	9	All	16		MHz
				10, 11	All	10		MHz
			C_L = 50 pF ±10%	9	All	11		MHz
				10, 11	All	6		MHz
Propagation delay time, from A to Q_A	t_{PHL1}		C_L = 15 pF ±10%	9	All		18	ns
				10, 11	All		25	ns
			C_L = 50 pF ±10%	9	All		23	ns
				10, 11	All		32	ns
	t_{PLH1}		C_L = 15 pF ±10%	9	All		16	ns
				10, 11	All		22	ns
			C_L = 50 pF ±10%	9	All		21	ns
				10, 11	All		29	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, from A to Q_D	t_{PHL2}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	All		50	ns
				10, 11	All		70	ns
			C_L = 50 pF ±10%	9	All		55	ns
				10, 11	All		77	ns
	t_{PLH2}		C_L = 15 pF ±10%	9	All		48	ns
				10, 11	All		67	ns
			C_L = 50 pF ±10%	9	All		53	ns
				10, 11	All		74	ns
Propagation delay time, from B to Q_B	t_{PHL3}		C_L = 15 pF ±10%	9	All		21	ns
				10, 11	All		29	ns
			C_L = 50 pF ±10%	9	All		26	ns
				10, 11	All		36	ns
	t_{PLH3}		C_L = 15 pF ±10%	9	All		16	ns
				10, 11	All		22	ns
			C_L = 50 pF ±10%	9	All		21	ns
				10, 11	All		29	ns
Propagation delay time, from B to Q_C	t_{PHL4}		C_L = 15 pF ±10%	9	All		35	ns
				10, 11	All		49	ns
			C_L = 50 pF ±10%	9	All		40	ns
				10, 11	All		56	ns
	t_{PLH4}		C_L = 15 pF ±10%	9	All		32	ns
				10, 11	All		45	ns
			C_L = 50 pF ±10%	9	All		37	ns
				10, 11	All		52	ns
Propagation delay time, from B to Q_D	t_{PHL5}		C_L = 15 pF ±10%	9	All		35	ns
				10, 11	All		49	ns
			C_L = 50 pF ±10%	9	All		40	ns
				10, 11	All		56	ns
	t_{PLH5}		C_L = 15 pF ±10%	9	All		32	ns
				10, 11	All		45	ns
			C_L = 50 pF ±10%	9	All		37	ns
				10, 11	All		52	ns
Propagation delay time, from set-to-0 to output	t_{PHL6}		C_L = 15 pF ±10%	9	All		40	ns
				10, 11	All		56	ns
			C_L = 50 pF ±10%	9	All		45	ns
				10, 11	All		63	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, from set-to-9 to Q_B or Q_C	t_{PHL7}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	All		40	ns
				10, 11	All		56	ns
			C_L = 50 pF ±10%	9	All		45	ns
				10, 11	All		63	ns
Propagation delay time, from set-to-9 to Q_A or Q_D	t_{PLH7}		C_L = 15 pF ±10%	9	All		30	ns
				10, 11	All		42	ns
			C_L = 50 pF ±10%	9	All		35	ns
				10, 11	All		49	ns

1/ Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed one second.

2/ Propagation delay time testing and maximum clock frequency testing may be performed using either C_L = 15 pF or C_L = 50 pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50 pF load.

Case outlines	A, B, C, and D	2
Terminal number	Terminal symbol	
1	CKB	NC
2	$R_{0(1)}$	CKB
3	$R_{0(2)}$	$R_{0(1)}$
4	NC	$R_{0(2)}$
5	V_{CC}	NC
6	$R_{9(1)}$	NC
7	$R_{9(2)}$	NC
8	Q_C	V_{CC}
9	Q_B	$R_{9(1)}$
10	GND	$R_{9(2)}$
11	Q_D	NC
12	Q_A	Q_C
13	NC	Q_B
14	CKA	GND
15	- - -	NC
16	- - -	Q_D
17	- - -	NC
18	- - -	Q_A
19	- - -	NC
20	- - -	CKA

FIGURE 1. Terminal connections.

Reset/count function table

Reset inputs				Output			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level, X = irrelevant.

BI-Quinary (5-2)
(See note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

BCD count sequence
(See note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

FIGURE 2. Truth tables.

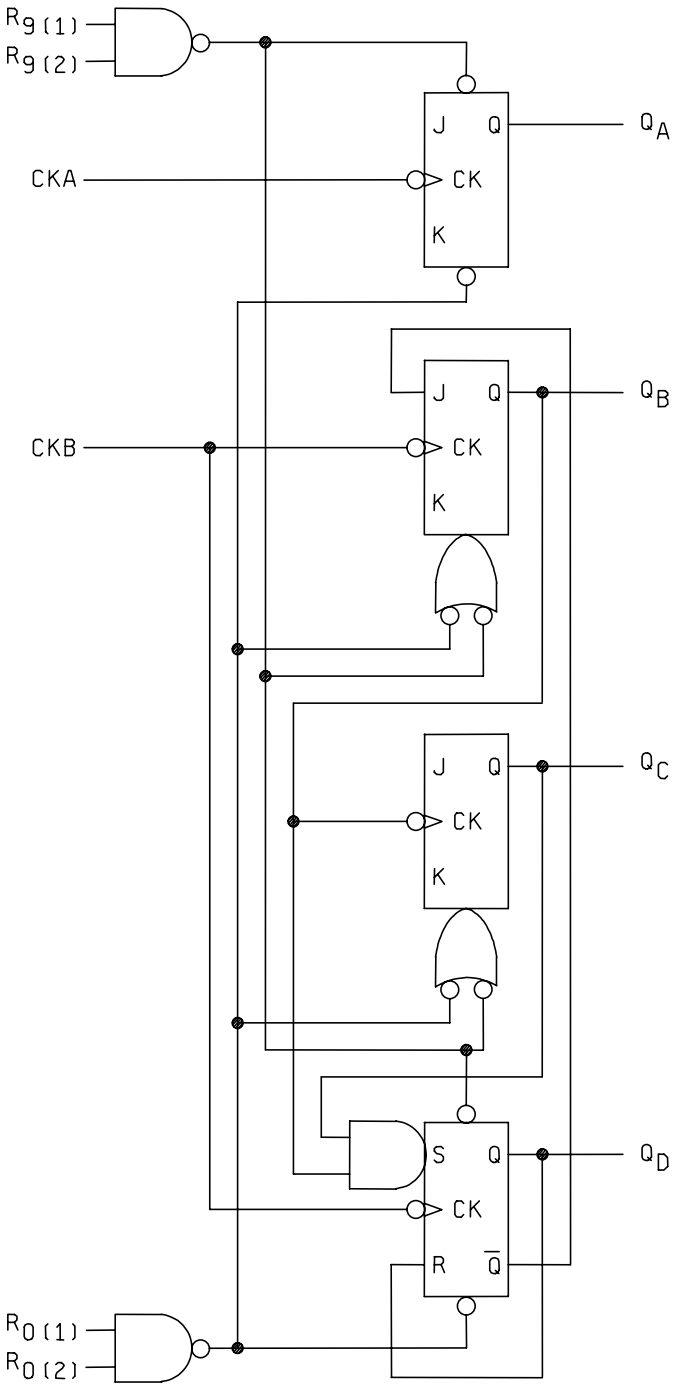

FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c, Subgroup 7 shall include verification of the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-08-16

Approved sources of supply for SMD 76032 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification part number
7603201AA	3/	54LS90	M38510/31501BAA
7603201BA	3/	54LS90	M38510/31501BBA
7603201CA	01295	SNJ54LS90J	M38510/31501BCA
7603201DA	01295	SNJ54LS90W	M38510/31501BDA
76032012A	3/	54LS90M/B2AJC	M38510/31501B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 POC: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.