REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
F	Convert to military drawing format. Change Code Ident. No. to 67268. Change max. clock frequency at temp. subgroups 10 and 11 at 15 pF. Add LCC package.	87-10-17	N. A. Hauck
G	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	03-01-07	Raymond Monnin
H	Update to reflect latest changes in format and requirements. Correct paragraph in 3.5. Editorial changes throughout. –les	05-08-16	Raymond Monnin
J	Update drawing to current MIL-PRF-38535 requirements. -jt	17-07-14	Charles Saffle

ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			J	J	J	J	J	J	J	J	J	J	J	J		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Joseph A. Kerby

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
76-03-19

MICROCIRCUIT, DIGITAL, LOW-POWER SCHOTTKY TTL, COUNTERS, MONOLITHIC SILICON

REVISION LEVEL
J

SIZE	CAGE CODE	
A	**14933**	**76009**

SHEET 1 OF 12

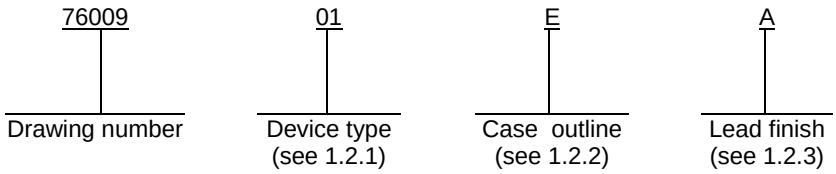
DSCC FORM 2233
APR 97

5962-E450-17

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54LS191	Synchronous, up/down counter with down/up mode control

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	192mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -400 µA V_{IN} = 0.7 V or 2.0 V		1, 2, 3	All	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4 mA V_{IN} = 0.7 V or 2.0 V		1, 2, 3	All		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA, T_C = +25°C		1	All		-1.5	V
High level input current, enable input	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3	All		60	µA
High level input current, other inputs	I_{IH2}			1, 2, 3	All		20	µA
High level input current, enable input	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		0.3	mA
High level input current, other inputs	I_{IH4}			1, 2, 3	All		0.1	mA
Low level input current, enable input	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		1, 2, 3	All		-1.2	mA
Low level input current, other inputs	I_{IL2}			1, 2, 3	All		-0.4	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V 1/		1, 2, 3	All	-20	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V		1, 2, 3	All		35	mA
Functional tests		See 4.3.1c		7	All			
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	All	20		MHz
				10, 11	All	12		MHz
			C_L = 50 pF ±10%	9	All	15		MHz
				10, 11	All	10		MHz
Propagation delay time, high to low level, load to Q_A, Q_B, Q_C, Q_D	t_{PHL1}		C_L = 15 pF ±10%	9	All		50	ns
				10, 11	All		70	ns
			C_L = 50 pF ±10%	9	All		55	ns
				10, 11	All		77	ns
Propagation delay time, low to high level, load to Q_A, Q_B, Q_C, Q_D	t_{PLH1}		C_L = 15 pF ±10%	9	All		33	ns
				10, 11	All		46	ns
			C_L = 50 pF ±10%	9	All		38	ns
				10, 11	All		53	ns
Propagation delay time, high to low level, data A, B, C , D to Q_A, Q_B, Q_C, Q_D	t_{PHL2}		C_L = 15 pF ±10%	9	All		40	ns
				10, 11	All		56	ns
			C_L = 50 pF ±10%	9	All		45	ns
				10, 11	All		63	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, low to high level, data A, B, C , D to Q_A, Q_B, Q_C, Q_D	t_{PLH2}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	All		32	ns
				10, 11	All		45	ns
			C_L = 50 pF ±10%	9	All		37	ns
				10, 11	All		52	ns
Propagation delay time, high to low level, clock to ripple clock	t_{PHL3}		C_L = 15 pF ±10%	9	All		24	ns
				10, 11	All		34	ns
			C_L = 50 pF ±10%	9	All		29	ns
				10, 11	All		41	ns
Propagation delay time, low to high level, clock to ripple clock	t_{PLH3}		C_L = 15 pF ±10%	9	All		20	ns
				10, 11	All		28	ns
			C_L = 50 pF ±10%	9	All		25	ns
				10, 11	All		35	ns
Propagation delay time, high to low level, clock to Q_A, Q_B, Q_C, Q_D	t_{PHL4}		C_L = 15 pF ±10%	9	All		36	ns
				10, 11	All		50	ns
			C_L = 50 pF ±10%	9	All		41	ns
				10, 11	All		57	ns
Propagation delay time, low to high level, clock to Q_A, Q_B, Q_C, Q_D	t_{PLH4}		C_L = 15 pF ±10%	9	All		24	ns
				10, 11	All		34	ns
			C_L = 50 pF ±10%	9	All		29	ns
				10, 11	All		41	ns
Propagation delay time, high to low level, clock to maximum	t_{PHL5}		C_L = 15 pF ±10%	9	All		52	ns
				10, 11	All		73	ns
			C_L = 50 pF ±10%	9	All		57	ns
				10, 11	All		80	ns
Propagation delay time, low to high level, clock to maximum	t_{PLH5}		C_L = 15 pF ±10%	9	All		42	ns
				10, 11	All		59	ns
			C_L = 50 pF ±10%	9	All		47	ns
				10, 11	All		66	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, high to low level, down/up to ripple clock	t_{PHL6}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	All		45	ns
				10, 11	All		63	ns
			C_L = 50 pF ±10%	9	All		50	ns
				10, 11	All		70	ns
Propagation delay time, low to high level, down/up to ripple clock	t_{PLH6}		C_L = 15 pF ±10%	9	All		45	ns
				10, 11	All		63	ns
			C_L = 50 pF ±10%	9	All		50	ns
				10, 11	All		70	ns
Propagation delay time, high to low level, down/up to maximum	t_{PHL7}		C_L = 15 pF ±10%	9	All		33	ns
				10, 11	All		46	ns
			C_L = 50 pF ±10%	9	All		38	ns
				10, 11	All		53	ns
Propagation delay time, low to high level, down/up to maximum	t_{PLH7}		C_L = 15 pF ±10%	9	All		33	ns
				10, 11	All		46	ns
			C_L = 50 pF ±10%	9	All		38	ns
				10, 11	All		53	ns
Propagation delay time, high to low level, enable to ripple clock	t_{PHL8}		C_L = 15 pF ±10%	9	All		33	ns
				10, 11	All		46	ns
			C_L = 50 pF ±10%	9	All		38	ns
				10, 11	All		53	ns
Propagation delay time, low to high level, enable to ripple clock	t_{PLH8}		C_L = 15 pF ±10%	9	All		33	ns
				10, 11	All		46	ns
			C_L = 50 pF ±10%	9	All		38	ns
				10, 11	All		53	ns

1/ Not more than one output should be shorted at a time, and the duration of the short-circuit condition should not exceed one second.

2/ Propagation delay time testing may be performed using either C_L = 15 pF or C_L = 50 pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50 pF load.

Device types	01	01
Case outlines	E, F	2
Terminal number	Terminal symbols	Terminal symbols
1	B	N/C
2	Q_B	B
3	Q_A	Q_B
4	$\overline{CTEN}$	Q_A
5	$D/\overline{U}$	$\overline{CTEN}$
6	Q_C	N/C
7	Q_D	$D/\overline{U}$
8	GND	Q_C
9	D	Q_D
10	C	GND
11	$\overline{LOAD}$	N/C
12	MAX MIN	D
13	$\overline{RCO}$	C
14	CLK	$\overline{LOAD}$
15	A	MAX MIN
16	V_{CC}	N/C
17	- - -	$\overline{RCO}$
18	- - -	CLK
19	- - -	A
20	- - -	V_{CC}

FIGURE 1. Terminal connections.

Up Count	Output				RIP CLK
	Q_D	Q_C	Q_B	Q_A	
0	L	L	L	L	H
1	L	L	L	H	H
2	L	L	H	L	H
3	L	L	H	H	H
4	L	H	L	L	H
5	L	H	L	H	H
6	L	H	H	L	H
7	L	H	H	H	H
8	H	L	L	L	H
9	H	L	L	H	H
10	H	L	H	L	H
11	H	L	H	H	H
12	H	H	L	L	H
13	H	H	L	H	H
14	H	H	H	L	H
15	H	H	H	H	L

Down Count	Output				RIP CLK
	Q_A	Q_B	Q_C	Q_D	
15	H	H	H	H	H
14	L	H	H	H	H
13	H	L	H	H	H
12	L	L	H	H	H
11	H	H	L	H	H
10	L	H	L	H	H
9	H	L	L	H	H
8	L	L	L	H	H
7	H	H	H	L	H
6	L	H	H	L	H
5	H	L	H	L	H
4	L	L	H	L	H
3	H	H	L	L	H
2	L	H	L	L	H
1	H	L	L	L	H
0	L	L	L	L	L

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

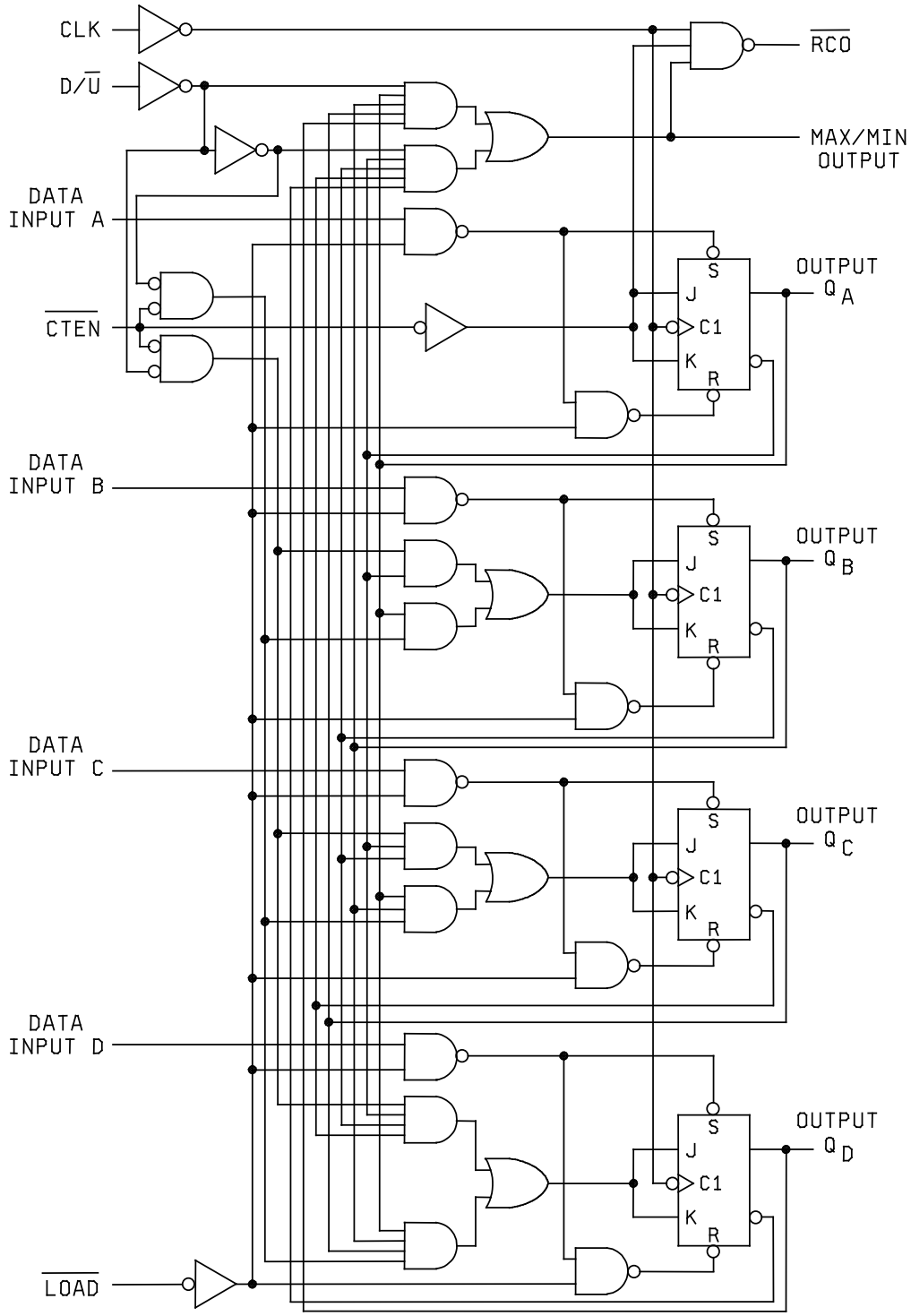


FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9
Group C end-point electrical parameters (method 5005)	1, 2, 3, 10**, 11**
Group D end-point electrical parameters (method 5005)	1, 2, 3*

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-07-14

Approved sources of supply for SMD 76009 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
7600901EA	01295 3/ 3/	SNJ54LS191J 54LS191/BEAJC 54LS191/BEA	M38510/31509BEA
7600901FA	01295 3/ 3/	SNJ54LS191W 54LS191/BFA 54LS191/BFAJC	M38510/31509BFA
76009012A	01295 3/ 3/	SNJ54LS191EK 54LS191/B2A 54LS191M/B2AJC	M38510/31509B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243