REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
F	Convert to military drawing format. Add LCC package. Add logic diagram. Remove vendors CAGE 34335, 07263, 27014. Change Ident. No. to 67268.	87-10-08	M. A. Frye
G	Add another column for $\overline{CLR}$ input on the truth table (see figure 2). Add inversion circle on the CLR inputs of the flip flops (see figure 3). Editorial changes throughout the document.	88-04-11	M. A. Frye
H	Changes in accordance with NOR 5962-R178-92. --tvn	92-04-29	Monica L. Poelking
J	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	02-12-12	Raymond Monnin
K	Add class "V" to document. Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	04-01-20	Raymond Monnin
L	Update drawing to current requirements. Editorial changes throughout. - gap	10-05-06	Charles F. Saffle

CURRENT CAGE CODE 67268

The original first sheet of this drawing has been replaced.

REV																				
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REV																				
SHEET																				
REV STATUS				REV			L	L	L	L	L	L	L	L	L	L	L	L		
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12		

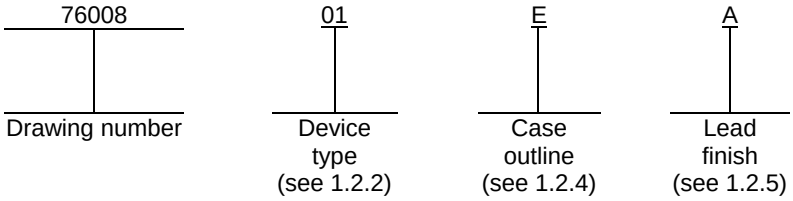
PMIC N/A	PREPARED BY W. A. Denick	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY R. F. Gonzales	
	APPROVED BY N. A. Hauck	MICROCIRCUIT, DIGITAL, LOW-POWER SCHOTTKY TTL, COUNTERS, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 76-03-19	
AMSC N/A	REVISION LEVEL L	SIZE A / CAGE CODE **14933** / **76008**
		SHEET 1 OF 12

1. SCOPE

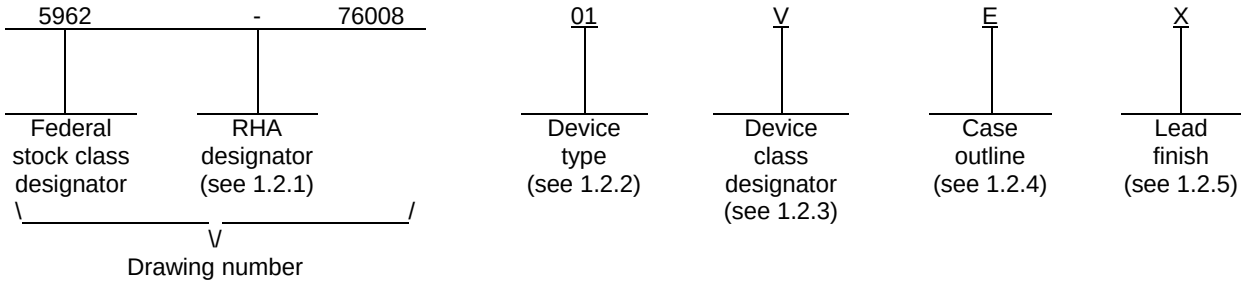
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54LS161	Synchronous, 4-bit binary counter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line package
F	GDFP2-F16 or CDFP3-F16	16	Flat package
2	CQCC1-N20	20	Square chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	176mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test e.g., I_{OS}.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit. The test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 12 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -400 µA V_{IN} = 0.7 V or 2.0 V		1, 2, 3	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4 mA V_{IN} = 0.7 V or 2.0 V		1, 2, 3		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA, T_C = +25°C		1		-1.5	V
High level input current at data, clear, or enable P	I_{IH1}	V_{CC} = 5.5 V, V_{IH} = 2.7 V		1, 2, 3		24	µA
High level input current at load, clock, or enable T	I_{IH2}			1, 2, 3		40	µA
High level input current at data, clear, or enable P	I_{IH3}	V_{CC} = 5.5 V, V_{IH} = 5.5 V		1, 2, 3		100	µA
High level input current at load, clock, or enable T	I_{IH4}			1, 2, 3		200	µA
Low level input current at data, clear, or enable P	I_{IL1}	V_{CC} = 5.5 V, V_{IL} = 0.4 V		1, 2, 3		-480	µA
Low level input current	I_{IL2}	V_{CC} = 5.5 V, V_{IL} = 0.4 V	Load, Enable T	1, 2, 3		-800	µA
	I_{IL3}		Clock	1, 2, 3		-1200	µA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V 1/		1, 2, 3	-6	-130	mA
High level supply current	I_{CCH}	V_{CC} = 5.5 V		1, 2, 3		31	mA
Low level supply current	I_{CCL}			1, 2, 3		32	mA
Functional tests		See 4.4.1c		7, 8			
Maximum clock frequency	F_{MAX}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9	25		MHz
				10, 11	15		MHz
			C_L = 50 pF ±10%	9	20		MHz
				10, 11	14		MHz
Propagation delay time, high-to-low level, clear to Q	t_{PHL1}		C_L = 15 pF ±10%	9		38	ns
				10, 11		53	ns
			C_L = 50 pF ±10%	9		43	ns
				10, 11		60	ns
Propagation delay time, low-to-high level, clock to carry	t_{PLH2}		C_L = 15 pF ±10%	9		35	ns
				10, 11		49	ns
			C_L = 50 pF ±10%	9		40	ns
				10, 11		56	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, high-to-low level, clock to carry	t_{PHL2}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5% 2/	C_L = 15 pF ±10%	9		35	ns
				10, 11		49	ns
			C_L = 50 pF ±10%	9		40	ns
				10, 11		56	ns
Propagation delay time, low-to-high level, clock (load input high) to Q	t_{PLH3}		C_L = 15 pF ±10%	9		24	ns
				10, 11		34	ns
			C_L = 50 pF ±10%	9		29	ns
				10, 11		41	ns
Propagation delay time, high-to-low level, clock (load input high) to Q	t_{PHL3}		C_L = 15 pF ±10%	9		27	ns
				10, 11		38	ns
			C_L = 50 pF ±10%	9		32	ns
				10, 11		45	ns
Propagation delay time, low-to-high level, clock (load input low) to Q	t_{PLH4}		C_L = 15 pF ±10%	9		25	ns
				10, 11		35	ns
			C_L = 50 pF ±10%	9		30	ns
				10, 11		42	ns
Propagation delay time, high-to-low level, clock (load input low) to Q	t_{PHL4}		C_L = 15 pF ±10%	9		29	ns
				10, 11		41	ns
			C_L = 50 pF ±10%	9		34	ns
				10, 11		48	ns
Propagation delay time, low-to-high level, enable T to carry	t_{PLH5}		C_L = 15 pF ±10%	9		23	ns
				10, 11		32	ns
			C_L = 50 pF ±10%	9		28	ns
				10, 11		39	ns
Propagation delay time, high-to-low level, enable T to carry	t_{PHL5}		C_L = 15 pF ±10%	9		23	ns
				10, 11		32	ns
			C_L = 50 pF ±10%	9		28	ns
				10, 11		39	ns

1/ Not more than one output should be shorted at a time, and the duration of the short-circuit condition should not exceed one second.

2/ Propagation delay time testing may be performed using either C_L = 15 pF or C_L = 50 pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50 pF load.

Device type 01		
Case outlines	E, F	2
Terminal number	Terminal symbols	Terminal symbols
1	$\overline{CLR}$ (clear)	N/C
2	CLK (clock)	$\overline{CLR}$ (clear)
3	A	CLK (clock)
4	B	A
5	C	B
6	D	N/C
7	ENP (enable P)	C
8	GND	D
9	$\overline{LOAD}$	ENP (enable P)
10	ENT (enable T)	GND
11	Q_D	N/C
12	Q_C	$\overline{LOAD}$
13	Q_B	ENT (enable T)
14	Q_A	Q_D
15	RCO	Q_C
16	V_{CC}	N/C
17		Q_B
18		Q_A
19		RCO
20		V_{CC}

FIGURE 1. Terminal connections.

$\overline{LOAD}$	Enable T	Enable P	$\overline{CLR}$	Action on the rising clock edge (⎍)
X	X	X	L	Reset (clear)
L	X	X	H	Load ($Data_n$ - - - - Q_n)
H	H	H	H	Count (increment)
H	L	X	H	No change (hold)
H	X	L	H	No change (hold)

H = High voltage level
L = Low voltage level
X = Don't care

FIGURE 2. Truth table.

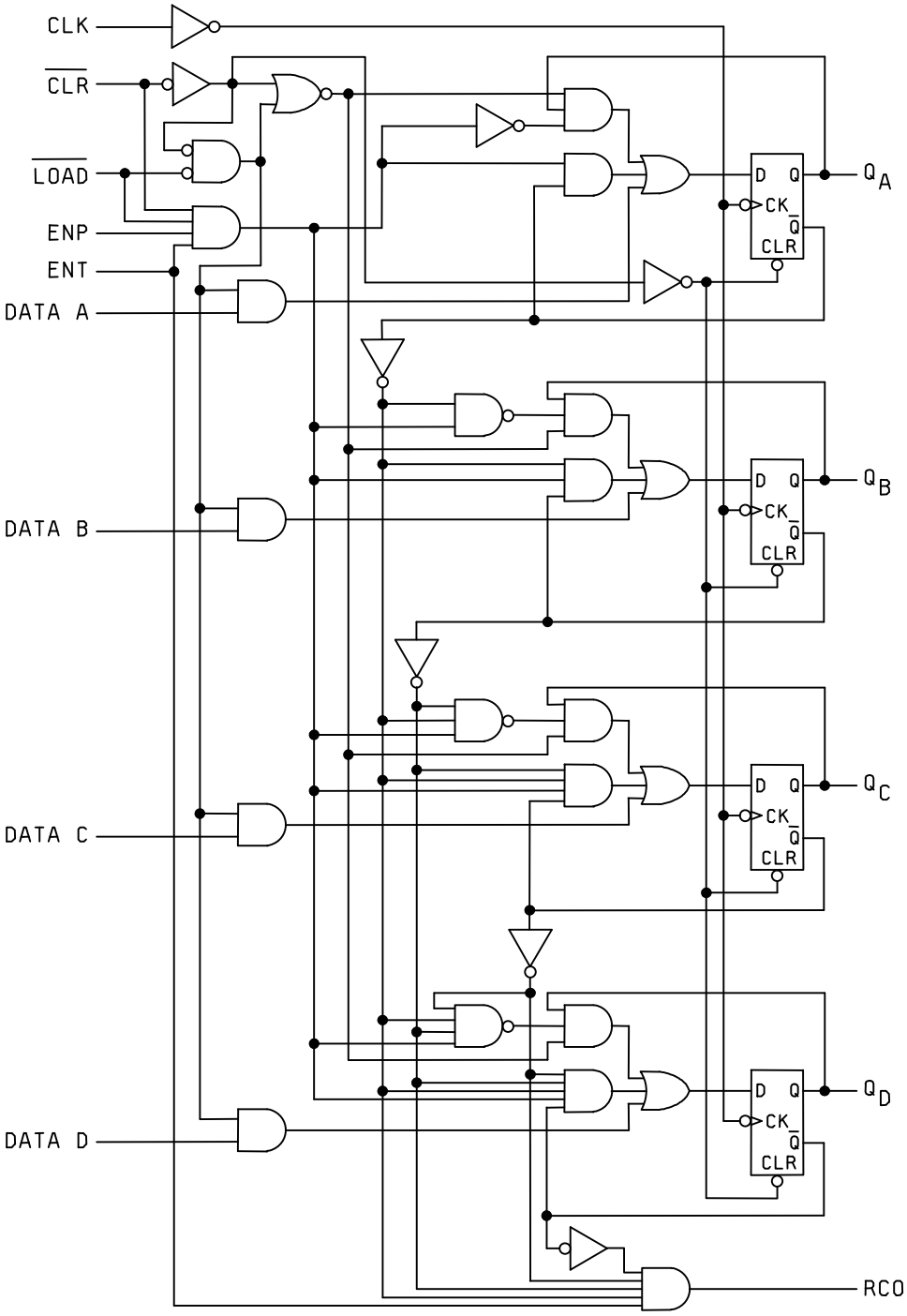
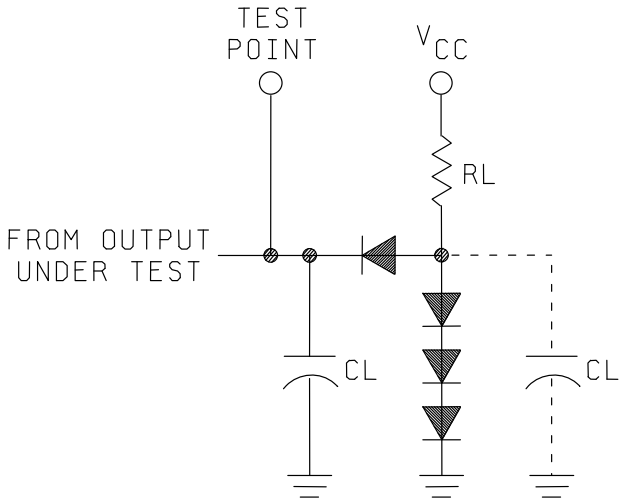


FIGURE 3. Logic diagram.



NOTE:

Propagation delay limits are based on single output switching.
The load circuit shall be as specified on figure 4 herein.
t_{PHL} and t_{PLH} voltage waveforms shall be in accordance with method 3003 of MIL-STD-883, with threshold voltage points at 50 percent:
$t_r \leq 15$ ns, $t_f \leq 6$ ns.

FIGURE 4. Test circuit,

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	- - -
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 9	1/ 3/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	3/ 1, 2, 3, 7, 8, 9, 10, 11	3/ 1, 2, 3, 7, 8, 9, 10, 11	3/ 1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8,
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.
b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-05-06

Approved sources of supply for SMD 76008 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
7600801EA	01295	SNJ54LS161AJ	M38510/31504BEA
	3/	54LS161A/BEAJC	
	3/	54LS161A/BEA	
	58625	SL54LS161/BEA	
5962-7600801VEA	01295	SNV54LS161AJ	- - -
7600801FA	01295	SNJ54LS161AW	M38510/31504BFA
	3/	54LS161A/BFA	
	3/	54LS161A/BFAJC	
	58625	SL54LS161/BFA	
5962-7600801VFA	01295	SNV54LS161AW	- - -
76008012A	01295	SNJ54LS161AFK	M38510/31504B2A
	3/	54LS161A/B2A	
	3/	54LS161AM/B2AJC	
	58625	SL54LS161/B2A	
76008012C	58625	SL54LS161/B2C	M38510/31504B2C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 POC U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493
58625	Lansdale Semiconductor Inc. 2412 W. Huntington Dr. Tempe, AZ 85282

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