REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Revision Status of Sheets

REV																					
SHEET																					
REV																					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18			

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
24-12-26

REVISION LEVEL
-

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR, RAIL-TO-RAIL INPUT AND OUTPUT, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-23214**

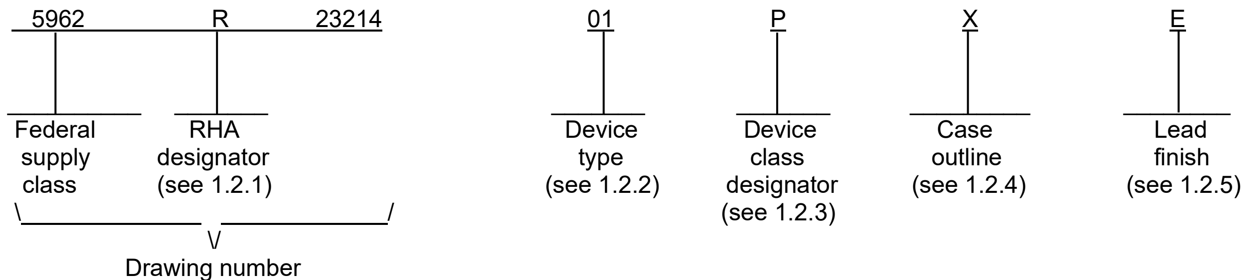
SHEET 1 OF 18

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents product assurance class levels consisting of high reliability (device class Q), space application (device class V or Y), and plastic encapsulated microcircuits (PEM) (device class N) for military, terrestrial and avionics application and device class P for space application. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device classes N and P, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. RHA marked devices classes are N, P, Q, Y, and V and meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	OPA4H199-SP	Radiation hardened, 40V, 4.5MHz, rail-to-rail input and output, low offset voltage, low noise, operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N or P	Certification and qualification to MIL-PRF-38535 for PEM performance environments.
Y	Certification and qualification to MIL-PRF-38535. Non hermetic flip chip technology on a ceramic or organic substrate.
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, JEDEC PUB 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	14	Plastic small outline transistor package (SOT-23)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, P, Q, Y, and V.

Finish designator	Material
A	Gold over Palladium over Nickel
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage, V_S = (V+) – (V-) .... 0 V to 42 V [0 V to ±21 V] 2/
Signal input pins:
Common-mode voltage .... [(V-) - 0.5] V to [(V+) + 0.5] V 3/
Differential voltage .... (V_S + 0.2) V maximum 3/
Current .... -10 mA to 10 mA 3/
Output short-circuit .... Continuous 4/
Junction temperature, T_J .... +150°C
Storage temperature, T_{stg} .... -65°C to +150°C
Electrostatic discharge (ESD):
Human body model (HBM) .... ±2 kV 5/
Charged device model (CDM) .... ±1 kV 6/

1.4 Recommended operating conditions.

Supply voltage (V_S) [(V+) - (V-)] .... 2.7 V to 40 V [±1.35 V to ±20 V] 2/
Input voltage range (V_I) .... [(V-) - 0.1] V to [(V+) + 0.1] V
Storage temperature range .... -65ºC to +150ºC
Case outline X:
Thermal resistance, junction-to-ambient (θ_{JA}) 121.6ºC/W
Thermal resistance, junction-to-case (θ_{JC})TOP 53.6ºC/W
Thermal resistance, junction-to-board (θ_{JB}) 47.8ºC/W
Characterization parameter, junction-to-top (ψ_{JT}) 2.1ºC/W
Characterization parameter, junction-to-board (ψ_{JB}) 47.6ºC/W
Ambient operating temperature range .... -55°C to +125°C
Glass Transition Temperature
Mold Compound (Tg) .... 110°C nominal 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Voltage range applies to the differential voltage [(V+) ─ (V-)] between supply pins.
3/ Short-circuit to ground, one amplifier per package. This device has been designed to limit electrical damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual thermal destruction.
4/ Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
5/ Human body model (HBM) tested per ANSI/ESDA/JEDEC JS-001 or TM 3015 of MIL-STD-883.
6/ Charged device model (CDM) tested per ANSI/ESDA/JEDEC JS-002.
7/ Glass transition temperature (T_g) of Mold compound measured spec value is 110°C but tested T_g is 135°C.

1.4.1 Typical operating performance.

Input offset voltage (V_{CM} = V-) .... +125 µV 8/
Input offset voltage drift .... +0.3 µV/°C 9/
Input offset voltage vs power supply (V_{CM} = V-, V_S = 4 V to 40 V) .... +0.3 µV/V 9/
Channel separation (f = 0 Hz) .... ±1 µV/V 8/
Input bias current .... ±10 pA 8/
Input offset current .... ±10 pA 8/
Input voltage noise (f = 0.1 Hz to 10 Hz) .... 1.8 µVpp 8/
Input voltage noise density (f = 1 kHz) .... 10.8 nV/√Hz 8/
Input voltage noise density (f = 10 kHz) .... 9.4 nV/√Hz 8/
Input current noise density (f = 1 kHz) .... 82 fA/√Hz 8/
Input voltage noise density (f = 10 kHz) .... 9.4 nV/√Hz 8/
Input current noise density (f = 1 kHz) .... 82 fA/√Hz 8/
Common-mode rejection ratio
V_S = 40 V, (V-) - 0.1 V < V_{CM} < (V+) – 2 V (Main input pair) .... 130 dB 9/
V_S = 4 V, (V-) - 0.1 V < V_{CM} < (V+) – 2 V (Main input pair) .... 100 dB 9/
V_S = 2.7 V, (V-) - 0.1 V < V_{CM} < (V+) – 2 V (Main input pair) .... 95 dB 9/
V_S = 2.7 V to 40 V, (V+) – 1V < V_{CM} < (V+) + 0.1 V (Aux input pair) .... 85 dB 9/
Differential input impedance .... 100 || 9 MΩ || pF 8/
Common-mode input impedance .... 6 || 1 TΩ || pF 8/
Open-loop voltage gain
V_S = 40 V, V_{CM} = V-, (V-) + 0.1V < V_O < (V+) – 0.1V .... 145 dB 8/
V_S = 40 V, V_{CM} = V-, (V-) + 0.1V < V_O < (V+) – 0.1V .... 142 dB 9/
V_S = 4V, V_{CM} = V-, (V-) + 0.1V < V_O < (V+) – 0.1V .... 130 dB 8/
V_S = 4V, V_{CM} = V-, (V-) + 0.1V < V_O < (V+) – 0.1V .... 125 dB 9/
V_S = 2.7 V, V_{CM} = V-, (V-) + 0.1V < V_O < (V+) – 0.1V .... 120 dB 8/
V_S = 2.7 V, V_{CM} = V-, (V-) + 0.1V < V_O < (V+) – 0.1V .... 118 dB 9/
Gain-bandwidth product .... 4.5 MHz 8/
Slew rate (V_S = 40 V, G = +1, C_L = 20 pF) .... 21 V/µs 8/
Settling time
To 0.01%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF .... 2.5 µs 8/
To 0.01%, V_S = 2 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF .... 1.5 µs 8/
To 0.1%, V_S = 40 V, V_{STEP} = 10 V, G = +1, C_L = 20 pF .... 2 µs 8/
To 0.1%, V_S = 40 V, V_{STEP} = 2 V, G = +1, C_L = 20 pF .... 1 µs 8/
Phase margin (G = +1, R_L = 10 kΩ, C_L = 20 pF) .... 60° 8/
Overload recovery time (V_{IN} x gain > V_S) .... 400 ns 8/
Total harmonic distortion + noise
V_S = 40 V, V_{OUT} = 3 V_{RMS}, G = +1, f = 1 kHz 0.00021% 8/, 9/
Voltage output swing from rail (positive and negative headroom)
V_S = 40 V, R_L = no load .... 5 mV 8/
V_S = 40 V, R_L = 10 kΩ .... 50 mV 8/
V_S = 40 V, R_L = 2 kΩ .... 300 mV 8/
V_S = 2.7 V, R_L = no load .... 1 mV 8/
V_S = 2.7 V, R_L = 10 kΩ .... 5 mV 8/
V_S = 2.7 V, R_L = 2 kΩ .... 25 mV 8/
Short-circuit current .... ±75 mA 8/
Capacitive load drive .... 1,000 pF 8/
Open-loop output impedance (f = 1 MHz, I_O = 0 A) .... 525 Ω 8/
Quiescent current per amplifier (V_{CM} = V-, I_O = 0 A) .... 560 µA 8/

8/ For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and device is connected in closed-loop feedback unless otherwise specified.
9/ For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = -55°C to 125°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and device is connected in closed-loop feedback unless otherwise specified.

1.5 Radiation features.

Maximum total dose available (effective dose rate = 165 mrad(Si)/s) .... 100 krad(Si) 10/

Maximum total dose available (low dose rate = 10 mrad(Si)/s) .... 100 krad(Si) 10/

Heavy ion Single event phenomenon (SEP) test:

No SEL occurs at effective LET (see 4.4.4.2) ....$\leq$ 65 MeV-cm^2 /mg 11/

Neutron/Displacement damage test (1-MeV equivalent): ....= 1 x 10^{13} n/cm^2 12/

10/ The manufacturer supplying device type 01 has performed characterization of BiCMOS (LBC9) technology total ionizing dose (TID) test in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 (condition A and condition D) to a maximum total dose of 100 krads(Si). The effective dose rate after 168 hours room temperature anneal is 165 mrad(Si)/s for device type 01 per MIL-STD-883, method 1019, condition A, paragraph 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower, environment. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019 to a maximum total dose of 100 krad(Si).

11/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Praseodymium (Pr) ion beams were used at an angle of incidence of 0° at flux of 10^5 ions/cm$^{2}\cdot$s, fluence level of 10^7 ions/cm^2. After the runs, no single event latch-up (SEL) were observed at an effective LET of 65 MeV·cm^2/mg under certain test conditions. For more information on SEE/SEP test please contact device manufacturer.

12/ Neutron/Displacement damaged dosimetry test was performed for BiCMOS(LBC9) technology devices in Fast Neutron Irradiation (FNI) facility of The University of Massachusetts Lowell. The results show that all devices were fully functional and within production test limits after having been irradiated up to 1 x 10^{13} n/cm^2 (1-MeV equivalent). A sample size of nine units was exposed to radiation testing per MIL-STD-883, Method 1017 for Neutron Irradiation, and an additional one device was used as a control unit and was not irradiated.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation *or contract*.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org).

JEDEC - SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC JS-002 – Electrostatic Discharge Sensitivity Testing - Charge Device Model (CDM)
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org/).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, P, Q, Y, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.6 Organic or polymeric materials in device type 01. For device type 01, plastic packages inherently use organic or polymeric materials (adhesives, mold compounds, underfill, organic substrates, etc.).

3.2.7 Internal lead wire and die bond pad materials in device type 01. For device type 01, plastic packages internal lead wire metals are dissimilar from the die metallization metal. Internal lead wire metal is Au and the die metallization metal is Al.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, P, Q, Y, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_A ≤ +125°C $T_A = T_J$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
OFFSET VOLTAGE							
Input offset voltage	V_{OS}	V_{CM} = V-	1	01	-925	925	µV
		V_{CM} = V-	1, 2, 3	01	-895	895	
Input offset voltage versus power supply	PSRR	V_{CM} = V-, V_S = 4 V to 40 V	1, 2, 3	01	-1	1	µV/V
		V_{CM} = V-, V_S = 2.7 V to 40 V	1, 2, 3		-5	5	
INPUT VOLTAGE RANGE							
Common-mode rejection ratio	CMRR	V_S = 40 V, (V-) - 0.1 V < V_{CM} < (V+) - 2 V (Main input pair)	1, 2, 3	01	107		dB
		V_S = 4 V, (V-) - 0.1 V < V_{CM} < (V+) - 2 V (Main input pair)			82		
		V_S = 2.7 V, (V-) - 0.1 V < V_{CM} < (V+) - 2 V (Main input pair)			75		
OPEN-LOOP GAIN							
Open-loop voltage gain	A_{OL}	V_S = 40 V, V_{CM} = V_- (V_-) + 0.1 V < V_O < (V_+) – 0.1 V	1	01	120		dB
		V_S = 4 V, V_{CM} = V_- (V_-) + 0.1 V < V_O < (V_+) – 0.1 V			104		
		V_S = 2.7 V, V_{CM} = V_- (V_-) + 0.1 V < V_O < (V_+) – 0.1 V			101		
OUTPUT							
Voltage output swing from rail	Positive and negative rail headroom	V_S = 40 V, R_L = no load	1	01		10	mV
		V_S = 40 V, R_L = 10 kΩ				70	
		V_S = 40 V, R_L = 2 kΩ				350	
		V_S = 2.7 V, R_L = no load				6	
		V_S = 2.7 V, R_L = 10 kΩ				12	
		V_S = 2.7 V, R_L = 2 kΩ				40	
POWER SUPPLY							
Quiescent current per amplifier	I_Q	V_{CM} = V–, I_O = 0 A	1	01		685	µA
			1, 2, 3			750	

1/ For V_S = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and device is connected in closed-loop feedback unless otherwise specified.

2/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and D. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP	Temperature	Conditions : Bias VIN = 40 V No SEL and SEB/SEGR were observed at effective LET
01	No SEL	125°C	LET ≤ 65 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Praseodymium (Pr) ion beams were used at an angle of incidence of 0° and 30° respectively at flux of 10^5 ions/cm^2·s, fluence level of 10^7 ions/cm^2. After the runs, no single event latch-up (SEL) were observed at an effective LET of 6**5** MeV·cm^2/mg under certain test conditions. For more information on SEE/SEP test please contact device manufacturer.

Case outline X

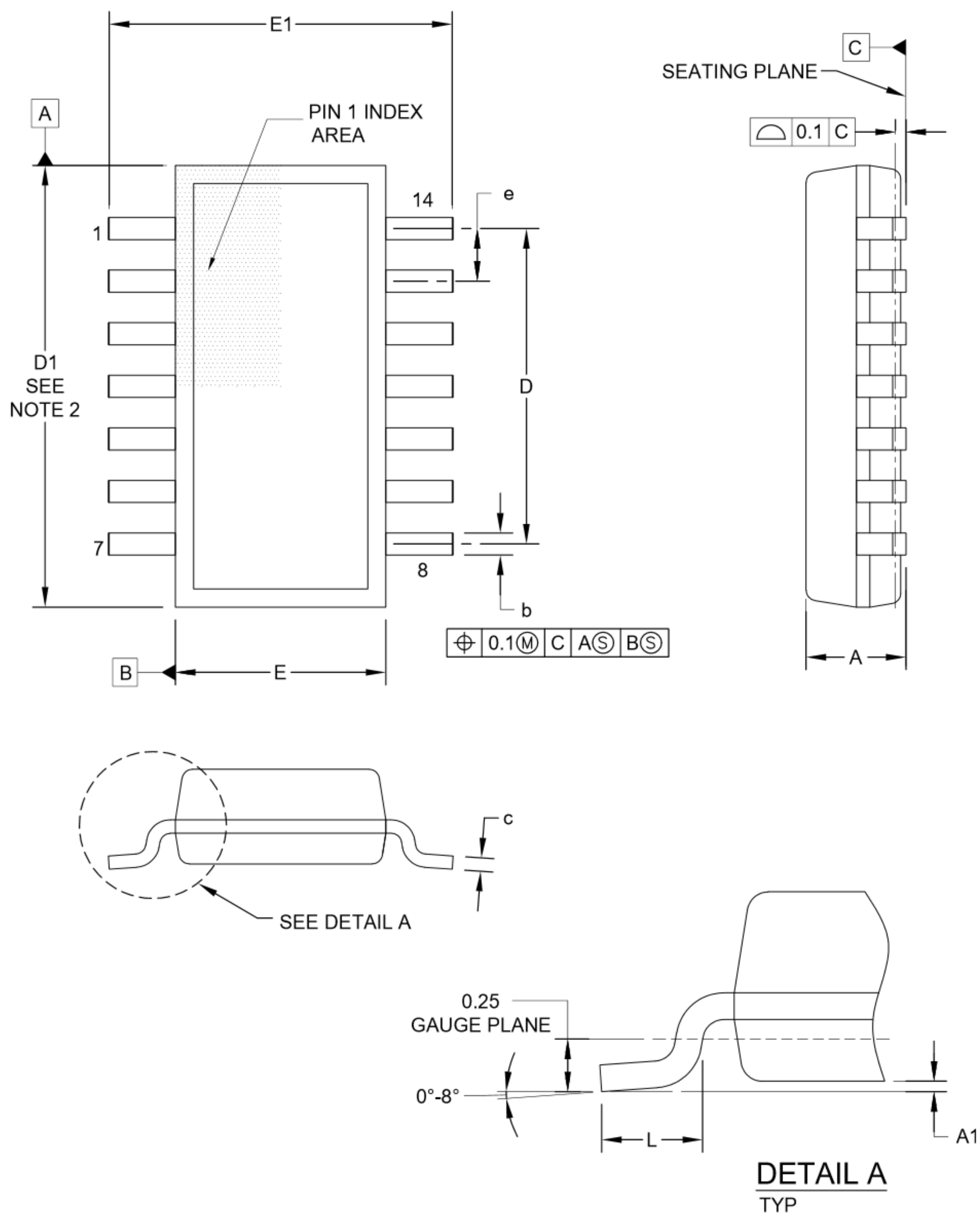


FIGURE 1. Case outline.

Case X - Continued

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	---	1.10	---	.0433
A1	0	.100	0	.0039
b	.110	.310	.0043	.0122
c	.080	.200	.0031	.0078
D	3.00 BSC		.1181 BSC	
D1	4.10	4.30	.1614	.1692
E	1.90	2.10	.0748	.0826
e	3.16	3.36	.1244	.1322
E1	.500 BSC		.0197 BSC	
L	.330	.630	.0130	.0248

NOTES:

1. Controlling dimensions are millimeters, inch dimensions are given for reference only.
2. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
3. Features may differ or may not be present.

Device types	01
Case outline	X
Terminal number	Terminal symbol
1	OUT1
2	IN1-
3	IN1+
4	V+
5	IN2+
6	IN2-
7	OUT2
8	OUT3
9	IN3-
10	IN3+
11	V-
12	IN4+
13	IN4-
14	OUT4

FIGURE 2. Terminal connections

Terminal symbol	I/O	Description
IN1+	I	Noninverting input, channel 1
IN1-	I	Inverting input, channel 1
IN2+	I	Noninverting input, channel 2
IN2-	I	Inverting input, channel 2
IN3+	I	Noninverting input, channel 3
IN3-	I	Inverting input, channel 3
IN4+	I	Noninverting input, channel 4
IN4-	I	Inverting input, channel 4
OUT1	O	Output, channel 1
OUT2	O	Output, channel 2
OUT3	O	Output, channel 3
OUT4	O	Output, channel 4
V+	-	Positive (highest) power supply
V-	-	Negative (lowest) power supply

FIGURE 2. Terminal connections – Continued

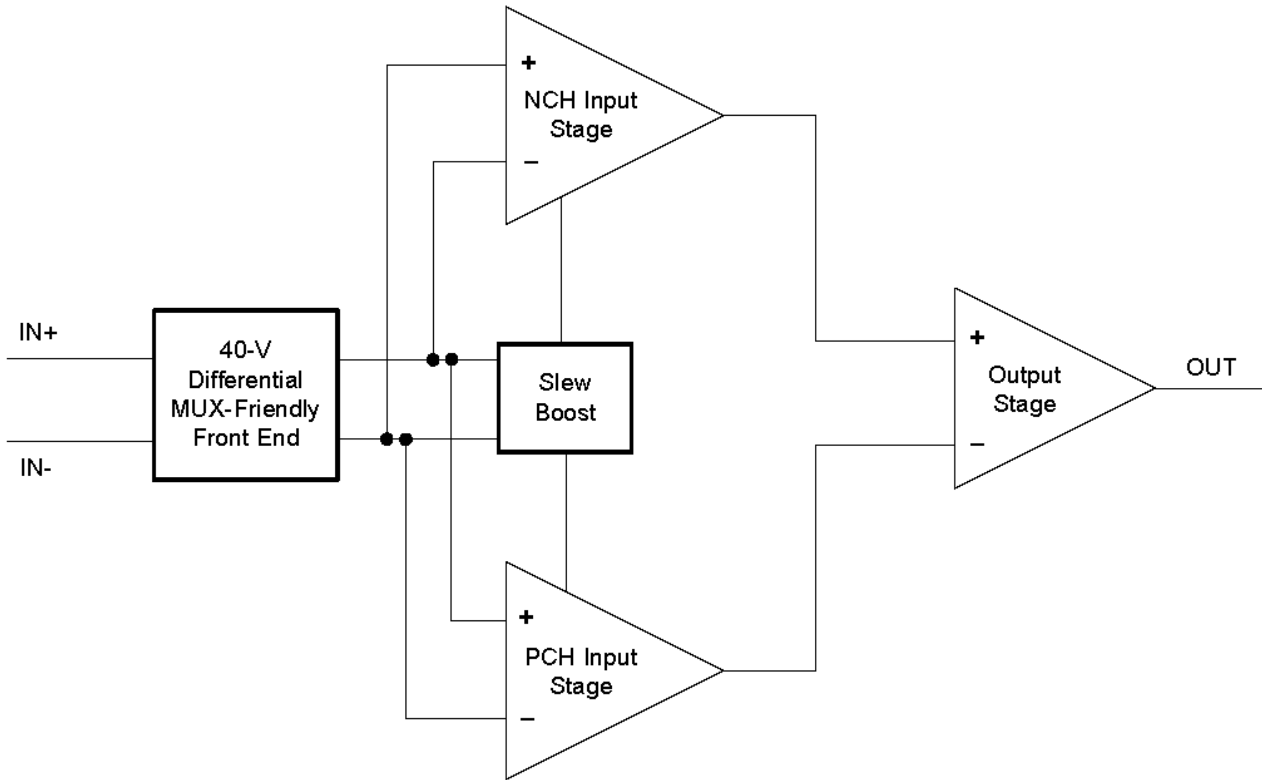


FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, P, Q, Y, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, P, Q, Y, and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, P, Q, Y and V.

a. Test condition A, B, C and D. Burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Unless otherwise specified in the QM plan, for devices class N, P, Q, Y, and V, dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

c. For devices class P, Y, and V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

4.3 Qualification inspection. Qualification inspection for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. Preconditioning shall be performed on non hermetic device classes N, P, and Y surface mount devices as specified in the manufacturer’s QM plan. Thermal shock is not applicable to class N, P, and organic class Y.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)				
	Device class N	Device class P	Device class Q	Device class V	Device class Y
Interim (pre burn-in) electrical parameters (see 4.2)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6
Post burn-in electrical parameters (see 4.2.1)	1,2,3,4,5,6 1/ 2/	1,2,3,4,5,6 1/ 2/	1,2,3,4,5,6 1/ 2/	1,2,3,4,5,6 1/ 2/	1,2,3,4,5,6 1/ 2/
Group A (Final electrical) test requirements (see 4.4.1)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4.2)	1,2,3,4,5,6 2/	1,2,3,4,5,6 2/	1,2,3,4,5,6 2/	1,2,3,4,5,6 2/	1,2,3,4,5,6 2/
Group D end-point electrical parameters (see 4.4.3)	1,4	1,4	1,4	1,4	1,4
Group E end-point electrical parameters (see 4.4.4)	1,4	1,4	1,4	1,4	1,4

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in Table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. 1/ 2/ 3/

Parameters	Symbol	Delta limits	Units
Quiescent current per amplifier	I_Q	±85	µA
Input offset voltage	V_{OS}	±550	µV

1/ 240 hour burn in and group C end point electrical parameters.
Deltas are performed at T_A = +25°C.

2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in electrical limit.

3/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall correspond to the test defined in TABLE IA (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table IA.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. RHA levels for device classes N, P, Q, Y, and V, shall be as specified in MIL-PRF-38535 and the end-point electrical parameters subgroups shall be as specified in table IIA herein.

b. For device classes N, P, Q, Y, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and condition D and as specified herein (see 1.5).

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 or JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C ±10°C for single event upset testing and at the maximum rated operating temperature ±10°C for single event latch up testing.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

4.4.4.3 Neutron /Displacement damaged dosimetry testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ±5°C after an exposure of 1 x 10^{13} neutrons/cm^2 (minimum).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 General applications: The manufacturer is supplying this SMD device as a high-performing space-grade high voltage (40 V) general purpose operational amplifier for space application. The device offers exceptional DC precision and AC performance and is suitable for supporting low earth orbit space applications, space sensor and control (telemetry), satellite electrical power system (EPS), flight control, satellite command & data handling, and satellite payloads.

6.1.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply. Sources of supply for device classes N, P, Q, Y, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-12-26

Approved sources of supply for SMD 5962-23214 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R2321401PXE	01295	OPA4H199-SP

1/ The lead finish shown for each PIN is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. 12500 T I Blvd Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.