REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
24-09-25

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR, BiCMOS, 2.5 V to 14 V, 2 AMP, LOW DROPOUT REGULATOR, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL	SIZE A	CAGE CODE **67268**	**5962-23203**
		SHEET 1 OF 20		

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	R	23203	01	V	X	C
Federal supply class	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

_______________ _______________/
V
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H1121-SP	Radiation hardened, BiCMOS, 2.5 V to 14 V, 2 amp, low dropout regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	22	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Input voltage supply:	
Supply voltage (IN), STAB	-0.3 V to 16 V
Enable (EN), Power good (PG)	-0.3 V to 7.5 V
Feedback (FB), Current limit (CL)	-0.3 V to 3.3 V
Output voltage:	
Regulated output (OUT)	-0.6 V to 16 V
Linear dropout voltage (VLDO)	-0.3 V to 3.6 V
Soft start (SS)	-0.3 V to 3.3 V
PG input current	-1 mA to 10 mA
OUT output current	-3.9 A to 3.9 A
Maximum operating junction temperature range (T_J)	-55°C to +150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to ambient ($R_{\theta JA}$)	30.5°C/W
Thermal resistance, junction to case (top) ($R_{\theta JC(top)}$)	13.3°C/W
Thermal resistance, junction to board ($R_{\theta JB}$)	13.5°C/W
Characterization parameter, junction to top (Ψ_{JT})	5.0 °C/W
Characterization parameter, junction to board (Ψ_{JB})	13.3°C/W
Thermal resistance, junction to case (bottom) ($R_{\theta JC(bot)}$)	4.1°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HBM)	±2000 V 3/
Charge device model (CDM)	±1000 V 4/

1.4 Recommended operating conditions.

Input voltage:	
IN	2.25 V to 14 V
EN, PG	0 V to 7 V
Output voltage:	
Regulated output (OUT)	0.6 V to V_{IN} - V_{DO} V
Soft start (SS)	0 V to 1.2 V
PG input current	0 mA to 2 mA
OUT output current	0 A to 2 A
Operating junction temperature range (T_J)	-55°C to +125°C

1/ Operation outside the absolute maximum ratings may cause permanent damage to the device. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under recommended operating conditions. If used outside the recommended operating conditions but within the absolute maximum ratings, the device may not be fully functional, and this may affect device reliability functionality, performance, and shorten the device lifetime.

2/ All voltage values are with respect to GND

3/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rad(Si)/s) .... 100 krad(Si) 5/

Heavy ion single event phenomenon (SEP):

No Single event latch-up (SEL) occurs at effective LET (see 4.3) .... $\leq$ 75 MeV·cm^2/mg 6/

No Single event burnout (SEB) occurs at effective LET (see 4.3) .... $\leq$ 75 MeV·cm^2/mg 6/

No Single event gate rupture (SEGR) occurs at effective LET (see 4.3) .... $\leq$ 75 MeV·cm^2/mg 6/

Neutron/Displacement damage test (1-MeV equivalent): .... = 1 x 10^{13} n/cm^2 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

5/ The manufacturer supplying 7th generation BiCMOS (LBC7) technology (which is over 99% CMOS components) devices performed total ionizing dose (TID) characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads(Si). However, device type 01 is irradiated at dose rate = 50 - 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A to TID level as specified. For more information on TID test report, please contact device manufacturer.

6/ The heavy-ion tests were performed at TAMU Cyclotron Radiation Effects Facility using Holmium (^{165}Ho) ion beam and Michigan State University (MSU) Facility for Rare Isotope Beams (FRIB) using Thulium (^{169}Tm) ion beam. For both ions, the angle of incidence was 0° at flux of approximately 10^5 ions/cm^2·s, fluence level of 10^7 ions/cm^2, and a temperature of 125°C. No single event latch-up (SEL) was observed at LET of 75 MeV·cm^2/mg. Manufacturer also tests Single event burnout (SEB) and Single event gate rupture (SEGR) test with Holmium (^{165}Ho) and Thulium (^{169}Tm) ion beams at an angle of incidence of 0°. No SEB/SEGR observed up to LET of 75 MeV·cm2/mg. For more information on SEE/SEP test please contact device manufacturer.

7/ Neutron/Displacement damaged dosimetry test was performed in Fast Neutron Irradiation (FNI) facility of The University of Massachusetts Lowell. The results show that all devices were fully functional and within production test limits after having been irradiated up to 1 × 10^{13} n/cm^2 (1-MeV equivalent). A sample size of nine units was exposed to radiation testing with guidance from MIL-STD-883, method 1017 for Neutron Irradiation, and an additional one device was used as a control unit and was not irradiated. For more information on Neutron test please contact device manufacturer.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation *or contract*.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org).

JEDEC - SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org/).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIB. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device Type	Limits Min	Limits Max	UNIT
POWER SUPPLIES AND CURRENTS								
Dropout voltage $V_{DO} = V_{IN(forced)} - V_{OUT(set)}$ 3/	V_{DO}	$V_{OUT(set)}$ = 2.25 V, $V_{OUT(measured)}$ = 98% x $V_{OUT(NOM)}$,	I_{OUT} = 100 mA	1, 2, 3	01		60	mV
			I_{OUT} = 250 mA	1, 2, 3	01		141	
			I_{OUT} = 500 mA	1, 2, 3	01		280	
			I_{OUT} = 1 A	1, 2, 3	01		570	
		$V_{OUT(set)}$ = 2.5 V, $V_{OUT(measured)}$ = 98% x $V_{OUT(NOM)}$,	I_{OUT} = 1.5 A	1, 2, 3	01		750	mV
			I_{OUT} = 2 A	1, 2, 3	01		900	
		$3 \le V_{OUT(set)} \le 13.3$ V, $V_{OUT(measured)}$ = 98% x $V_{OUT(NOM)}$	I_{OUT} = 100 mA	1, 2, 3	01		50	mV
			I_{OUT} = 250 mA	1, 2, 3	01		100	
			I_{OUT} = 500 mA	1, 2, 3	01		180	
			I_{OUT} = 1 A	1, 2, 3	01		340	
			I_{OUT} = 1.5 A	1, 2, 3	01		490	
			I_{OUT} = 2 A	1, 2, 3	01		700	
Programmed current limit	I_PCL	V_{IN} = 3.3 V, $V_{OUT(short)}$ = 0.1 V	RCL = 442 kΩ	1, 2, 3	01	0.19	0.45	A
			RCL = 174 kΩ	1, 2, 3	01	0.485	1.01	
			RCL = 82.5 kΩ	1, 2, 3	01	1.16	1.94	
			RCL = 41.2 kΩ	1, 2, 3	01	2.4	3.6	
Quiescent current	I_Q	V_{EN} = 7 V, I_{OUT} = 0 A		1, 2, 3	01		15	mA
Ground current	I_GND ($I_{IN} - I_{OUT}$)	V_{EN} = 7 V	I_{OUT} = 1 A	1, 2, 3	01		18	mA
			I_{OUT} = 2 A	1, 2, 3	01		20	mA
Internal linear regulator output voltage	VLDO	V_{IN} = 2.25 V		1, 2, 3	01	2.05	2.25	V
		$3 V \le V_{IN} \le 14$ V		1, 2, 3	01	2.3	2.78	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device Type	Limits Min	Limits Max	UNIT
Shutdown current	I_{SHDN}	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V		1, 2, 3	01		775	μA
Feedback leakage current	I_{FB}	V_{FB} = 0.7 V		1, 2, 3	01		15	nA
ACCURACY								
Output voltage accuracy	V_{ACC}	10 mA ≤ I_{OUT} ≤ 2 A, 0.6 V ≤ V_{OUT} ≤ V_{IN} – V_{DO}, P_D ≤ 3 W 4/	3 V ≤ V_{IN} ≤ 14 V	1, 2, 3	01	-1.5%	1.5%	
			3 V ≤ V_{IN} ≤ 14 V, T_A = 25°C	1	01	-1.1%	1.1%	
			2.25 V ≤ V_{IN} ≤ 3 V	1, 2, 3	01	-1.8%	1.8%	
Feedback voltage	V_{FB}	3V ≤ V_{IN} ≤ 14V		1, 2, 3	01	0.588	0.606	V
			T_A = 25°C	1	01	0.591	0.603	
		2.25V ≤ V_IN ≤ 3V		1, 2, 3	01	0.586	0.608	
Line regulation	$\Delta V_{OUT}/\Delta V_{IN}$	3V ≤ V_{IN} ≤ 14V		1, 2, 3	01		650	μV/V
		2.25V ≤ V_{IN} ≤ 3V		1, 2, 3	01		1800	
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	10 mA ≤ I_{OUT} ≤ 2 A, V_{IN} = 5 V, V_{OUT} = 3.3 V		1, 2, 3	01		16	mV/A
ENABLE								
Enable rising threshold (turn-on)	$V_{EN(rising)}$			1, 2, 3	01	0.565	0.625	V
Enable falling threshold (turn-off)	$V_{EN(falling)}$			1, 2, 3	01	0.465	0.52	V
EN propagation delay	$t_{EN(delay)}$	EN high to V_{OUT} = 10 mV, See figure 4		9, 10, 11	01		150	μs
Enable leakage current	$I_{EN(LKG)}$	V_{EN} = 7 V		1, 2, 3	01		30	nA
POWER GOOD								
Power good rising as percent of V_OUT	V_{PG_RISE}			1, 2, 3	01	93%	97%	
Power good falling as percent of V_OUT	V_{PG_FALL}			1, 2, 3	01	88.5%	94%	
Power good output low	$V_{PG(OL)}$	$I_{PG(SINK)}$ = 2 mA		1, 2, 3	01		190	mV

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device Type	Limits Min	Limits Max	UNIT
POWER GOOD – continued.								
Minimum V_IN for valid PG (V_PG < 0.5 V)	$V_{IN(MIN\_PG)}$	$I_{PG(SINK)}$ = 0.5 mA		1, 2, 3	01		0.8	V
Power good leakage	$I_{PG(LKG)}$	V_{PG} = 7 V, V_{FB} = 0.7 V		1, 2, 3	01		2	µA
SOFT START								
Soft-start current	I_{SS}			1, 2, 3	01	1.4	2.7	µA
Soft-start time	t_{SS}	V_{IN} = 5 V, V_{OUT} = 3.3 V, measured from V_{OUT} = 10 mV to PG assert, See figure 4	C_{SS} = 1 nF	9, 10, 11	01	0.22	0.48	ms
			C_{SS} = 33 nF	9, 10, 11	01	5.5	14.5	

1/ Over 2.25 V ≤ V_{IN} ≤ 14 V, $V_{OUT(set)}$ ≤ V_{IN} – 0.5V, I_{OUT} = 10 mA, C_{OUT} = 47 µF, over operating temperature range, T_A = – 55°C to 125°C, unless otherwise noted.

2/ Devices supplied to this drawing have been testing TID through all levels M, D, P, L and R of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA.
When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

3/ PD is the internal power dissipation. When PD exceeds 3W, the current is lowered to avoid excessive local heating (due to tester limitations).

4/ $V_{OUT(SET)}$ is the output voltage the regulator is configured using the feedback resistors, $V_{OUT(NOM)}$ is the measured output voltage. V_{IN} is set 2 V above the output (limited to 14 V maximum) and is decreased to the output voltage set point, $V_{OUT(SET)}$. When V_{OUT} falls to 98% of the nominal value, $V_{OUT(NOM)}$, the dropout voltage is recorded.

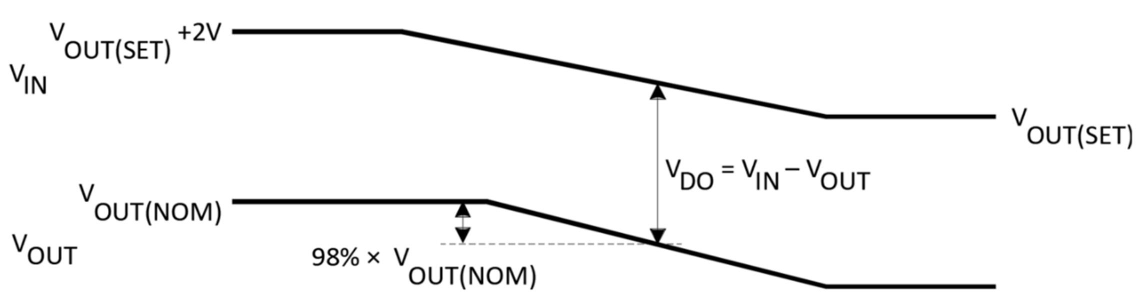

Table IB. SEP test limits 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_A)	V_{IN}	Effective linear energy transfer (LET)
01	No SEL	125°C	14 V	≤ 75 MeV·cm^2/mg
	No SEB	25°C	14 V	≤ 75 MeV·cm^2/mg
	No SEGR	25°C	14 V	≤ 75 MeV·cm^2/mg

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ The heavy-ion tests were performed at TAMU Cyclotron Radiation Effects Facility using Holmium (^{165}Ho) ion beam and Michigan State University (MSU) Facility for Rare Isotope Beams (FRIB) using Thulium (^{169}Tm) ion beam. For both ions, the angle of incidence was 0° at flux of approximately 10^5 ions/cm^2·s, fluence level of 10^7 ions/cm^2, and a temperature of 125°C. No single event latch-up (SEL) was observed at LET of 75 MeV·cm^2/mg. Manufacturer also tests Single event burnout (SEB) and Single event gate rupture (SEGR) test with Holmium (^{165}Ho) and Thulium (^{169}Tm) ion beams at an angle of incidence of 0°. No SEB/SEGR observed up to LET of 75 MeV·cm^2/mg. For more information on SEE/SEP test please contact device manufacturer.

Case X

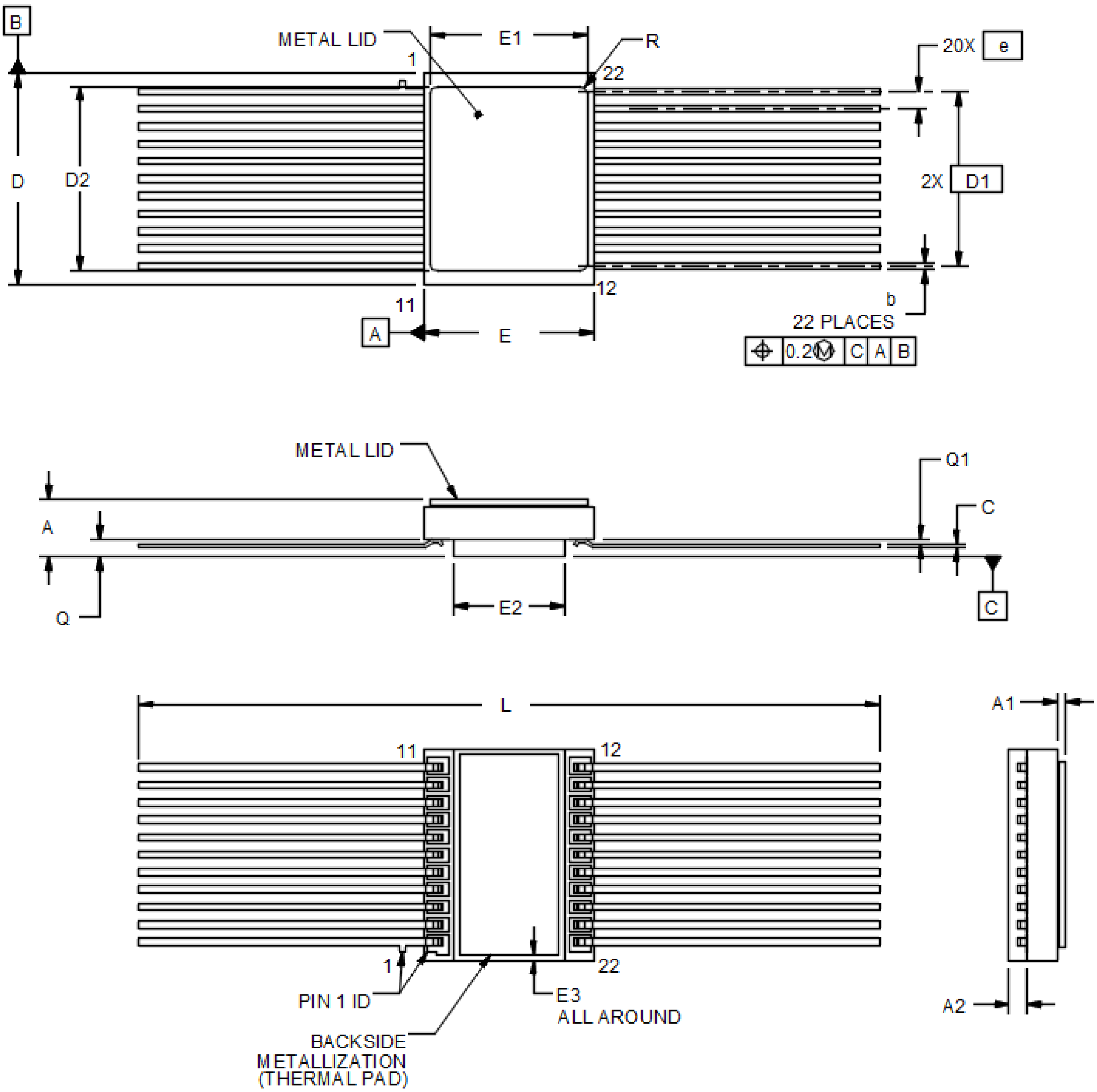

FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-23203**
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Case X - Continued

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.728	2.428	.068	.096
A1	.300 REF		.012 REF	
A2	.635 REF		.025 REF	
b	.204	.304	.008	.012
c	.097	.177	.004	.007
D	7.446	7.946	.293	.313
D1	6.35 BSC		.250 BSC	
D2	6.73 REF		.265 REF	
E	5.961	6.461	.235	.254
E1	5.70 REF		.224 REF	
E2	3.876	4.176	.153	.164
E3	.203 REF		.008 REF	
e	.635 BSC		.025 BSC	
L	26.50	27.50	1.04	1.08
Q	.555	.715	.022	.028
Q1	.053	.353	.002	.014
R	.250 REF		.010 REF	

NOTE:
Controlling dimensions are millimeters, inch dimensions are given for reference only.

FIGURE 1. Case outline – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	EN	I	Enable. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device. If enable functionality is not required, connect this pin to IN using a resistor divider network. Do not float this pin.
2	IN	I	Input power. An input capacitor (nominally 10µF) near this pin is recommended.
3	IN	I	Input power. An input capacitor (nominally 10µF) near this pin is recommended.
4	IN	I	Input power. An input capacitor (nominally 10µF) near this pin is recommended.
5	IN	I	Input power. An input capacitor (nominally 10µF) near this pin is recommended.
6	IN	I	Input power. An input capacitor (nominally 10µF) near this pin is recommended.
7	IN	I	Input power. An input capacitor (nominally 10µF) near this pin is recommended.
8	SS	I/O	Soft-start. A minimum 1nF capacitor is required to prevent excessive inrush currents.
9	GND	---	Ground
10	CL	I	Programmable current limit. A resistor to GND sets the over-current limit activation point. The range of resistor that can be used on the CL terminal to GND is 41.2 kΩ to 442 kΩ.
11	STAB	I/O	Stability pin. This is an output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Standard compensation networks can be applied to the STAB; however, an output capacitance of 22 µF to 220 µF typically achieve high stability margins.
12	FB	I	The output voltage feedback input through voltage dividers.
13	GND	---	Ground
14	GND	---	Ground
15	VLDO	O	Output of internal linear regulator, requires a 470 nF capacitor connected to ground.
16	OUT	O	Output power pin. The regulated output voltage. A single 47 µF tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22 µF and 220 µF are generally supported without additional compensation and wider ranges are supported with use of the STAB pin.

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
17	OUT	O	Output power pin. The regulated output voltage. A single 47 µF tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22 µF and 220 µF are generally supported without additional compensation and wider ranges are supported with use of the STAB pin.
18	OUT	O	Output power pin. The regulated output voltage. A single 47 µF tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22 µF and 22 0µF are generally supported without additional compensation and wider ranges are supported with use of the STAB pin.
19	OUT	O	Output power pin. The regulated output voltage. A single 47 µF tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22 µF and 220 µF are generally supported without additional compensation and wider ranges are supported with use of the STAB pin.
20	OUT	O	Output power pin. The regulated output voltage. A single 47µF tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22 µF and 220 µF are generally supported without additional compensation and wider ranges are supported with use of the STAB pin.
21	OUT	O	Output power pin. The regulated output voltage. A single 47 µF tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22 µF and 220 µF are generally supported without additional compensation and wider ranges are supported with use of the STAB pin.
22	PG	I/O	Power good indicator. This is an open drain pin. Use a pull-up resistor or a resistor divider (to ensure pin voltage does not exceed 7 V) to achieve desired logic level when tied to VOUT. It is recommended to pull down PG to ground if left unused, the PG pin can be left floating if necessary. When the output reaches 95% (typ) of the set output voltage the PG pin is asserted.

FIGURE 2. Terminal connections – continued.

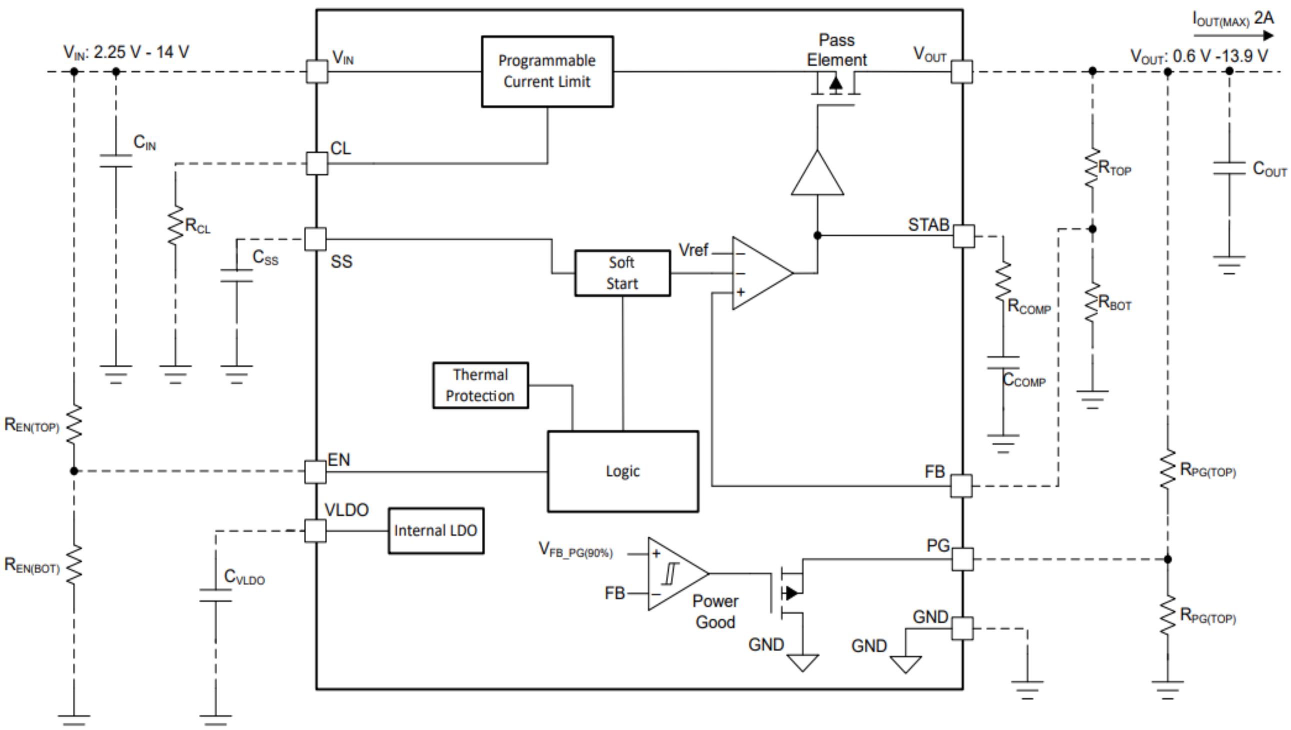
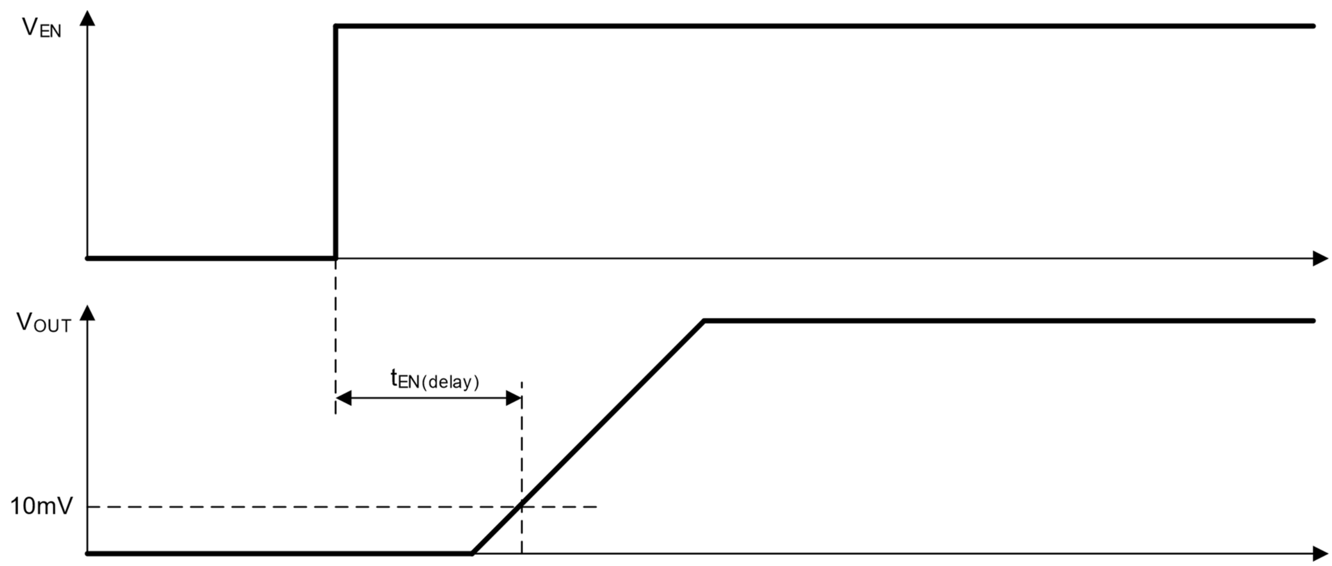
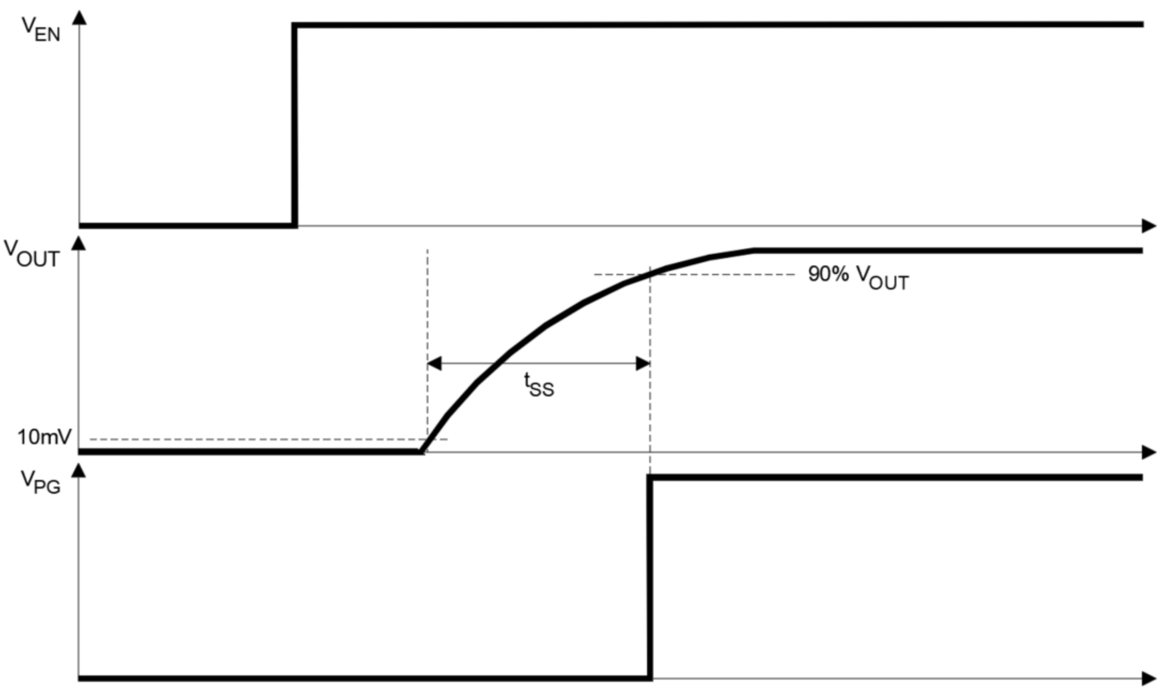


FIGURE 3. Block diagram.



Enable propagation delay

FIGURE 4. Timing waveforms.



Soft start time

FIGURE 4. Timing waveforms - continued.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Final electrical parameters (see 4.2)	1, 2, 3, 9, 10, 11 1/	1, 2, 3, 9, 10, 11 1/ 2/
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11 2/
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in Table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. 1/ 2/ 3/

Parameters	Symbol	Test condition	Delta limits	Units
Dropout voltage	V_{DO}	$V_{OUT(set)}$ = 2.5 V, $V_{OUT(measured)}$ = 98% x $V_{(OUT)NOM}$	±40	mV
Quiescent current	I_Q	V_{EN} = 7 V, I_{OUT} = 0 A	±400	µA
Shutdown current	I_{SHDN}	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V	±40	µA

1/ 240 hour burn-in and group C end point electrical parameters. Deltas are performed at T_A = +25°C.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in electrical limit.
3/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall correspond to the test defined in TABLE IA (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table IA.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and D, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C ±10°C for SET, SEB, and SEGR testing and at the maximum rated operating temperature ±10°C for SEL testing.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

4.4.4.3 Neutron /Displacement damaged dosimetry testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25°C ±5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-09-25

Approved sources of supply for SMD 5962-23203 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R2320301VXC	01295	TPS7H1121-SP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. 12500 TI Blvd Dallas, TX 75243