REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02 and 03.	24-03-06	Muhammad A. Akbar

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
23-12-01

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR BiCMOS, RADIATION HARDENED, HALF BRIDGE GaN FET GATE DRIVER, MONOLITHIC SILICON

AMSC N/A

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-22201**

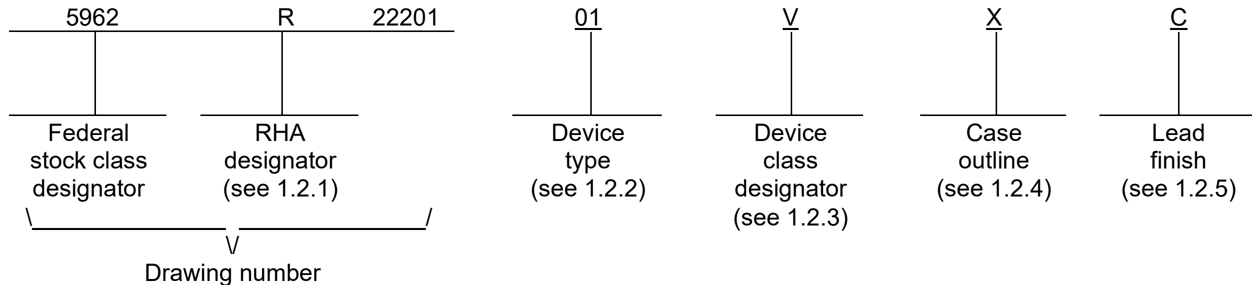
SHEET 1 OF 22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H6003-SP	Radiation Hardness Assured 200-V, 1.3-A, 2.5-A, Half Bridge GaN FET Gate Driver
02	TPS7H6013-SP	Radiation Hardness Assured 60-V, 1.3-A, 2.5-A, Half Bridge GaN FET Gate Driver
03	TPS7H6023-SP	Radiation Hardness Assured 22-V, 1.3-A, 2.5-A, Half Bridge GaN FET Gate Driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device type	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Ceramic flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

VIN to AGND	-0.3 V to 16 V
BP7L to AGND	-0.3 V to 8 V
BP5L to AGND	-0.3 V to 7 V
BP5H to SW	-0.3 V to 7 V
BOOT to SW	-0.3 V to V_{SW} + 16 V
EN_HI	-0.3 V to 16 V
PWM_LI	-0.3 V to 16 V
DHL, DLH	-0.3 V to V_{BP5L} + 0.3 V
LOH, LOL	-0.3 V to V_{BP5L} + 0.3 V
HOH, HOL	V_{SW} – 0.3 V to V_{BP5H} + 0.3 V
PGOOD	-0.3 V to V_{BP5L} + 0.3 V
SW to AGND (TPS7H6003-SP)	-10 V to 200 V
SW to AGND (TPS7H6013-SP)	-10 V to 60 V
SW to AGND (TPS7H6023-SP)	-10 V to 22 V
BOOT to AGND (TPS7H6003-SP)	0 V to 216 V
BOOT to AGND (TPS7H6013-SP)	0 V to 76 V
BOOT to AGND (TPS7H6023-SP)	0 V to 38 V
BST to AGND	-0.3 V to 16 V
BST current (3-μ transient pulse, non-repetitive)	4-A maximum
Operating junction temperature	-55 ºC to 150 ºC
Storage temperature, Tstg	-65 ºC to 150 ºC
Electrostatic discharge (ESD) ratings:	
Human body model (HBM), all pins	± 2000 V 2/
Charged device model (CDM), all pins	± 500 V 3/
Thermal characteristics:	
Junction-to-ambient thermal resistance, $R_{\theta JA}$	22.3 °C/W
Junction-to-case (top) thermal resistance, $R_{\theta JC(top)}$	7.1 °C/W
Junction-to-case (bottom) thermal resistance, $R_{\theta JC(bot)}$	6.2 °C/W
Junction-to-board thermal resistance, $R_{\theta JB}$	8.5 °C/W
Junction-to-top characterization parameter, $\Psi_{\theta JT}$	3.7 °C/W
Junction-to-board characterization parameter, $\Psi_{\theta JB}$	8.3 °C/W

1.4 Recommended operating conditions.

VIN to AGND	10 V to 14 V
EN_HI	0 V to 14 V
PWM_LI	0 V to 14 V
BOOT to SW	V_{SW} + 8 V to V_{SW} + 14 V
SW (TPS7H6003-SP)	-10 V to 150 V
SW (TPS7H6013-SP)	-10 V to 45 V
SW (TPS7H6023-SP)	-10 V to 14 V
SW slew rate	100 V/ns maximum
VIN slew rate	0.03 V/μs maximum
PWM_LI, EN_HI slew rate	2 V/μs minimum
Operating junction temperature	-55 ºC to 125 ºC

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

3/ Per ANSI/ESDA/JEDEC JS-002. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

1.5 Radiation Features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) .... 100 krad (Si) 4/
Single event phenomenon (SEP):
No SEL occurs at effective linear energy transfer (LET) (see 4.4.4.2) .... ≤ 75 MeV/(mg/cm^2) 5/
No SEB observed at effective LET (see 4.4.4.2) .... ≤ 75 MeV/(mg/cm^2) 5/
No SEGR observed at effective LET (see 4.4.4.2) .... ≤ 75 MeV/(mg/cm^2) 5/
Neutron Displacement Damage Test (1 MeV equivalent) .... $1x10^{13}$ n/cm^2 6/

4/ The device type 01, 02, and 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads (Si).

5/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Holmiun (^{165}Ho) ion beam was used at an angle of incidence of 0° at flux of 10^5 ions/cm^2·s, fluences level of 10^7 ions/cm^2 and a temperature of 125°C and no single event latch-up (SEL) was observed at LET of 75 MeV/(mg/cm^2). Manufacturer also test Single event burnout (SEB) and Single event gate rupture (SEGR) test with Holmiun (^{165}Ho) ion beam at an angles of incidence of 0°. No SEB/SEGR observed up to LET of 75 MeV/(mg/cm^2). For more information on SEE/SEP test please contact device manufacturer.

6/ Neutron/Displacement damaged dosimetry test was performed in Fast Neutron Irradiation (FNI) facility of The University of Massachusetts Lowell. The results show that all devices were fully functional and within production test limits after having been irradiated up to 1×10^{13} n/cm^2 (1-MeV equivalent). A sample size of nine units was exposed to radiation testing per MIL-STD-883, Method 1017 for Neutron Irradiation, and an additional one device was used as a control unit and was not irradiated.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of this document is available online at https://www.astm.org.)

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JEP57 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.
JEDEC JEP155 - Recommended ESD Target Level for HBM Qualification.
JEDEC JEP157 - Recommended ESD-CDM Target Levels.
JEDEC JS-001 - Joint ANSI/ESDA/JEDEC standard for electrostatic discharge sensitivity test – Human Body Model (HBM).
JEDEC JS-002 - Joint ANSI/ESDA/JEDEC standard for electrostatic discharge sensitivity test – Charged Device Model (CDM).

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram shall be as specified on figure 3.

3.2.4 Operating mode selection. The functional operating mode selection shall be as specified on figure 4.

3.2.5 Truth table. The truth table for each functional operating mode shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 5/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SUPPLY CURRENTS 3/							
Low-side quiescent current	I_{QLS}	MODE = PWM, EN = 0 V, VIN = 12 V, BOOT = 10 V	1, 2, 3	All		6.8	mA
		MODE = IIM, LI = HI = 0 V, VIN = 12 V, BOOT = 10 V				8	
High-side quiescent current	I_{QHS}	MODE = PWM, EN = 0 V, VIN = 12 V, BOOT = 10 V	1, 2, 3			6.3	mA
		MODE = IIM, LI = HI = 0 V, VIN = 12 V, BOOT = 10 V				6.3	
BOOT to AGND quiescent current (TPS7H6003-SP)	I_{QBG}	SW = 100 V, BOOT = 110 V		01	20 TYP 6/		μA
BOOT to AGND quiescent current (TPS7H6013-SP)		SW = 28 V, BOOT = 38 V		02	15 TYP 6/		
BOOT to AGND quiescent current (TPS7H6023-SP)		SW = 12 V, BOOT = 22 V		03	10 TYP 6/		
BOOT to AGND operating current (TPS7H6003-SP)	I_{OP_BG}	SW = 100 V, BOOT = 110 V		01	20 TYP 6/		μA
BOOT to AGND operating current (TPS7H6013-SP)		SW = 28 V, BOOT = 38 V		02	15 TYP 6/		
BOOT to AGND operating current (TPS7H6023-SP)		SW = 12 V, BOOT = 22 V		03	10 TYP 6/		
Low-side operating current	I_{OP_LS}	MODE = PWM, f = 500 kHz, no load for LOL and LOH	1, 2, 3	All		9	mA
		MODE = PWM, f = 1 MHz, no load for LOL and LOH				11	
		MODE = PWM, f = 2 MHz, no load for LOL and LOH				16	
		MODE = PWM, f = 5 MHz, no load for LOL and LOH				30	
		MODE = IIM, f = 500 kHz, no load for LOL and LOH				9	
		MODE = IIM, f = 1 MHz, no load for LOL and LOH				12	
		MODE = IIM, f = 2 MHz, no load for LOL and LOH				17	
		MODE = IIM, f = 5 MHz, no load for LOL and LOH				30	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 5/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SUPPLY CURRENTS – Continued 3/							
High-side operating current	I_{OP_HS}	MODE = PWM, f = 500 kHz, no load for HOL and HOH	1, 2, 3	All		6.5	mA
		MODE = PWM, f = 1 MHz, no load for HOL and HOH				8	
		MODE = PWM, f = 2 MHz, no load for HOL and HOH				10.5	
		MODE = PWM, f = 5 MHz, no load for HOL and HOH				17.5	
		MODE = IIM, f = 500 kHz, no load for HOL and HOH				6.5	
		MODE = IIM, f = 1 MHz, no load for HOL and HOH				8	
		MODE = IIM, f = 2 MHz, no load for HOL and HOH				10.5	
		MODE = IIM, f = 5 MHz, no load for HOL and HOH				15	
GATE DRIVER							
Low-level output voltage	V_{OL}	I_{OL} = 100 mA	1, 2, 3	All		0.15	V
High-level output voltage	BP5x - V_{OH}	I_{OH} = 100 mA				0.3	V
Peak source current	I_{OH}	HOH, LOH = 0 V (BP5x = 5 V)			0.7	2.3	A
Peak sink current	I_{OL}	HOL, LOL = 5 V (BP5x = 5 V)			1.6	4.6	A
INTERNAL REGULATORS							
Low-side 5 V regulator output voltage	V_{BP5L}	C_{BP5L} = 1 µF	1, 2, 3	All	4.75	5.175	V
Required BP5L output capacitor 4/					1		µF
High-side 5 V regulator output voltage	V_{BP5H}	C_{BP5H} = 1 µF			4.75	5.175	V
Required BP5H output capacitor 4/					1		µF
7 V regulator output voltage	V_{BP7L}				6.65	7.35	V
Required BP7L output capacitor 4/					1		µF
UNDERVOLTAGE PROTECTION							
BP5H UVLO rising threshold	$BP5H_R$	C_{BP5H} = 1 µF	1, 2, 3	All	4.0	4.5	V
BP5H UVLO falling threshold	$BP5H_F$	C_{BP5H} = 1 µF			3.8	4.3	
BP5L UVLO rising threshold	$BP5L_R$	C_{BP5L} = 1 µF			4.0	4.5	
BP5L UVLO falling threshold	$BP5L_F$	C_{BP5L} = 1 µF			3.8	4.3	
BP7L UVLO rising threshold	$BP7L_R$	C_{BP7L} = 1 µF			6.2	6.8	
BP7L UVLO falling threshold	$BP7L_F$	C_{BP7L} = 1 µF			5.9	6.5	
VIN UVLO rising threshold	VIN_R				8.0	9.0	
VIN UVLO falling threshold	VIN_F				7.5	8.5	
BOOT UVLO rising threshold	$BOOT_R$				6.6	7.4	
BOOT UVLO falling threshold	$BOOT_F$				6.2	7	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 5/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
INPUT PINS							
Input rising edge threshold	V_{IR}		1, 2, 3	All	1.80	2.65	V
Input falling edge threshold	V_{IF}				1.15	1.85	V
Input pull-down resistance	R_{PD}	V = 2.15 V applied at input (EN_HI or PWM_LI)			100	400	kΩ
PROGRAMMBLE DEAD TIME 3/							
LO off to HO on dead time		MODE = PWM, RLH = 3.32 kΩ, LO falling to HO rising (90% to 10%)	9, 10, 11	All	0	10	ns
		MODE = PWM, RLH = 11.8 kΩ, LO falling to HO rising (90% to 10%)			8	15.5	
		MODE = PWM, RLH = 21 kΩ, LO falling to HO rising (90% to 10%)			15.5	24	
		MODE = PWM, RLH = 52.3 kΩ, LO falling to HO rising (90% to 10%)			36	59	
		MODE = PWM, RLH = 105 kΩ, LO falling to HO rising (90% to 10%)			74	113.5	
HO off to LO on dead time		MODE = PWM, RHL = 7.87 kΩ, HO falling to LO rising (90% to 10%)			0	10	ns
		MODE = PWM, RHL = 13.3 kΩ, HO falling to LO rising (90% to 10%)			6	15	
		MODE = PWM, RHL = 23.7 kΩ, HO falling to LO rising (90% to 10%)			16	24.5	
		MODE = PWM, RHL = 57.6 kΩ, HO falling to LO rising (90% to 10%)			44	61	
		MODE = PWM, RHL = 113 kΩ, HO falling to LO rising (90% to 10%)			86	125	
BOOTSTRAP DIODE SWITCH							
Bootstrap Diode Switch Parallel Resistance			1, 2, 3	All	0.8	1.2	kΩ
POWER GOOD							
Logic-low output		I_{FLT} = 1 mA	1, 2, 3	All		0.4	V
PGOOD internal resistance		BP5L = 5 V, BP7L = 7 V, VIN = 12 V			0.7	1.9	MΩ
Minimum BP5L voltage for valid PGOOD output						2.45	V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 5/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SWITCHING CHARACTERISTICS 3/							
LO turnoff propagation delay	t_{LPHL}	MODE = PWM, PWM rising to LOL falling	9, 10, 11	All		48	ns
		MODE = IIM, LI falling to LOL falling				38	
LO turnon propagation delay	t_{LPLH}	MODE = IIM, LI rising to LOH rising				38	
HO turnoff propagation delay	t_{HPHL}	MODE = PWM, PWM falling to HOL falling				50	
		MODE = IIM, HI falling to HOL falling				40	
HO turnon propagation delay	t_{HPLH}	MODE = IIM, HI rising to HOH rising				40	
Delay matching LO on and HO off	t_{MON}	MODE = IIM				12	
Delay matching LO off and HO on	t_{MOFF}	MODE = IIM				4	
HO rise time	t_{HRC}	C_L = 1000 pF, 10% to 90%				7.5	
LO rise time	t_{LRC}	C_L = 1000 pF, 10% to 90%				7.5	
HO fall time	t_{HFC}	C_L = 1000 pF, 90% to 10%				5.5	
LO fall time	t_{LFC}	C_L = 1000 pF, 90% to 10%				5.5	
Minimum input pulse width (turn-on)	t_{PW_IIM}	MODE = IIM				8	
Minimum input pulse width (turn-off)	t_{PW_PWM}	MODE = IIM				12	

1/ Unless otherwise noted, VIN = 10 V to 14 V, V_{BP5L} = V_{BP5H} = 5 V, and no load on LOH, LOL, HOH and HOL.

2/ RHA devices supplied to this drawing are tested at the R level in accordance with MIL-STD-883, method 1019, condition A (see 1.5 herein).

3/ See figure 4 for MODE selection.

4/ Specified by design only. Not tested in production.

5/ Note: $T_A = T_J$

6/ Typical values are provided for information only.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_A)	Effective Linear energy transfer (LET)
All	No SEL	125 ºC	LET ≤ 75 [MeV/(mg/cm^2)]
	No SEB	25 ºC	LET ≤ 75 [MeV/(mg/cm^2)]
	No SEGR	25 ºC	LET ≤ 75 [MeV/(mg/cm^2)]

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Holmiun (^{165}Ho) ion beam was used at an angle of incidence of 0° at flux of 10^5 ions/cm^2·s, fluences level of 10^7 ions/cm^2 and a temperature of 125°C and no single event latch-up (SEL) was observed at LET of 75 MeV·cm^2/mg. Manufacturer also test Single event burnout (SEB) and Single event gate rupture (SEGR) test with Holmiun (^{165}Ho) ion beam at an angles of incidence of 0°. No SEB/SEGR observed up to LET of 75 MeV·cm^2/mg. For more information on SEE/SEP test please contact device manufacturer.

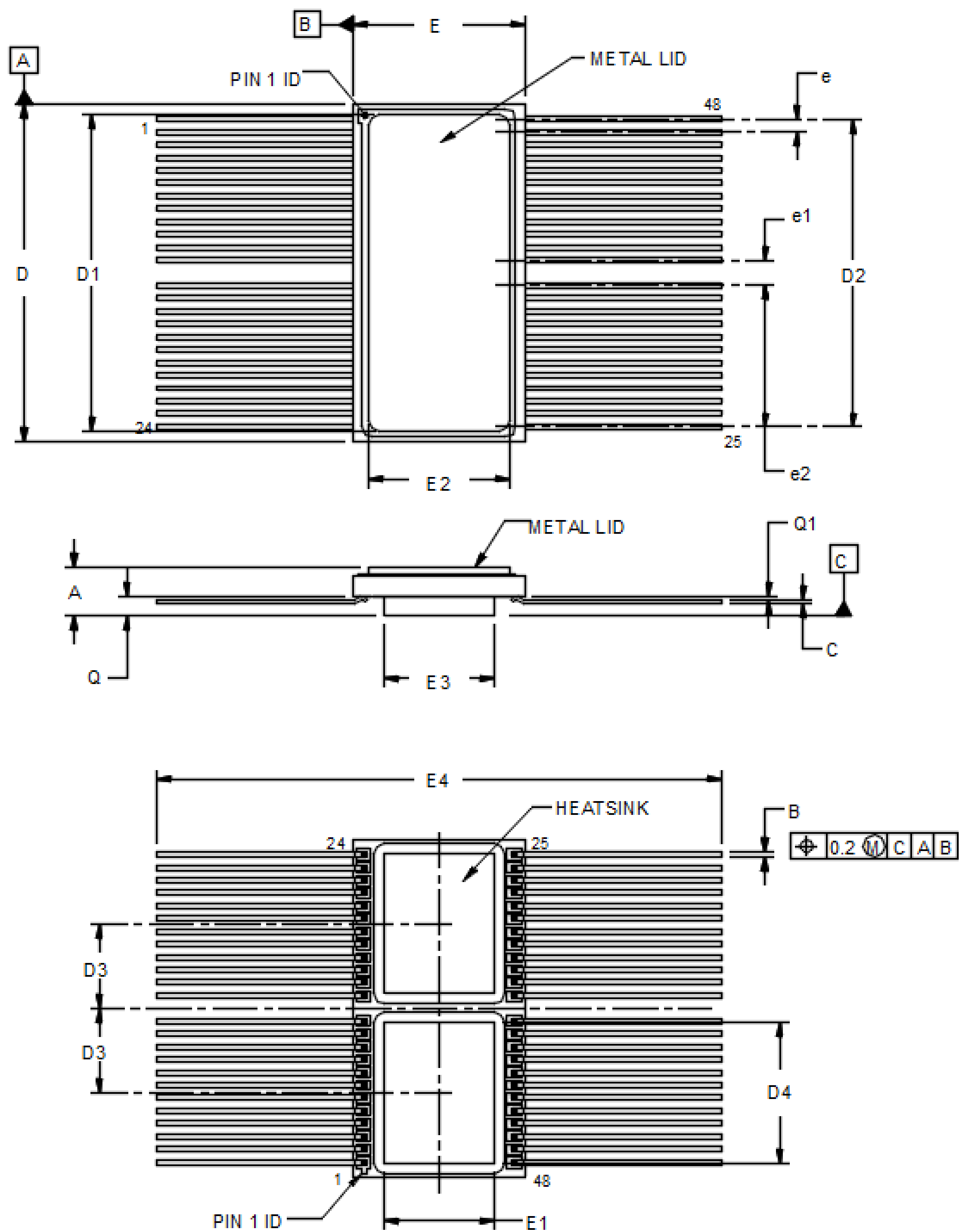


FIGURE 1. Case outline.

Symbol	Millimeter		Symbol	Millimeter	
	Min	Max		Min	Max
A	2.181	2.667	E1	5.24	5.64
B	0.204	0.304	E2	7.01 REF	
c	0.1	0.2	E3	5.44 REF	
D	16.49	16.99	E4	27.5	28.5
D1	15.7 REF		Q	0.84	1.04
D2	15.24 TYP		Q1	0.2 REF	
D3	4.195 TYP		e	0.635 TYP	
D4	6.74	7.14	e1	1.27 TYP	
E	8.28	8.68	e2	6.985 TYP	

NOTES:

1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.

FIGURE 1. Case outline - Continued.

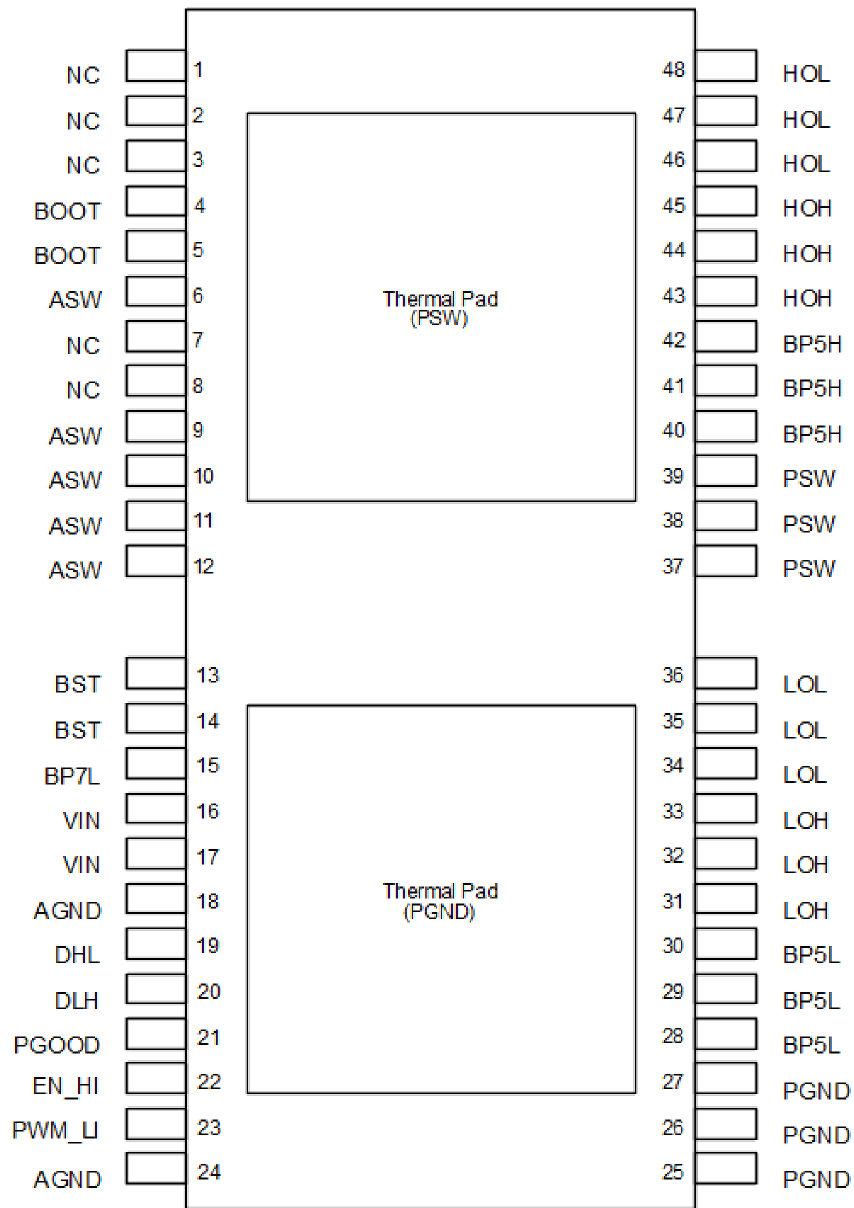


FIGURE 2. Terminal connections.

PIN		I/O	DESCRIPTION
Number	Name	1/	
4-5	BOOT	I	Input voltage supply of the high-side linear regulator. The external bootstrap capacitor is placed between BOOT and ASW. The cathode of the external bootstrap diode is connected to this pin. A Zener diode clamp may be needed between BOOT and ASW in order to not exceed the absolute maximum electrical rating.
6, 9-12	ASW	—	High-side driver signal return. ASW(6) is internally connected to PSW and the high-side thermal pad. Connect ASW(9-12) to ASW externally.
13-14	BST	O	For bootstrap charging that utilizes the internal bootstrap switch, this pin serves as the bootstrap diode anode connection point. The external high-side bootstrap capacitor can be charged through this pin using the input voltage applied to VIN, internal bootstrap switch, and external bootstrap diode(s).
15	BP7L	O	Low-side 7-V linear regulator output. A minimum of 1-uF capacitance is required from BP7L to AGND.
16-17	VIN	I	Gate driver input voltage supply. Input voltage range is from 10 V to 14 V. This pin serves as the input to the low-side linear regulators and the internal bootstrap switch. For bootstrap charging directly from the input voltage, VIN also serves as the bootstrap diode anode connection point.
18, 24	AGND	—	Low-side driver signal return. AGND(24) is internally connected to PGND and the low-side thermal pad. Connect AGND(18) to AGND externally.
19	DHL	I	High-side to low-side dead time set. In PWM mode, a resistor from DHL to AGND sets the dead time between the high-side turn-off and low-side turn-on. In independent input mode (IIM), DHL is used to configure the input interlock protection of the driver. DHL is connected to 5 V in IIM with interlock enabled. A resistor valued between 100 kΩ and 220 kΩ is connected from DHL to AGND for IIM with interlock disabled.
20	DLH	I	Low-side to high-side dead time set. In PWM mode, a resistor from DLH to AGND sets the dead time between the low-side turn-off and high-side turn-on. In independent input mode (IIM), DLH is used to configure the input interlock protection of the driver. A resistor valued between 100 kΩ and 220 kΩ is connected from DLH to AGND for IIM with interlock enabled. DLH is connected to 5 V in IIM with interlock disabled.
21	PGOOD	O	Power good pin. Asserts low when any of the low-side internal linear regulators or VIN goes into undervoltage lockout. Requires a 10-kΩ pull-up resistor to BP5L.
22	EN_HI	I	Enable input or high-side driver control input. In PWM mode this is used as an enable pin. In independent input mode (IIM) this serves as the control input for the high-side driver.

See footnotes at end of table.

FIGURE 2. Terminal connections - Continued.

PIN		I/O	DESCRIPTION
Number	Name	1/	
23	PWM_LI	I	PWM input or low-side driver control input. In PWM mode this is used as the PWM input to the gate driver. In independent input mode (IIM) this serves as the control input for the low-side driver.
25-27	PGND	—	Low-side power ground. Connected to the source of the low-side GaN FET. Should be connected to AGND.
28-30	BP5L	O	Low-side 5-V linear regulator output. A minimum of 1-μF capacitance is required from BP5L to PGND.
31-33	LOH	O	Low-side driver source current ouput. Connect to the gate of low-side GaN FET with short, low inductance path. A resistor between LOH and the gate of the GaN FET can be used to adjust the turn-on speed.
34-36	LOL	O	Low-side driver sink current output. Connect to the gate of the low-side GaN FET with short, low inductance path. A resistor between LOL and the gate of the GaN FET can be used to adjust the turn-off speed.
37-39	PSW	—	Switch node connection. Connected to the source of the high-side GaN FET. Should be connected to ASW.
40-42	BP5H	O	High-side 5-V linear regulator output. A minimum of 1-μF capacitance is required from BP5H to PSW.
43-45	HOH	O	High-side driver source current output. Connect to the gate of the high-side GaN FET with short, low inductance path. A resistor between HOH and the gate of the GaN FET can be used to adjust the turn-on speed.
46-48	HOL	O	High-side driver sink current output. Connect to the gate of the high-side GaN FET with short, low inductance path. A resistor between HOL and the gate of the GaN FET can be used to adjust the turn-off speed.
1-3, 7-8	NC	—	No connect. These pins can be left unconnected or connected to the high-side reference voltage (ASW).
--	PSW PAD	—	High-side thermal pad. Intentionally connected to ASW (6) and PSW. Should be connected to ASW pins.
--	PGND PAD	—	Low-side thermal pad. Intentionally connected to AGND (18) and PGND. Should be connected to AGND pins.

1/ I = Input, O = Output, I/O = Input or Output, — = Other

FIGURE 2. Terminal connections - Continued.

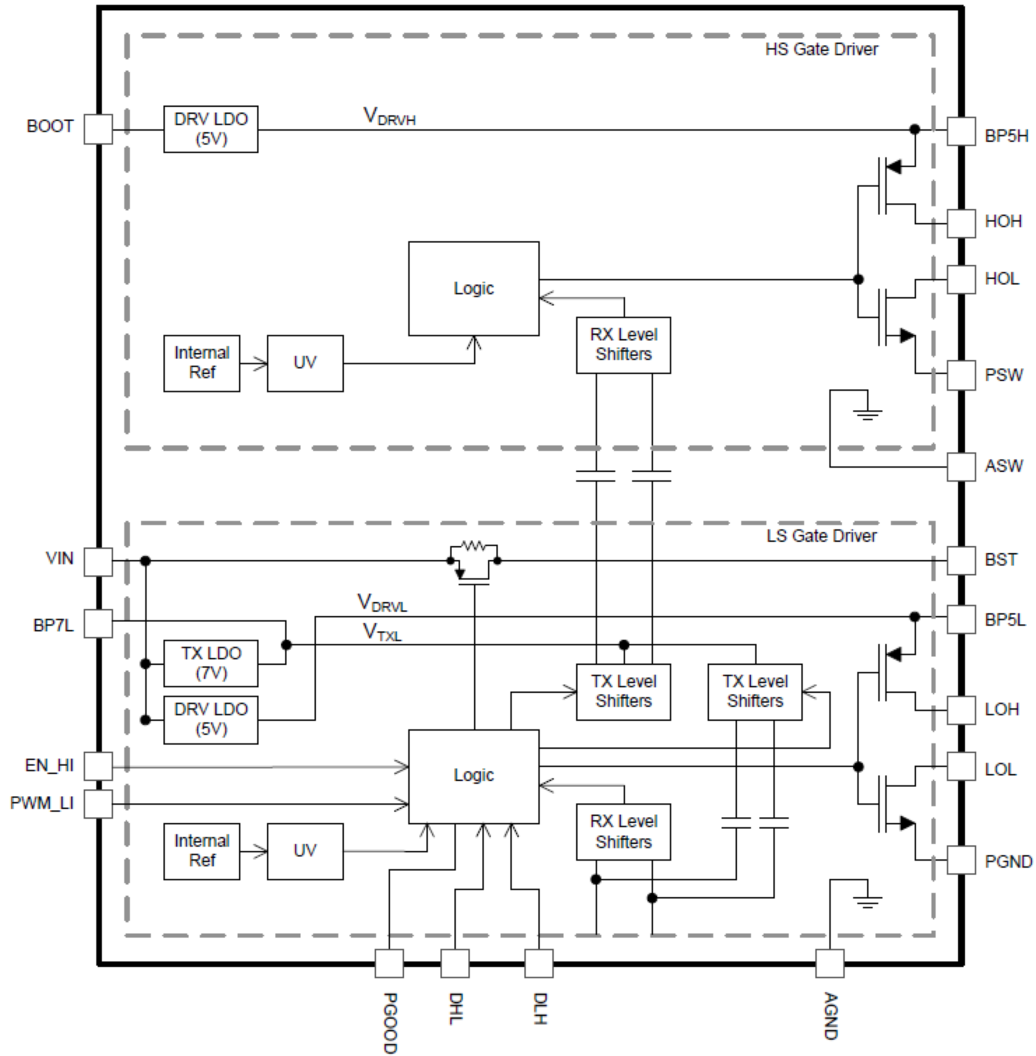


FIGURE 3. Block diagram.

Operating Mode 1/	DLH	DHL
PWM	Resistor to AGND 2/	Resistor to AGND 2/
Independent input mode (IIM) – input interlock disabled	BP5L	Resistor to AGND (100 kΩ to 220 kΩ) 3/
Independent input mode (IIM) – input interlock enabled	Resistor to AGND (100 kΩ to 220 kΩ) 3/	BP5L

1/ Pins DHL and DLH determine the mode of operation. There are two different operational modes: PWM and independent input mode (IIM). In PWM mode, the EN_HI pin is used to enable the device, a single PWM input signal is required on PWM_LI, and the device generates the complementary output signals on LO and HO. In IIM, separate PWM input signals are required on PWM_LI and EN_HI. The corresponding outputs of the device are driven directly from these inputs. In IIM, there is an optional interlock protection that can be enabled for the gate driver.

2/ Resistors are connected from DHL to AGND and DLH and AGND to program the dead time between the high-side and low-side outputs. See table IA for programmable dead time program characteristics.

3/ In IIM, resistors used must be valued between 100 kΩ and 220 kΩ

FIGURE 4. Operating mode selection.

Inputs		PWM mode		IIM – Interlock Disabled		IIM – Interlock Enabled	
EN_HI	PWM_LI	HO	LO	HO	LO	HO	LO
0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1
1	0	0	1	1	0	1	0
1	1	1	0	1	1	0	0

FIGURE 5. Truth table.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 1/ 6, 9, 10, 11	1, 2, 3, 4, 5, 1/ 2/ 6, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 2/ 6, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4
Group E end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA). Delta's are performed at room temperature.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Device Type	Delta limits	Units
Low-side quiescent current (MODE = IIM)	IQLS	All	±550	uA
High-side quiescent current (MODE = IIM)	IQHS		±550	uA
High-side operating current (MODE = PWM, f = 500 kHz)	IOP_HS		±450	uA
Low-side operating current (MODE = PWM, f = 500 kHz)	IOP_LS		±550	uA
Low-side operating current (MODE = IIM, f = 500 kHz)	IOP_LS		±550	uA

1/ Delta's are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C ±10% for SEB and SEGR. The test temperature shall be +125°C ±10% for SEL.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see Table IB herein.

4.4.4.3 Neutron /Displacement damaged dosimetry testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at TA = +25°C ±5°C after an exposure of 1 x 10^{13} neutrons/cm^2 (minimum).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latchup (SEL).

c. Occurrence of burnouts (SEB).

d. Occurrence of gate rupture (SEGR).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-03-06

Approved sources of supply for SMD 5962-22201 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R2220101VXC	01295	TPS7H6003-SP
5962R2220102VXC	01295	TPS7H6013-SP
5962R2220103VXC	01295	TPS7H6023-SP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.