REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS			REV																	
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
22-01-13

REVISION LEVEL

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, FLIP CHIP, CLASS Y, SiGe BiCMOS 130nm, QUAD 12-bit 1.6 GSps, ANALOG TO DIGITAL CONVERTER (ADC) WITH EMBEDDED CROSS-POINT SWITCH AND EASYSTREAM SERIAL DATA OUTPUT, MONOLITHIC

SIZE	CAGE CODE	
A	**67268**	**5962-21214**

DSCC FORM 2233
APR 97

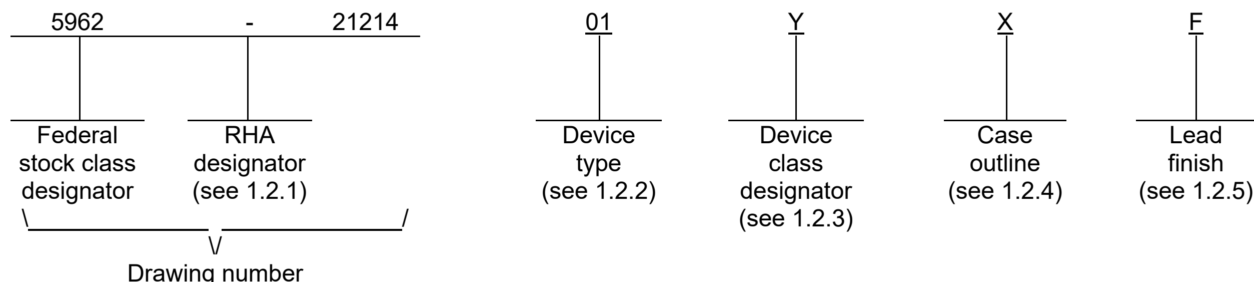
5962-E564-21

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability space application device class Y ceramic non-hermetic flip chip device. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Y RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	EV12AQ600	Quad 12-bit 1.6 GSps ADC

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Y	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	323	Ceramic Ball Grid Array (CBGA) 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device class Y.

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1. Terminal lead finish F is tin lead alloy. Package case outline X contained: Sn = 10% and Pb = 90%.

1.3 Absolute maximum ratings. 1/

Analog supply voltage 3.3 V (V_{CCA}) .... AGND -0.3 V to 4.0 V
Output supply voltage 2.5 V (V_{CCO}) .... GNDO -0.3 V to 3.1 V
Digital supply voltage 1.2 V (V_{CCD}) .... DGND -0.3 V to 1.5 V
SPI output supply voltage 2.5 or 3.3 V (V_{CC-SPI}) .... DGND -0.3 V to 4.0V
V_{SPI_SEL} supply voltage 2.5 or 3.3 V ($V_{SPI-SEL}$) .... DGND -0.3 V to 4.0V
Maximum Analog input swing (mode ON) | INxP – InxN | (x=0,1,2 or 3) .... 4.8 Vppdiff
Maximum Analog input swing (mode OFF) | INxP – InxN | (x=0,1,2 or 3) 2/ .... Vppdiff
Analog input peak voltage INxP or InxN (x=0,1,2 or 3) .... AGND -0.3 V to V_{CCA} + 0.3 V
Maximum Clock input swing (mode ON) |V_{CLKP} – V_{CLKN}| .... 4.0 Vppdiff
Maximum Clock input swing (mode OFF) |V_{CLKP} – V_{CLKN}| 2/ .... Vppdiff
Clock input voltage (V_{CLKP} or V_{CLK}) .... AGND -0.3 V to V_{CCA} + 0.3 V
Maximum SYNC input swing (mode ON) |V_{SYNCP} – V_{SYNCN}| .... 4.0 Vppdiff
Maximum SYNC input swing (mode OFF) |V_{SYNCP} – V_{SYNCN}| 2/ .... Vppdiff
SYNC input peak voltage (V_{SYNCP} or V_{SYNCN}) .... AGND -0.3 V to V_{CCA} + 0.3 V
SPI input voltage (CSN, SCLK, RSTN, MOSI) .... DGND -0.3 V to V_{CCO} + 0.3 V
Maximum junction temperature (T_{JMAX}) .... +150°C
Storage temperature (T_{STG}) .... -65°C to +150°C
VDIODEA input voltage to prevent leakage (VDIODEC=GND) ($VDIODE_A$) .... -0.3 V to 0.30 V
Maximum input current on DIODE ($IDIODE_A$) .... 1 mA
ESD protection
Human body model (HBM) 6/ .... 2000 V
Charged device model (CDM) .... 250 V

1.4 Recommended operating conditions.

Analog supply voltage (V_{CCA}) .... 3.3 V
Output supply voltage (V_{CCO}) .... 2.5 V
Digital supply voltage (V_{CCD}) 3/ .... 1.2 V
SPI output supply voltage (V_{CC-SPI}) .... 2.5 V or 3.3 V 3/
Maximum differential input voltage (Full Scale) (VIN – VINN):
.... 1 Vpp 4/
.... 1 dBm
Clock input power level (P_{CLK} P_{CLKN}) .... 6 dBm
Digital CMOS input (VD):
V_{IL} .... 0 V
V_{IH} 5/ .... 2.5 or 3.3 V
External Clock frequency (Fc) .... ≤6.4 GHz
Operating Temperature Range (T_C; T_J) .... -55°C to +125°C
Die operating life at T_J = +125°C (HTOL) 6/ 7/ .... 10 Years
Die operating life at T_J = +110°C (HTOL) 6/ 7/ .... 17 Years
Latch up (JEDEC 78A) (LU) 6/ .... ± 100 mA

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ For cold sparing application, see application manufacturer data note AN 60S 217359. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure. Input buffers and associated ESD protection have been designed to allow “cold sparing”.
3/ Depending on SPI output buffer logic compatibility (refer to manufacturer data §7.1)
4/ Above this value the ADC will saturate. It is recommended to provide a signal below -1 dBFS to avoid this saturation.
5/ Buffer compatible with both logic levels (refer to manufacturer data §7.1).
6/ This circuit is designed and manufactured and will be qualified to be compliant with space requirement (ESCC9000 and QML-Y specifications).
7/ T_J refers to the hot spot junction temperature on the die.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation

J-STD-020 - Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices

JEP163 - Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JESD22-B117 - Solder ball shear test method

JESD471 - Symbol and Label for Electrostatic Sensitivity Devices.

JESD625 - Requirements for Handling Electrostatic Discharge Sensitive (ESDs) Devices

(Copies of these documents are available online at http://www.jedec.org.)

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class Y shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device class Y.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2a and 2b.

3.2.3 Functional description. The functional description shall be as specified on figure 3.

3.2.4 Pinout Function. The pinout function shall be as specified on figure 4.

3.2.5 Block diagram. The block shall be as specified on figure 5.

3.2.6 Serial link eye diagram. The serial link eye diagram shall be as specified on figure 6.

3.2.7 Differential Internal blocks. The differential Internal blocks shall be as specified on figure 7.

3.2.8 Trigger mode timing diagram in serial interface. The trigger mode timing diagram in serial interface shall be as specified on figure 8.

3.2.9 Timing diagram in serial interface in 1-channel mode. The timing diagram in serial interface in 1-channel mode shall be as specified on figure 9.

3.2.10 Timing diagram in serial interface in 2-channel mode. The timing diagram in serial interface in 2-channel mode shall be as specified on figure 10.

3.2.11 Thermal characteristics. The thermal characteristics shall be as specified on figure 11.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.4.1 Solderability test for BGA/CGA packages: Solderability test for case outline X for CGA/BGA package has been verified during solder column or ball attachment process in accordance with method 2003 of MIL-STD-883.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For class Y packages where marking of the entire SMD PIN number is required (see herein 1.2). For RHA product, the RHA designator shall still be marked. Marking for device class Y shall be used ink or laser mark in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device class Y shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.5.1.1 Electrostatic discharge (ESD) sensitivity mark. ESD marking on devices and, on container/carriers are required as specified in MIL-PRF-38535. All of the markings shall appear on the carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. An industry standard symbol for identifying ESD sensitive items (e.g., JESD471 symbol) shall be marked on the carrier or container.

3.5.1.1.1 Moisture sensitivity level (MSL) mark. Non-hermetic devices such as class Y can exhibit sensitivity to moisture-induced stress and must be handled, packaged, and stored in a proper manner to avoid potential damage during assembly solder reflow attachment and/or repair operations. Moisture sensitivity levels are defined as a rating identifying a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. The manufacturer shall be required to define the moisture sensitivity level (MSL) for each non-hermetic device in accordance with J-STD-020.

3.5.2 Lot date code. Flip chip devices lot date code shall be assigned after underfill cured to identify the device with the assembly processing and assembly location. Devices will be traceable through the lot date code to the assembly year, underfill sealing week and assembly location.

3.6 Certificate of compliance. For device class Y, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets for device class Y and the requirements of MIL-PRF-38535.

3.7 Certificate of conformance. A certificate of conformance as required for device class Y in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T_C, T_j ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
POWER REQUIREMENTS **Power Supply Current** 2/							
Analog	I_{CCA}		1, 2, 3	01	1400	2035	mA
Output Reduced swing	I_{CCO}		1, 2, 3	01	300	410	
Digital	I_{CCD}		1, 2, 3	01	150	300	
SPI output	I_{CC_SPI}		1, 2, 3	01	-2.5	2.5	
Power Supply Current Standby mode							
Analog	I_{CCA}		1, 2, 3	01	410	750	mA
Output	I_{CCO}		1, 2, 3	01	10	30	
Digital	I_{CCD}		1, 2, 3	01	10	60	
SPI output	I_{CC_SPI}		1, 2, 3	01	-2.5	2.5	
Power dissipation – Full power mode 2/							
Reduced swing	PD		1, 2, 3	01	5.5	7.95	W
Stand-by mode			1, 2, 3	01	1.4	2.7	
ANALOG INPUTS							
Common mode compatibility for analog inputs	AC or DC	3/					
Input Common Mode (default register value)	VICM		1, 2, 3	01	1.48	1.78	V
Input leakage current for VINN = VINP = Common Mode + 75mV	IIN		1	01	40	220	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C, T_j ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLOCK INPUTS (CLKIN) Low phase noise Differential Sinewave							
Clock input common mode voltage	V_{CM}		1, 2, 3	01	2.4	2.8	V
Clock input resistance (differential)	R_{CLK}	4/	1, 2, 3	01	90	116	Ω
CLOCK OUTPUT (CLKOUT) Logic Compatibility CML 5/							
Output levels : swing adjust off = full swing							
Logic low	V_{OL}		1, 2, 3	01		V_{CCA} - 0.26	V
Logic high	V_{OH}		1, 2, 3	01	V_{CCA} - 0.20		V
Differential output	V_{OH}-V_{OL}		1, 2, 3	01	140	220	mVp
Common mode	V_{OCM}		1, 2, 3	01	V_{CCA} - 0.29	V_{CCA} - 0.19	V
Output levels : swing adjust on = reduced swing							
Logic low	V_{OL}		1, 2, 3	01		V_{CCA} - 0.12	V
Logic high	V_{OH}		1, 2, 3	01	V_{CCA} - 0.15		V
Differential output	V_{OH}-V_{OL}		1, 2, 3	01	70	110	mVp
Common mode	V_{OCM}		1, 2, 3	01	V_{CCA} - 0.2	V_{CCA} - 0.1	V
SYNC, SYNCN Signal							
Input Voltages to be applied Swing	V_{IH}- V_{IL}		1, 2, 3	01	80	600	mV
Common Mode	V_{ICM}		1, 2, 3	01	1.0	1.6	V
SYNCTRIGP, SYNCTRIGN input resistance	R_{SYNC}		1, 2, 3	01	98	134	Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C, T_j ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital CMOS signals (CSN, SCLK, RSTN, MOSI, MISO) 6/							
Low level threshold of Schmitt Trigger	V_{IL}		1, 2, 3	01		0.7	V
High level threshold of Schmitt Trigger	V_{IH}		1, 2, 3	01	1.7		
CMOS low level output voltage (Iolc = 3 mA)	V_{OLC}		1, 2, 3	01		0.20 * V_{CC_SPI}	
CMOS high level output voltage (Iohc = 3 mA)	V_{OHC}		1, 2, 3	01	0.8 * V_{CC_SPI}		
LVDS OUTPUTS (SSO, SYNCO) -- Logic Compatibility LVDS 5/ 7/							
Output levels : swing adjust off = full swing							
Logic low	V_{OL}		1, 2, 3	01		1.460	V
Logic high	V_{OH}		1, 2, 3	01	1.16		V
Differential output	V_{OH}-V_{OL}		1, 2, 3	01	200	375	mV
Common mode	V_{OCM}		1, 2, 3	01	1.05	1.5	V
Output levels : swing adjust on = reduced swing							
Differential output	V_{OH}-V_{OL}		1, 2, 3	01	80	275	mV
Common mode	V_{OCM}		1, 2, 3	01	1.1	1.55	V
SERIAL LINK OUTPUTS (ASLx,BSLx,CSLx,DSLx) with x=0 or 1 -- Logic Compatibility CML 5/							
Output levels : swing adjust off = full swing							
Logic low	V_{OL}		8/	01		V_{CCO} – 0.55	V
Logic high	V_{OH}		8/	01	V_{CCO} – 0.42		V
Differential output	V_{OH}-V_{OL}		8/	01	260	400	mVp
Common mode	V_{OCM}		8/	01	V_{CCO} – 0.6	V_{CCO} – 0.4	V
Output levels : swing adjust on = reduced swing							
Logic low	V_{OL}		8/	01		V_{CCO} – 0.35	V
Logic high	V_{OH}		8/	01	V_{CCO} – 0.32		V
Differential output	V_{OH}-V_{OL}		8/	01	170	280	mVp
Common mode	V_{OCM}		8/	01	V_{CCO} – 0.45	V_{CCO} – 0.25	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C, T_j ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low frequency characteristics **DC ACCURACY**							
Analog Input frequency = 100 MHz, -1 dBFS, 1-Channel mode							
DNLrms	DNL_{rms}		7, 8A, 8B	01		0.28	LSB
Differential non linearity	DNL		7, 8A, 8B	01	-0.85	1.2	LSB
INLrms	INL_{rms}		7, 8A, 8B	01		1.4	LSB
Integral non linearity	INL		7, 8A, 8B	01	-4.5	4.5	LSB
Dynamic Performance - 4-channel mode – 1.6 GSps at -1 dBFS output level **SFDR - Spurious Free Dynamic Range**							
Fin = 2230 MHz	SFDR		4, 5, 6	01	55		dBFS 9/ 10/ 11/ 12/
THD - Total harmonic distortion							
Fin = 2230 MHz	THD		4, 5, 6	01		-52	dBFS 9/
SNR - Signal to noise ratio							
Fin = 2230 MHz	SNR		4, 5, 6	01	49		dBFs 9/
SINAD - Signal to noise and distortion ratio							
Fin = 2230 MHz	SINAD		4, 5, 6	01	48		dBFs 9/
ENOB - Effective Number Of Bits							
Fin = 2230 MHz	ENOB		4, 5, 6	01	7.7		Bit_FS 9/

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C, T_j ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic Performance - 1-channel mode – 6.4 GSps at -1dBFS output level **SFDR - Spurious Free Dynamic Range**							
Fin = 2230 MHz	SFDR		4, 5, 6	01	53		dBFS 9/ 10/ 11/ 12/ 13/ 14/
THD - Total harmonic distortion							
Fin = 2230 MHz	THD		4, 5, 6	01		-54	dBFS 9/ 13/
TILD - Total InterLeaving Distortion							
Fin = 2230 MHz	TILD		4, 5, 6	01		-51	dBFS 9/ 13/ 14/
SNR - Signal to noise ratio							
Fin = 2230 MHz	SNR		4, 5, 6	01	49		dBFS 9/ 13/ 14/
SINAD - Signal to noise and distortion ratio							
Fin = 2230 MHz	SINAD		4, 5, 6	01	48		dBFs 9/ 13/ 14/
ENOB - Effective Number Of Bits							
Fin = 2230 MHz	ENOB		4, 5, 6	01	7.7		Bit_FS 9/ 13/ 14/

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C, T_j \leq +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Transient, Switching and Timing Characteristics							
Transient characteristics							
Conversion Error Rate at 1.6 GSps Less than 128 LSB (TBC)	CER	15/	8/	01	$10E^{-15}$ (typ)		Error/ sample
Overvoltage Recovery Time	ORT		8/	01	625 (typ)		ps
Switching characteristics - SWITCHING PERFORMANCE AND CHARACTERISTICS (Any Output Mode)							
External Clock low frequency range	F_{CLK}		8/	01	800	2000	MHz
External Clock high frequency range			8/	01	4500	6400	
Sampling Clock low frequency range per core	Fs		8/	01	200	500	MSps
Sampling Clock high frequency range per core			8/	01	1125	1600	
Max crosstalk from CLKOUT on clock input signal	XTALK_ CKO2CK	@ 12.8 Gbps	8/	01		-60	dB
ADC Aperture uncertainty (SDA disabled)	$JITTER_{SDA_OFF}$ 16/		8/	01	125 (typ)		fs_{RMS}
ADC Aperture uncertainty (SDA enabled min)	$JITTER_{SDA_MIN}$		8/	01	220 (typ)		fs_{RMS}
ADC Aperture uncertainty (SDA enabled max)	$JITTER_{SDA_MAX}$		8/	01	270 (typ)		fs_{RMS}
CLKOUT jitter			8/	01	70 (typ)		fs_{RMS}
Minimum SYNC pulse width	TSYNC		8/	01	2 (typ)		External Clock cycles
Switching characteristics - SWITCHING PERFORMANCE AND CHARACTERISTIC (SSO, SYNCO)							
CLK to SYNCO pipeline delay sync_edge rising	TPD_{SYNCO}		8/	01	1 (typ)		External Clock cycles
CLK to SYNCO pipeline delay sync_edge falling	TPD_{SYNCO}		8/	01	0.5 (typ)		External Clock cycles
CLK to SYNCO delay	TD_{SYNCO}		8/	01	350 (typ)		ps
CLK to SSO delay	TD_{SSO}		8/	01	1.2 (typ)		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions -55°C ≤ T_C, T_j ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switching characteristics - SWITCHING PERFORMANCE AND CHARACTERISTIC (Serial output)							
Output rise time for DATA (20%-80%)	TR	17/	8/	01	31 (typ)		ps
Output fall time for DATA (20%-80%)	TF	17/	8/	01	31 (typ)		ps
Total jitter (BER=10^{-15})	2XT1	@ 12.8 Gbps 17/ 19/	8/	01	25 (typ)		ps
First time to get YT2 amplitude voltage	XT2	@ 12.8 Gbps 17/ 19/	8/	01	25 (typ)		ps
Maximum amplitude voltage		@ 12.8 Gbps 17/ 19/	8/	01	400 (typ)		mV
Skew between serial output signal P and N	Tskew	17/	8/	01		3.5	ps
Conversion Core latency		18/	8/	01	5 (typ)		External Clock cycles
Total conversion latency		18/	8/	01	126	142	External Clock cycles
Crosstalk between xSL1 and xSL0@ 12.8 Gbps (x= A, B, C or D)	XTALK_SL2SL	17/	8/	01	-60 (typ)		dB
Max crosstalk between output serial link and analog input signal	XTALK_SL2IN	@ 12.8 Gbps 17/	8/	01	-60 (typ)		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1. Typical values are given for typical supplies V_{CCA} = 3.3 V, V_{CCD} = 1.2 V, V_{CCO} = 2.5 V at room temperature with Fclk = 6GHz and with nominal mode of the SPI (SDA, CLKOUT and SYNCO disabled). Minimum and Maximum values are given over temperature and power supplies. Unless otherwise specified
2. Enabling either SDA or other features (CLKOUT, SSO, SYNCO) increases power consumption by 170 mW (51 mA on V_{CCA}). Maximum power consumption is estimated at Tj = 125 °C, maximum supplies value and all features enabled.
3. The DC analog common mode voltage is provided by the ADC.
4. For optimal performance in term of VSWR, characteristic impedance of input traces on the PCB must be differential 100 Ω ± 5% and analog input impedance must be digitally trimmed to cope with process deviation (refer to manufacturer data §8.5.6).
5. 50 Ω transmission lines,100 Ω (2 x50 Ω differential termination)
6. Vil & Vih being referenced to Vcco (see simplified electrical schematics Table 14) the following equations apply: Vih_min = 0.65*Vcco_max & Vil_max = 0.3* Vcco_min
7. V_{OCM} is 1.425 V max with V_{CCA} = 3.3 V max.
8. Values listed for electrical parameters are tested in functional mode and may not be independently tested in production. This parameter is for informational purpose only.
9. Optimal bandwidth selection depends on signal characteristic. The bandwidth selection allows optimizing noise and linearity trade-off. For signals below 1.6 GHz, the bandwidth selection must be set to Nominal. For signals beyond this frequency, the bandwidth must be set to Extended. The extended bandwidth degrades noise floor up to 1 dB, compensated at high frequency by inputing signals with lower signal attenuation.
10. Linearity of high frequencies is dominated by H3 and H2, stepping back 3 or 6 dB on input signals involving signifiant improvement on SFDR figures. For narrow band operation (10 MHz or 50 MHz), a carefuly chosen frequency plan allows rejection of these folded harmonics up to H8 beyond the band of interest.
11. SFDR without H3 harmonic is better than 60 dBFS at -1 dBFS. Removing H2 and H3 allows an SFDR performance higher than 68 dBFS up to 5580 MHz. H3 dominates up to 5300 MHz, then H2 dominates above 5300 MHz.
12. Adjustment of input common mode can also be used to optimize ADC linearity.
13. For input frequencies < 800 MHz, the SFDR is given with the interleaving calibration set CALSET2. For input frequencies > 800 MHz, the SFDR is given with CALSET0.
14. Interleaving performance (1-channel and 2-channel mode) are given for IN0 only. For IN3, interleaving calibration must be done to achieve those performance.
15. Measured with 95% confidence level and a threshold of 100 LSB (< 2.5% full scale) . Fs = 1.6 GSps, T_J = 110ºC. For T_J = 125°C, CER value is $10E^{-12}$
16. See Definition of Terms (refer in manufacturer data §3.14)
17. 100 Ω load + PCB line 7 cm + cable 60 cm.
18. The latency of the conversion core is fixed. The total latency of the ADC (including the serial interface) can take any system external clock cycle between 126 and 142. ESIstream protocol wipes out the variable latency on the receiver’s end due to its intrinsic synchronization procedure.
19. See figure 6 for illustration of this value on the eye diagram on the serial links.

Case outline X

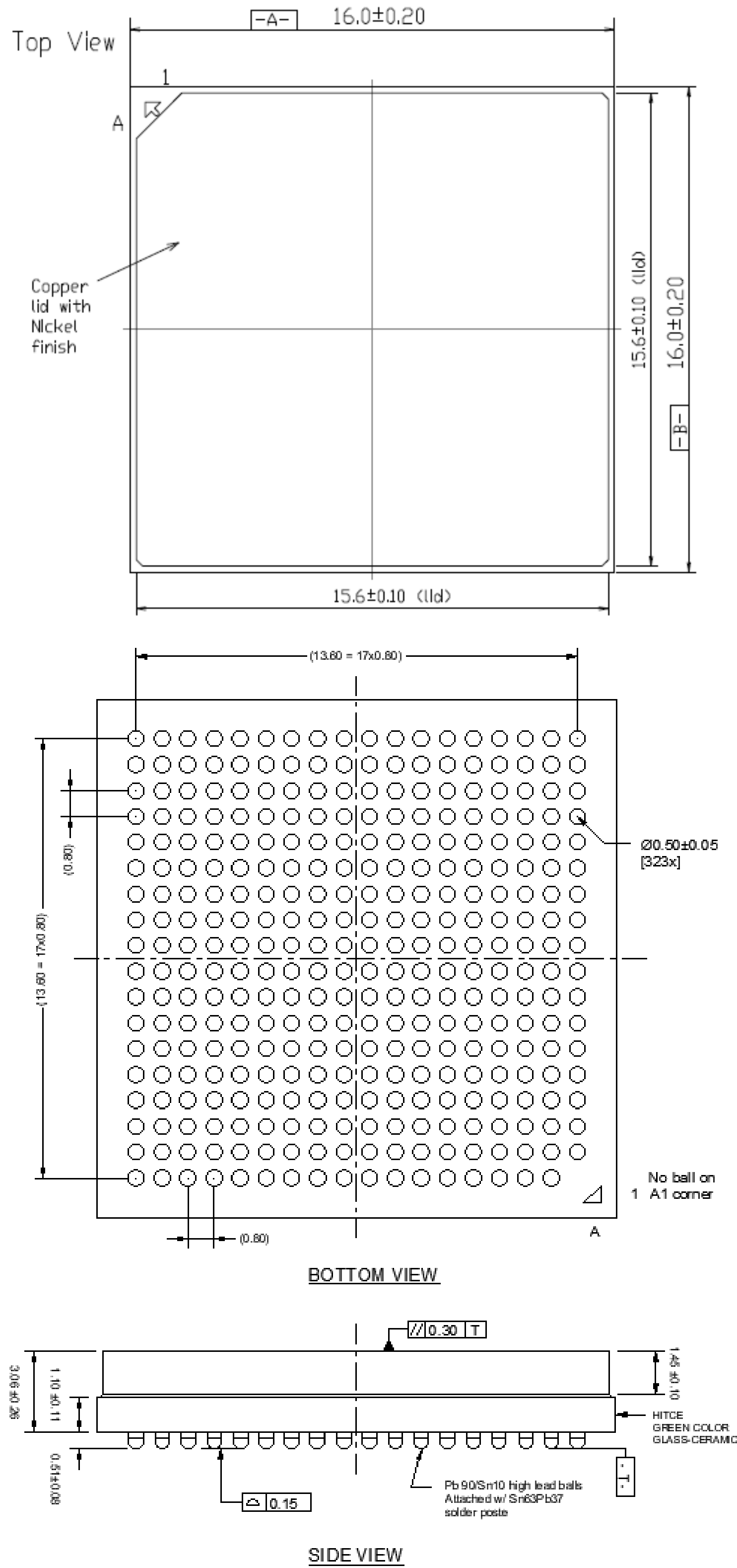


FIGURE 1. Case outline X (BGA Package).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		AGND	AGND	SYNCON	SYNCOP	AGND	CLKOUTN	CLKOUTP	AGND	AGND	CLKP	CLKN	AGND	SYNCTRIGP	SYNCTRIGN	AGND	AGND	DGND	A
B	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	B
C	miso	miso	rstn	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SSON	SSOP	AGND	DGND	DGND	VSPI_SEL	C
D	GNDO	GNDO	DNC	csn	sclk	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DNC	GNDO	GNDO	D
E	GNDO	GNDO	GNDO	DNC	DNC	DGND	AGND	AGND	VCCA	VCCA	AGND	AGND	DGND	DNC	DNC	GNDO	GNDO	GNDO	E
F	ASL1P	ASL1N	GNDO	GNDO	VCC_SPI	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	VCCD	GNDO	GNDO	DSLIN	DSLIP	F
G	GNDO	GNDO	GNDO	GNDO	DNC	VCCD	AGND	VCCA	VCCA	VCCA	VCCA	AGND	VCCD	DNC	GNDO	GNDO	GNDO	GNDO	G
H	ASL0P	ASL0N	GNDO	VCCO	VCCO	VCCD	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCD	VCCO	VCCO	GNDO	DSLON	DSLOP	H
J	GNDO	GNDO	GNDO	GNDO	GNDO	DGND	AGND	VCCA	AGND	AGND	VCCA	AGND	DGND	GNDO	GNDO	GNDO	GNDO	GNDO	J
K	BSL0P	BSL0N	GNDO	VCCO	VCCO	VCCD	AGND	VCCA	VCCA	VCCA	VCCA	AGND	VCCD	VCCO	VCCO	GNDO	CSLON	CSLOP	K
L	GNDO	GNDO	GNDO	GNDO	GNDO	DGND	AGND	VCCA	AGND	AGND	VCCA	AGND	DGND	GNDO	GNDO	GNDO	GNDO	GNDO	L
M	BSLIP	BSLIP	GNDO	VCCO	VCCO	VCCD	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCD	VCCO	VCCO	GNDO	CSLIN	CSLIP	M
N	GNDO	GNDO	GNDO	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDO	GNDO	GNDO	N
P	GNDO	GNDO	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDO	GNDO	P
R	DIODE_C	DIODE_A	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DNC	CMIREF	R
T	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	T
U	AGND	AGND	AGND	IN0P	IN0N	AGND	IN1N	IN1P	AGND	AGND	IN2P	IN2P	AGND	IN3N	IN3P	AGND	AGND	AGND	U
V	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

FIGURE 2a. Terminal connections.

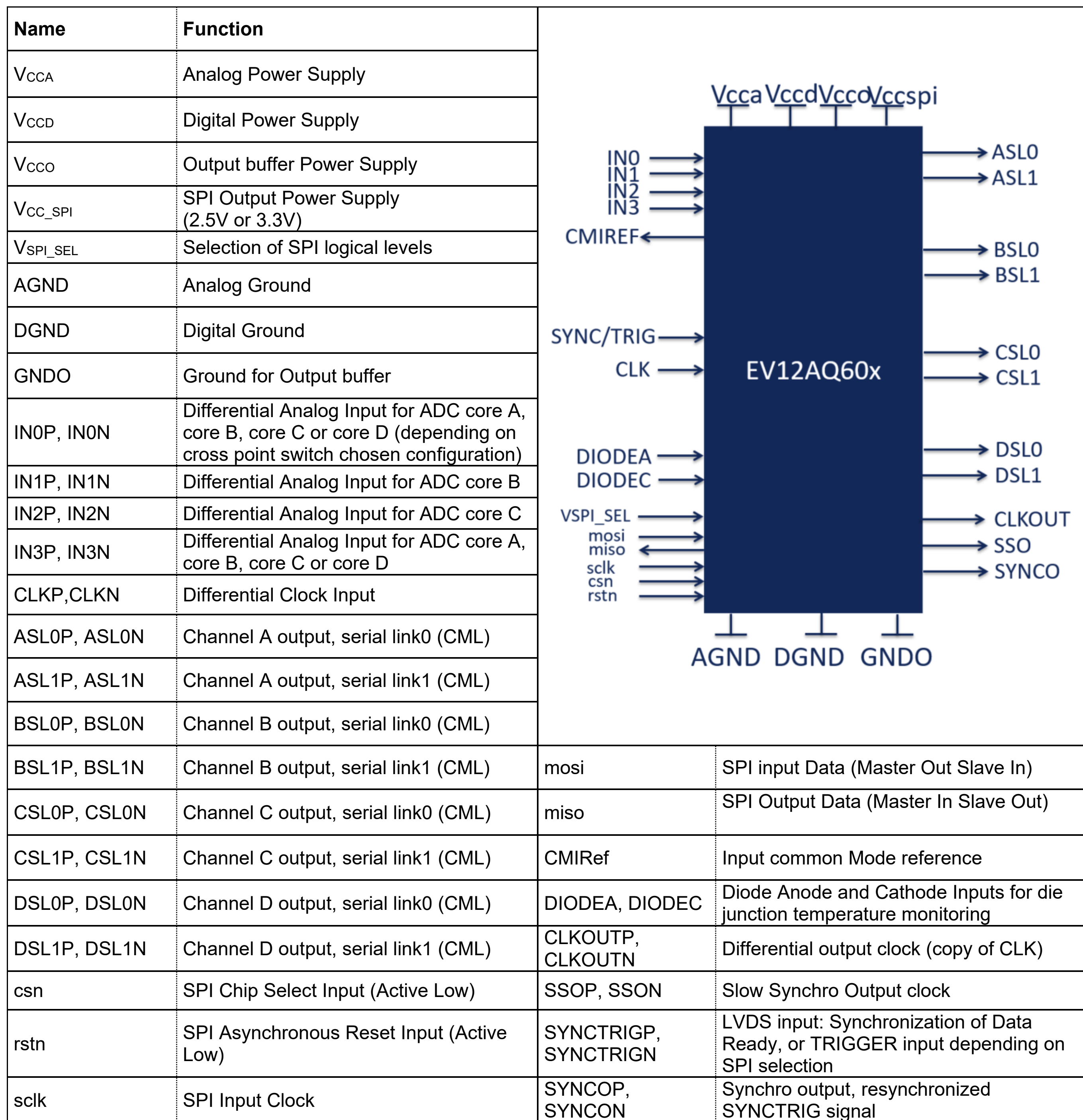
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		AGND	AGND	SYNCON	SYNCOP	AGND	CLKOUTN	CLKOUTP	AGND	AGND	CLKP	CLKN	AGND	SYNCTRIGP	SYNCTRIGN	AGND	AGND	DGND	A
B	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	B
C				DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SSON	SSOP	AGND	DGND	DGND		C
D	GNDO	GNDO				AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND		GNDO	GNDO	D
E	GNDO	GNDO				DGND	AGND	AGND	VCCA	VCCA	AGND	AGND	DGND			GNDO	GNDO	GNDO	E
F	31,9	24,9	GNDO	GNDO		DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	VCCD	GNDO	GNDO	24,9	31,9	F
G	GNDO	GNDO	GNDO	GNDO		VCCD	AGND	VCCA	VCCA	VCCA	VCCA	AGND	VCCD		GNDO	GNDO	GNDO	GNDO	G
H	27,4	20,3	GNDO	VCCO	VCCO	VCCD	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCD	VCCO	VCCO	GNDO	20,3	27,3	H
J	GNDO	GNDO	GNDO	GNDO	GNDO	DGND	AGND	VCCA	AGND	AGND	VCCA	AGND	DGND	GNDO	GNDO	GNDO	GNDO	GNDO	J
K	25,4	18,4	GNDO	VCCO	VCCO	VCCD	AGND	VCCA	VCCA	VCCA	VCCA	AGND	VCCD	VCCO	VCCO	GNDO	18,4	25,4	K
L	GNDO	GNDO	GNDO	GNDO	GNDO	DGND	AGND	VCCA	AGND	AGND	VCCA	AGND	DGND	GNDO	GNDO	GNDO	GNDO	GNDO	L
M	23,6	16,6	GNDO	VCCO	VCCO	VCCD	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCD	VCCO	VCCO	GNDO	16,6	23,6	M
N	GNDO	GNDO	GNDO	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDO	GNDO	GNDO	N
P	GNDO	GNDO	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GNDO	GNDO	P
R			AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND			R
T	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	T
U	AGND	AGND	AGND	IN0P	IN0P	AGND	IN1N	IN1P	AGND	AGND	IN2P	IN2N	AGND	IN3N	IN3P	AGND	AGND	AGND	U
V	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

PACKAGE AXIS

NOTE:
1. For further information, please refer to manufacturer data §4.3

FIGURE 2b. Terminal connections (Skew mapping)-continue.

Functional description



Name	Function
V_{CCA}	Analog Power Supply
V_{CCD}	Digital Power Supply
V_{CCO}	Output buffer Power Supply
V_{CC_SPI}	SPI Output Power Supply (2.5V or 3.3V)
V_{SPI_SEL}	Selection of SPI logical levels
AGND	Analog Ground
DGND	Digital Ground
GNDO	Ground for Output buffer
IN0P, IN0N	Differential Analog Input for ADC core A, core B, core C or core D (depending on cross point switch chosen configuration)
IN1P, IN1N	Differential Analog Input for ADC core B
IN2P, IN2N	Differential Analog Input for ADC core C
IN3P, IN3N	Differential Analog Input for ADC core A, core B, core C or core D
CLKP,CLKN	Differential Clock Input
ASL0P, ASL0N	Channel A output, serial link0 (CML)
ASL1P, ASL1N	Channel A output, serial link1 (CML)
BSL0P, BSL0N	Channel B output, serial link0 (CML)
BSL1P, BSL1N	Channel B output, serial link1 (CML)
CSL0P, CSL0N	Channel C output, serial link0 (CML)
CSL1P, CSL1N	Channel C output, serial link1 (CML)
DSL0P, DSL0N	Channel D output, serial link0 (CML)
DSL1P, DSL1N	Channel D output, serial link1 (CML)
csn	SPI Chip Select Input (Active Low)
rstn	SPI Asynchronous Reset Input (Active Low)
sclk	SPI Input Clock
mosi	SPI input Data (Master Out Slave In)
miso	SPI Output Data (Master In Slave Out)
CMIRef	Input common Mode reference
DIODEA, DIODEC	Diode Anode and Cathode Inputs for die junction temperature monitoring
CLKOUTP, CLKOUTN	Differential output clock (copy of CLK)
SSOP, SSON	Slow Synchro Output clock
SYNCTRIGP, SYNCTRIGN	LVDS input: Synchronization of Data Ready, or TRIGGER input depending on SPI selection
SYNCOP, SYNCON	Synchro output, resynchronized SYNCTRIG signal

FIGURE 3. Functional description.

Pinout Functions.

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Power supplies				
AGND	A2, A3, A6, A9, A10, A13, A16, A17; B3, B4, B5, B6, B7, B8, B9, B10, B11,B12, B13, B14, B15, B16; C5, C6, C7, C8, C9, C10, C11, C12, C15; D6, D7, D8, D9, D10, D11, D12, D13, D14; E7, E8, E11, E12 F7, F8, F9, F10, F11, F12; G7, G12; H7, H8, H11, H12; J7, J9, J10, J12; K7, K12; L7, L9, L10, L12; M7, M8, M11, M12; N4, N5, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15; P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16; R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16; T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18; U1, U2, U3, U6, U9, U10, U13, U16, U17, U18; V1, V2, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18;	Analog ground All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		
DGND	A18; B1, B2, B17, B18; C4, C16, C17; D15; E6, E13; F6, F13; J6, J13; L6, L13;	Digital ground All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		

FIGURE 4. Pinout Functions.

Pinout Functions – Continued.

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Power supplies – Continued.				
GNDO	D1, D2, D17, D18; E1, E2, E3, E16, E17, E18; F3, F4, F15, F16; G1,G2, G3, G4, G15, G16, G17, G18; H3, H16; J1, J2, J3, J4, J5, J14, J15, J16, J17, J18; K3, K16; L1, L2, L3, L4, L5, L14, L15, L16, L17, L18;M3, M16 N1, N2, N3, N16, N17, N18; P1, P2, P17, P18;	Ground for Output buffers All ground pins must be connected to a one solid ground (analog + digital) plane on PCB		
V_{CCA}	E9, E10; G8, G9, G10, G11; H9, H10; J8, J11; K8, K9, K10, K11; L8, L11; M9, M10;	Analog power supply		
V_{CC_SPI}	F5	SPI output power supply (2.5 V, 3.3 V)		
V_{CCD}	F14; G6, G13; H6, H13; K6, K13; M6, M13;	Digital power supply		
V_{CCO}	H4, H5, H14, H15; K4, K5, K14, K15; M4, M5, M14, M15;	Output power supply		

FIGURE 4. Pinout Functions - Continued.

Pinout Functions – Continued.

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Clock signal				
CLKP CLKN	A11, A12	In phase and Out of phase input clock signal	I	VCCA, 3.45KΩ, CLKN, 50Ω, 50Ω, 5.25pF, CLKP, GND, 13.45 KΩ, AGND
CLKOUTP CLKOUTN	A8, A7	In phase and Out of phase out clock signal	O	VCCA, 50 Ω, 50 Ω, CLKOUTP, CLKOUTN

FIGURE 4. Pinout Functions - Continued.

Pinout Functions – Continued.

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Analog signals				
IN0P IN0N	U4, U5	In phase analog input 0 Out of phase analog input 0 (must be unconnected if not used)	I	
IN1P IN1N	U8, U7	In phase analog input 1 Out of phase analog input 1 (must be unconnected if not used)	I	
IN2P IN2N	U11, U12	In phase analog input 2 Out of phase analog input 2 (must be unconnected if not used)	I	
IN3P IN3N	U15, U14	In phase analog input 3 Out of phase analog input 3 (must be unconnected if not used)	I	
CMIREF	R18	Output voltage reference In AC coupling operation this output could be left floating (not used) In DC coupling operation, these pins provides an output voltage which is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer.	O	

FIGURE 4. Pinout Functions - Continued.

Pinout Functions – Continued.

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Digital Output signals (CML)				
ASL0P, ASL0N	H1, H2	Channel A output data serial link 0	O	
ASL1P, ASL1N	F1, F2	Channel A output data serial link 1	O	
BSL0P, BSL0N	K1, K2	Channel B output data serial link 0	O	
BSL1P, BSL1N	M1, M2	Channel B output data serial link 1	O	
CSL0P, CSL0N	K18, K17	Channel C output data serial link 0	O	
CSL1P, CSL1N	M18, M17	Channel C output data serial link 1	O	
DSL0P, DSL0N	H18, H17	Channel D output data serial link 0	O	
DSL1P, DSL1N	F18, F17	Channel D output data serial link 1	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Digital output Signal (LVDS)				
SSOP, SSON	C14, C13	In phase and out of phase Slow Synchro Output.Fsso=Fclk/32	O	
SYNCOP, SYNCON	A5, A4	In phase and out of phase Sync Output.	O	

FIGURE 4. Pinout Functions - Continued.

Pinout Functions – Continued.

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Digital I/0 (CMOS)				
V_{SPI_SEL}	C18	used for logical level selection		
Sclk	D5	SPI signal Input SPI serial Clock Serial data is shifted into and out SPI synchronously to this signal on positive transition of sclk Internal pull-down	I	V_{CCO} IN 38 kΩ
Mosi	C2	SPI signal Data SPI Input signal (Master Out Slave In) Serial data input is shifted into SPI while sldn is active low Internal pull-down	I	
Csn	D4	SPI signal Input Chip Select signal (Active low) When this signal is active low, sclk is used to clock data present on MOSI or MISO signal Internal pull-up	I	V_{CCO} V_{CCO} 51 kΩ 11 kΩ IN 38 kΩ
Rstn	C3	SPI signal Input Digital asynchronous SPI reset (Active low) This signal allows to reset the internal value of SPI to their default value Internal pull-up	I	
Miso	C1	SPI signal Data output SPI signal (Master In Slave Out) Serial data output is shifted out SPI while csn is active low.	O	V_{CCD} Pdriv V_{Casc} V_{CCO} MISO 80 ohms 4mA Ndriv

FIGURE 4. Pinout Functions - Continued.

Pinout Functions – Continued.

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
DIGITAL INPUT (LVDS)				
SYNCTRIGP SYNCTRIGN	A14, A15	Differential Input Synchronization signal (LVDS) Active high signal This signal is used to synchronize internal ADC, if enabled Equivalent internal differential 100Ω input resistor Functionality Sync or Trigger depends on SPI selection	I	VCCA 13 KΩ SYNCTRIG SYNCTRIG 7.5KΩ AGND *****
MISCELLANEOUS				
DiodeA, DiodeC	R2, R1	Junction Temperature Monitoring diode Anode Junction Temperature Monitoring diode Cathode Cathode must be connected to ground (AGND) externally	I	DiodeC DiodeA

FIGURE 4. Pinout Functions - Continued.

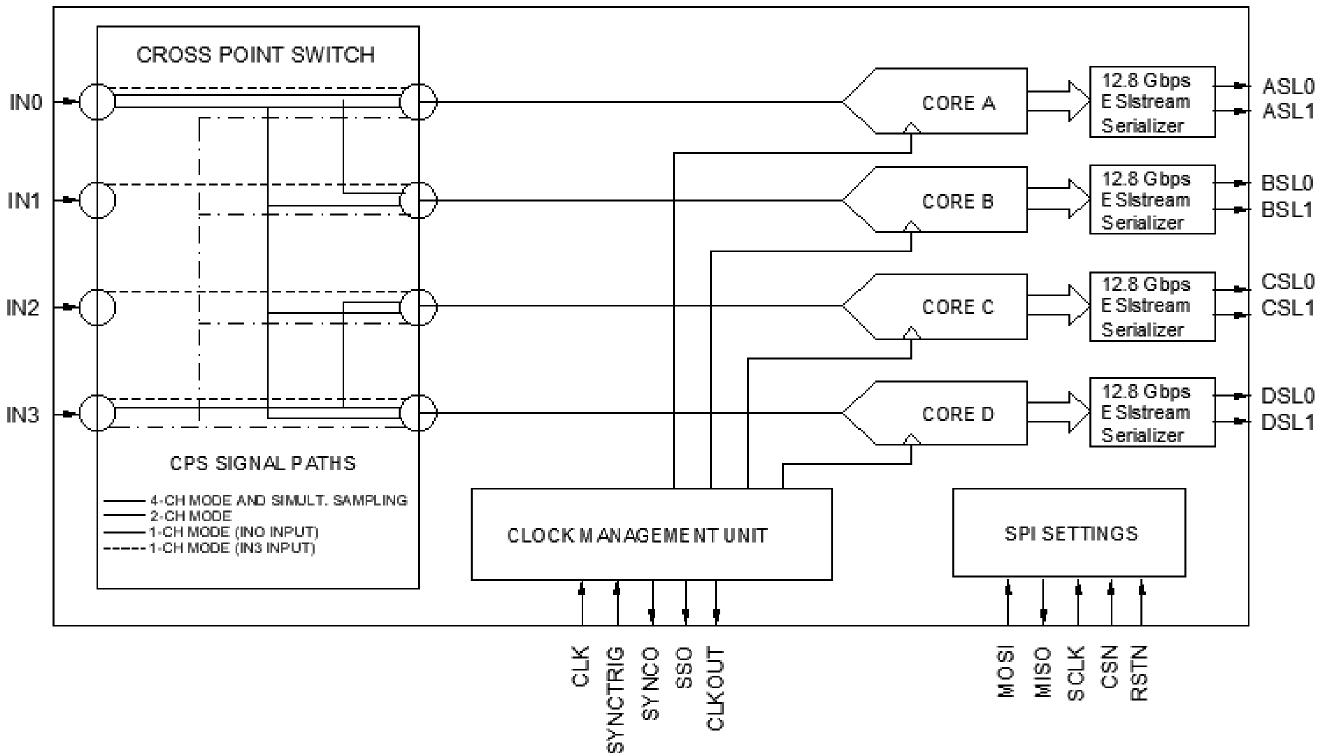


FIGURE 5. Block diagram.

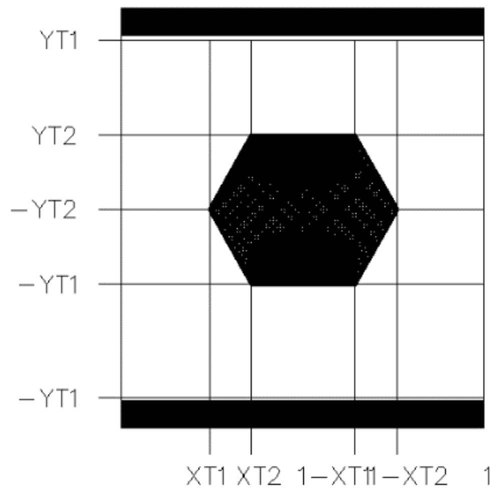


FIGURE 6. Serial link eye diagram.

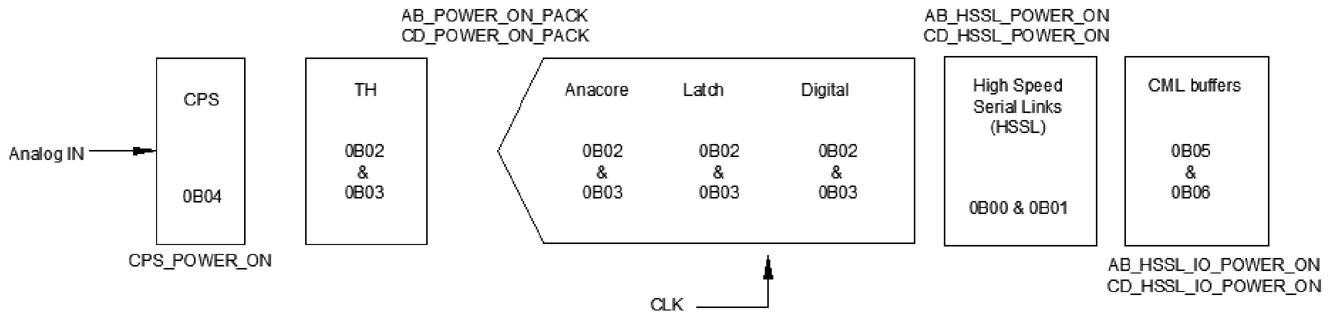


Figure 7: Differential Internal blocks.

CLOCK
X ANALOG INPUT
SYNCTRIG
Sampling sample N
CSL0
Sample N encoded / CBx = 0
Sampling sample N+4
CSL1
Sample N+4 encoded / CBx = 1
Sampling sample N+1
DSL0
Sample N+1 encoded / CBx = 1
Sampling sample N+5
DSL1
Sample N+5 encoded / CBx = 0
Sampling sample N+2
ASL0
Sample N+2 encoded / CBx = 1
ASL1
Sample N+6 encoded / CBx = 0
Sampling sample N+3
BSL0
Sample N+3 encoded / CBx = 1
BSL1
Sample N+7 encoded / CBx = 0

Figure 8: Trigger mode timing diagram in serial interface.

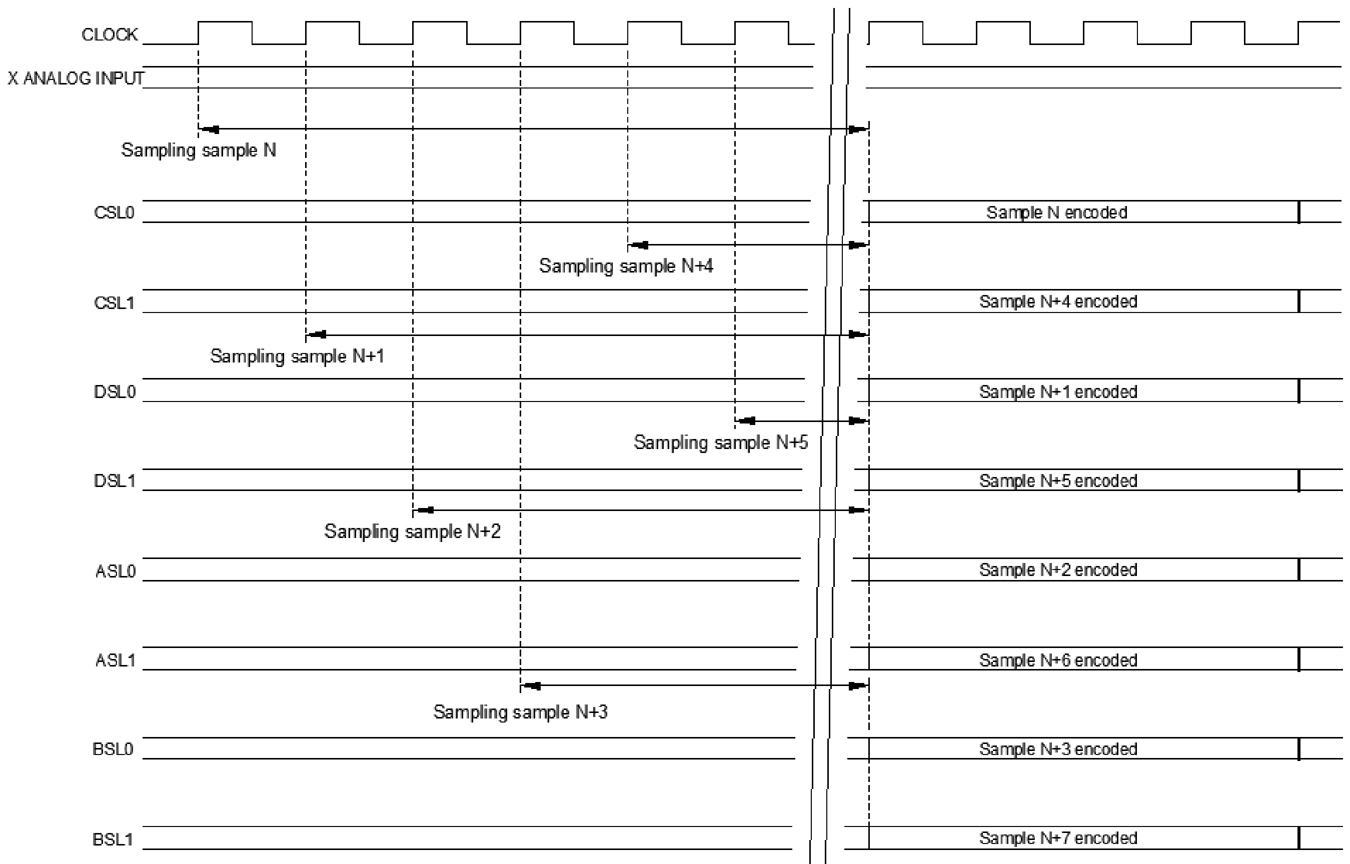


Figure 9: Timing diagram in serial interface in 1-channel mode.

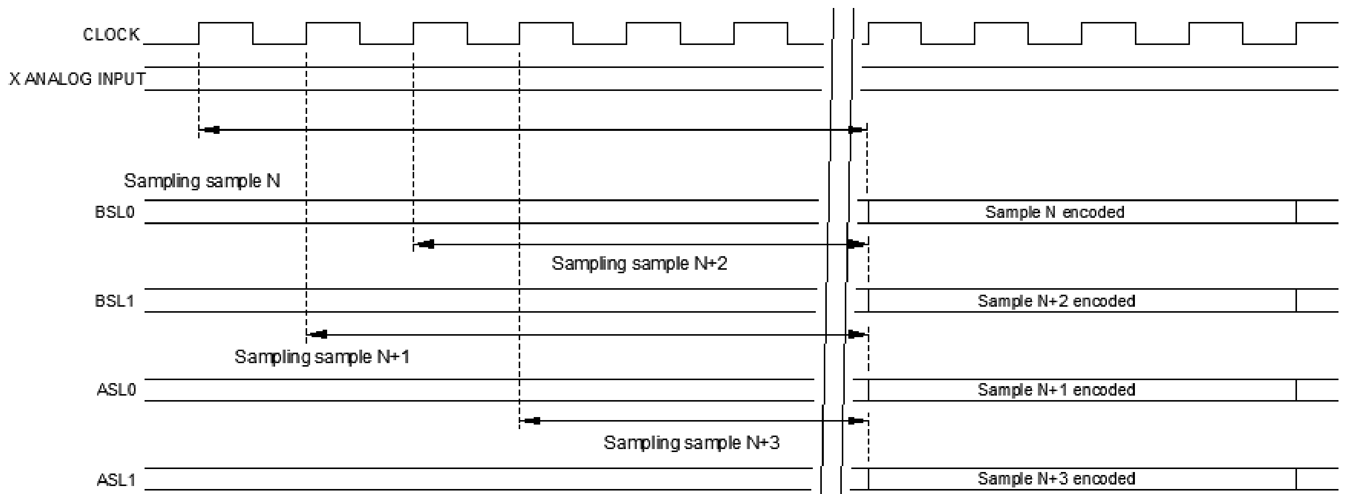


Figure 10: Timing diagram in serial interface in 2-channel mode.

Parameter	Symbol	Value	Unit
Thermal resistance from junction to bottom of balls 1/ 2/	$Rth_{Junction\ to\ Bottom\ of\ balls}$	4.0	°C/Watt
Thermal resistance from junction to board (JEDEC JESD51-8) 1/ 2/	$Rth_{Junction\ -\ board}$	5.5	°C/Watt
Thermal resistance from junction to top of lid 1/ 2/	$Rth_{Junction\ –\ lid}$	2.05	°C/Watt
Thermal resistance from junction to ambient (JEDEC standard) 1/ 3/	$Rth_{Junction\ –\ ambient}$	19.2	°C/Watt
Delta temperature Hot spot – temperature from diode		+6.2	°C

NOTES:

1. Rth are calculated from hot spot, not from average temperature of the die.
   They are thermal simulation results (finite elements method) with nominal cases.
2. Assumptions:
   - no air, pure conduction
   - no radiation
3. Assumptions:
   - Convection according to JEDEC
   - Still air
   - Horizontal 2s2p board
   - Board size 114.3 x 76.2 mm, 1.6 mm thickness

FIGURE 11. Thermal characteristics.

4. VERIFICATION

4.1 Sampling and inspection. For device class Y, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device class Y, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Burn-in criteria for class Y device.

a. The manufacturers shall provide appropriate burn-in information herein table II in accordance with JEDEC publication JEP163. The burn-in test duration, test condition and test temperature shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table III herein.

c. Additional screening for device class Y shall be required as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device class Y. Qualification inspection for device class Y shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for class Y shall be performed in accordance with MIL-PRF-38535 including groups A, B, C, D, and E (RHA test) and as specified.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Devices induced latch-up tests are required for device class Y. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device class Y, subgroups 7 and 8 tests shall be sufficient to verify the truth table on figure 2 herein or verifying the functionality of the device.

4.4.2 Group B inspection.

a. For class Y flip chip devices with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures of lid shear test for approval.

b. For ball grid array (BGA) packages, ball shear test shall be performed in accordance with JESD22-B117.

c. For column grid array (CGA) packages, solder column pull test shall be performed in accordance with TM 2038 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements (in accordance with MIL-PRF-38535, screening table I, group A, B, C, D, E and MIL-STD-883 test method)	Subgroups (in accordance with MIL-PRF-38535, table III)
	Device class Y
Interim electrical parameters, (screening table I)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Static burn-in I, method 1015 (see 4.2.1a)	Required 1/
Static burn-in II method 1015 (see 4.2.1a)	Required 1/
Dynamic burn-in , method 1015 (see 4.2.1a)	Required 1/
Final electrical parameters, (screening table I)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4.1)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group B end point electrical parameters, (see 4.4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters, (see 4.4.3)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group D end-point electrical parameters, (see 4.4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group E end-point electrical parameters, (see 4.4.5) 3/	1, 7, 9
Post ball attach electrical parameters test (see 4.2) 3/	1, 7, 9

1/ The manufacturers shall be provide appropriate burn-in information herein table II in accordance with burn-in publication JEP163.
2/ PDA applies to subgroups 1 and 7.
3/ For flip chip class Y BGA/CGA devices, screening and group A, B, C, D and RHA test group E shall be performed at land grid array (LGA) level (i.e. before ball or column attached to the devices). After ball or column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.

TABLE III. Burn-in and operating life test delta parameters (+25°C).

All critical parameter 1/ 2/	Symbol	Delta limits 3/
Power dissipation	P_{OWER}	±5%
Analog Power Supply Current	I_{CCA}	±5%
Input Common Mode I_{N0}	VICM	±5%
SAon_clkOUT_VOH_N	ClkOut V_{OH}	±5%
SAon_clkOUT_VOL_N	ClkOut V_{OL}	±5%
Signal to Noise Ratio	SNR	±2%

1/ These parameters shall be recorded before and after the required burn-in to determine delta drift limits.
2/ Manufacturer shall be specified in table III all critical parameters that have delta drift values during burn-in test.
3/ The delta drift limit shall be computed with reference to the previous interim electrical parameters. The delta drift limit shall be specified in table III.

4.4.3. Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein. For device class Y steady-state life tests circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.3.1 Additional criteria for device class Y. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class Y, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.5.1.1 Accelerated annealing testing. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.5.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.5.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

a. Transient dose rate upset testing for class Y devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.5.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 or C JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip. Range of the ion which shall be sufficiently penetrate well beyond the deepest part volume of the devices to of the sensitive detect latch-up.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

4.4.5.5 Neutron irradiation/displacement damage testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I, for the subgroups specified in table IIA herein at T_A = +25 °C ±5 °C after an exposure of 1 x 10^{12} neutrons/cm^2.

4.5 Delta measurements for device class Y. Class Y devices, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with MIL-PRF-38535, table III. Delta limits shall be required on class Y devices, and shall be recorded before and after the required burn-in screens and steady-state life tests to determine delta limit compliance. The electrical parameters to be measured, with associated delta limits are listed in table III.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device class Y.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device class Y. Sources of supply for device class Y are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Package integrity demonstration test plan (PIDTP). For class Y microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Flip chip PIDTP also shall address the materials and processes unique to solder bump interconnect attach, underfill and thermal interface materials (TIM). The QA approved PIDTP shall be documented in the product QM plan and shall be available upon requested in the purchase order or contract.

6.8 BGA packages lead finish: Microcircuits devices for ball grid array (BGA) packages are supplying to this drawing with terminal lead finish mark “F”. Terminal lead finish F is tin (Sn) and lead (Pb) alloy, and solder ball material contains compositions of Sn= 10% and Pb=90%.

6.9 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-01-13

Approved sources of supply for SMD 5962-21214 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-2121401YXF	F8385	EV12AQ600AMGH-Y

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8385	Teledyne e2v Semiconductors Avenue De Rochepleine BP 123 Saint Egreve CEDEX-38521, France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.