REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02 and case outline Y. -rrp	23-12-15	James R. Eschmeyer

Revision Status of Sheets

REV	A	A	A																			
SHEET	23	24	25																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
23-06-12

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

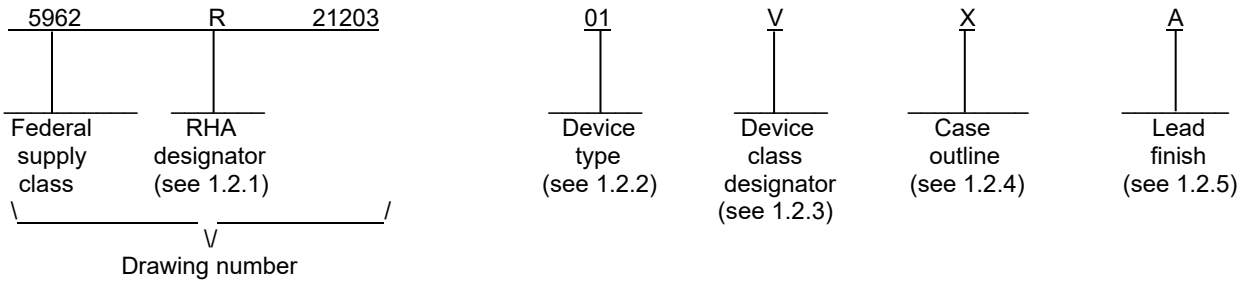
MICROCIRCUIT, LINEAR, LOW DROPOUT, VOLTAGE REGULATOR, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL A	SIZE A	CAGE CODE **67268**	**5962-21203**
		SHEET	1 OF 25	

1. SCOPE

1.1 Scope. This drawing documents product assurance class levels consisting of high reliability (device class Q), space application (device class V or Y), and plastic encapsulated microcircuits (PEM) (device class N) for military, terrestrial and avionics application and device class P for space application. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device classes N and P, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. RHA marked devices classes are N, P, Q, Y, and V and meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H1111-SP	Radiation hardened, 1.5 A, low noise, low dropout, voltage regulator
02	TPS7H1111-SP (QMLP)	Radiation hardened, 1.5 A, low noise, low dropout, voltage regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N or P	Certification and qualification to MIL-PRF-38535 for PEM performance environments.
Y	Certification and qualification to MIL-PRF-38535. Non hermetic flip chip technology on a ceramic or organic substrate.
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, JEDEC Publication 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	14	Flat pack
Y	See figure 1	28	Plastic small outline package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, P, Q, Y, and V.

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage:
- IN ..... -0.3 V to 7.5 V
- BIAS ..... -0.3 V to 16 V
- EN, PG, FB_PG, OUTS, CLM ..... -0.3 V to 7.5 V

Output voltage:
- OUT ..... -0.3 V to 7.5 V
- SS_SET, REF, STAB ..... -0.3 V to 7.5 V

Input current of PG ..... -0.001 A to 0.01 A
Output current of OUT ..... -2 A to 2.25 A
Junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Case X:
- Thermal resistance, junction to ambient ($R\theta_{JA}$) ..... 25.1°C/W
- Thermal resistance, junction to case (top) ($R\theta_{JC(top)}$) ..... 6.3°C/W
- Thermal resistance, junction to board ($R\theta_{JB}$) ..... 9.3°C/W
- Characterization parameter, junction to top (Ψ_{JT}) ..... 1.4°C/W
- Characterization parameter, junction to board (Ψ_{JB}) ..... 9.1°C/W
- Thermal resistance, junction to case (bottom) ($R\theta_{JC(bot)}$) ..... 0.5°C/W

Case Y:
- Thermal resistance, junction to ambient ($R\theta_{JA}$) ..... 24.4°C/W
- Thermal resistance, junction to case (top) ($R\theta_{JC(top)}$) ..... 15.8°C/W
- Thermal resistance, junction to board ($R\theta_{JB}$) ..... 6.4°C/W
- Characterization parameter, junction to top (Ψ_{JT}) ..... 0.2°C/W
- Characterization parameter, junction to board (Ψ_{JB}) ..... 6.4°C/W
- Thermal resistance, junction to case (bottom) ($R\theta_{JC(bot)}$) ..... 0.7°C/W

Electrostatic discharge (ESD) rating:
- Human body model (HBM), per JEDEC JS-001, all pins ..... ±2000 V 2/
- Charge device model (CDM), per JEDEC JS-002, all pins ..... ±1000 V 3/

1/ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
2/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
3/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

1.4 Recommended operating conditions.

Input voltage:
- IN ..... 0.85 V to 7 V
- BIAS 4/ ..... V_{IN} to 14 V
  2.2 V to 14 V
- PG, EN ..... 0 V to 7 V
- FB_PG ..... 0 V to 6 V
- CLM ..... 0 V to V_{IN}

Output voltage:
- OUT 5/ ..... $V_{IN} – V_{DO}$ maximum
  0.4 V to 5.5 V
- SS_SET 5/ ..... $V_{IN} – V_{DO}$ maximum
  0.4 V to 5.5 V

Input current of PG ..... 0 A to 0.002 A
Output current of OUT ..... 0 A to 1.5 A
Output bulk capacitance: 6/
- COUT ..... 132 µF to 308 µF
- ESR ..... 7 mΩ to 40 mΩ
- ESL ..... 0.8 nH to 2.4 nH

Reference configuration (RREF) ..... 11 kΩ to 13 kΩ
EN toggle time (t_{EN_LOW}) 7/ ..... 20 µs minimum
Ambient operating temperature range (T_A) ..... -55°C to +125°C
Glass transition temperature:
- Mold compound (T_g) ..... +115°C nominal 8/

4/ BIAS has two minimum values, V_{IN} and 2.2 V. BIAS must be set greater than or equal to the larger of these two values. The BIAS max value is always 14 V. For full performance set $V_{BIAS} \geq V_{OUT}$ + 1.6 V. See the manufacturer's datasheet for further details

5/ OUT and SS_SET have two maximum values, ($V_{IN} – V_{DO}$) and 5.5 V. OUT and SS_SET must be set to less than or equal to the smaller of these two values. The OUT and SS_SET min value is always 0.4 V.

6/ These are the default acceptable output capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL) values for the bulk capacitance. Other values may be acceptable, such as by modifying the control loop with external compensation using the STAB pin. Tantalum or Tantalum Polymer capacitors are normally used to meet these requirements. Additional ceramic decoupling capacitors are not required, but a single 0.1 µF ceramic capacitor with low ESL near the point of load is acceptable. Additional larger ceramic capacitors are not needed due to the high PSRR and low noise provided by the device LDO across a wide bandwidth. Therefore, the device is not designed to support larger ceramic capacitors. See the manufacturer's datasheet for additional information.

7/ t_{EN_LOW} is the time the EN pin must be driven low before again being driven high for the device to detect a reset. This is generally only applicable when attempting to exit turn-off current limit mode.

8/ Glass transition temperature (Tg) of Mold compound measured spec value 115°C but tested Tg is 135°C.

1.5 Radiation features.

Maximum total dose available (effective dose rate = 0.165 Rad(Si)/s).....100 krads(Si) 9/
Heavy ion Single Event Phenomena (SEP) test:
No SEL occurs at effective LET (see 4.4.5.2) ..... ≤ 75 MeV-cm^2 /mg 10/
No SEB observe at effective LET (see 4.4.5.2) ..... ≤ 75 MeV-cm^2 /mg 10/
No SEGR observe at effective LET (see 4.4.5.2) ..... ≤ 75 MeV-cm^2 /mg 10/
Neutron/Displacement damage test (1-MeV equivalent): ..... = 1 x 10^{13} n/cm^2 11/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

9/ The manufacturer supplying 7th generation BiCMOS (LBC7) technology (which is over 99% CMOS components) devices performed total ionizing dose (TID) characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads(Si). However, device type 01 is irradiated at dose rate = 50 - 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate for device type 01 after extended room temperature anneal = 0.165 rad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower environment. For more information on TID test report, please contact device manufacturer.

10/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Holmiun (165Ho) ion beam was used at an angle of incidence of 0° at flux of 105 ions/cm2·s, fluences level of 107 ions/cm2 and a temperature of 125°C and no single event latch-up (SEL) was observed at LET of 75 MeV·cm2/mg. Manufacturer also test Single event burnout (SEB) and Single event gate rupture (SEGR) test with Holmiun (165Ho) ion beam at an angle of incidence of 0°. No SEB/SEGR observed up to LET of 75 MeV·cm2/mg. For more information on SEE/SEP test please contact device manufacturer.

11/ Neutron/Displacement damaged dosimetry test was performed at VPTRad facility in Chelmsford Massachusetts. The results show that all devices were fully functional and within production test limits after having been irradiated up to 1 × 10^{13} n/cm2 (1-MeV equivalent). A sample size of nine units was exposed to radiation testing per MIL-STD-883, Method 1017 for Neutron Irradiation, and an additional one device was used as a control unit and was not irradiated. For more information on neutron displacement damage test, please contact device manufacturer.

2.2 Non-Government publications. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JS-001 – Human Body Model Testing of Integrated Circuits
JS-002 - Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level
JEP155 – Recommended ESD Target Levels for HBM/MM Qualification.
JEP157 – Recommended ESD-CDM Target Levels.

(Copies of these documents are available online at https://www.jedec.org/).

ELECTRONIC COMPONENTS INDUSTRY ASSOCIATION

RS-198 – Ceramic Dielectric Capacitors Classes 1, 2, and 3

(Copy of this document is available online at https://www.ecianow.org/).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, P, Q, Y, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supplies and currents							
Dropout voltage with $V_{BIAS} \ge V_{OUT} + 1.6$ V	V_{DO}	I_{OUT} = 0.1 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	1, 2, 3	01, 02		40	mV
		I_{OUT} = 0.5 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$				150	
		I_{OUT} = 1 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$				280	
		I_{OUT} = 1.5 A, 0.85 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$				430	
Dropout voltage with $V_{BIAS} = V_{IN}$	V_{DO}	I_{OUT} = 0.1 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$	1, 2, 3	01, 02		1100	mV
		I_{OUT} = 0.5 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$				1150	
		I_{OUT} = 1 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$				1250	
		I_{OUT} = 1.5 A, 2.2 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 98.5% × $V_{OUT(NOM)}$				1400	
Output current limit	I_{LIM}	2.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.5 V , $V_{CLM} = V_{IN}$	3	01, 02	1.8	2.1	A
			1		1.75	2	
			2		1.7	1.95	
CLM input leakage current	$I_{CLM(LKG)}$	V_{CLM} = 7 V	1, 2, 3	01, 02		150	nA
Quiescent current	I_{Q_IN}	V_{EN} = 7 V, I_{OUT} = 0 A	1, 2, 3	01, 02		27	mA
Bias current with no output load	I_{Q_BIAS}	V_{EN} = 7 V, I_{OUT} = 0 A	1, 2, 3	01, 02		25	mA
$I_{IN} - I_{OUT}$ with full output load	I_{IN_GND}	V_{EN} = 7 V, I_{OUT} = 1.5 A	1, 2, 3	01, 02		27	mA
Bias current with full output load	I_{BIAS}	V_{EN} = 7 V, I_{OUT} = 1.5 A	1, 2, 3	01, 02		25	mA
Shutdown current	I_{SHDN}	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V	1, 2, 3	01, 02		350	µA
Shutdown bias current	I_{SHDN_BIAS}	V_{EN} = 0 V, I_{OUT} = 0 A, V_{OUT} = 0 V	1, 2, 3	01, 02		1000	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Accuracy							
Output voltage accuracy	V_{ACC}	1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V 3/, P_D ≤ 4 W 4/	1, 2, 3	01, 02	-1.3	1.2	%
			3		-1.3	0.5	
			1		-0.7	0.9	
			2		-0.7	1.2	
		M,D,P,L,R, 1 mA ≤ I_{OUT} ≤ 1.5 A, 2.2 V ≤ V_{BIAS} ≤ 14 V 3/, P_D ≤ 4 W 4/	1		-0.7	1.1	
SS_SET pin current to set V_{OUT}	I_{SET}		1, 2, 3	01, 02	98.8	101	µA
			3		98.8	100.3	
			1		99.0	100.9	
			2		99.2	101	
Output offset voltage ($V_{OUT} - V_{SS\_SET}$)	V_{OS}		1, 2, 3	01, 02	-2	0.78	mV
			3		-1.33	0.78	
			1		-1.45	0.76	
			2		-2.0	0.7	
		M,D,P,L,R	1		-1.45	1.5	
Reference voltage	V_{REF}		1, 2, 3	01	1.191	1.220	V
				02	1.190	1.221	
Line regulation	$\Delta V_{OUT} / \Delta V_{IN}$	0.85 V ≤ V_{IN} ≤ 7 V, I_{OUT} = 1 mA, V_{BIAS} = 5 V, V_{OUT} = 0.4 V, see figure 4	1, 2, 3	01, 02		200	µV/V
Load regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	1 mA ≤ I_{OUT} ≤ 1.5 A, V_{BIAS} = 5 V, V_{IN} = 2.5 V V_{OUT} = 1.8 V, see figure 5	1, 2, 3	01, 02		1000	µV/A
OUTS leakage current	$I_{OUTS(LKG)}$		1, 2, 3	01, 02		200	nA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable							
Enable rising threshold (turn-on)	$V_{EN(rising)}$		1, 2, 3	01, 02	0.58	0.62	V
Enable falling threshold (turn-off)	$V_{EN(falling)}$		1, 2, 3	01, 02	0.48	0.52	V
EN propagation delay	$t_{EN(delay)}$	EN high to V_{OUT} = 10 mV	9, 10, 11	01, 02		500	µs
Enable input leakage current	$I_{EN(LKG)}$	V_{EN} = 7 V	1, 2, 3	01, 02		150	nA
Power good							
Power good rising threshold	$V_{FB\_PG(rising)}$		1, 2, 3	01, 02	290	313	mV
Power good hysteresis	$V_{FB\_PG(HYS)}$		1, 2, 3	01, 02	7	19	mV
FB_PG input leakage current	$I_{FB\_PG(LKG)}$	V_{FB_PG} = 6 V	1, 2, 3	01, 02		150	nA
Power good output low	$V_{PG(OL)}$	$I_{PG(SINK)}$ = 0 mA to 2 mA	1, 2, 3	01, 02		200	mV
Minimum V_{IN} or V_{BIAS} for valid PG ($V_{PG} < 0.5$ V)	$V_{IN(MIN\_PG)}$	$I_{PG(sink)}$ = 0.6 mA	1, 2, 3	01, 02		0.8	V
Power good leakage	$I_{PG(LKG)}$	V_{PG} = 7 V, $V_{FB\_PG} > V_{FB\_PG}$(rising threshold)	1, 2, 3	01, 02		2	µA
Soft start							
SS_SET pin current during startup	$I_{SS\_SET(start)}$		1, 2, 3	01, 02	1.68	2.52	mA

1/ Over 0.85 V ≤ V_{IN} ≤ 7 V, $V_{BIAS} \ge V_{OUT}$ + 1.6 V ($V_{IN} \le V_{BIAS} \le$ 14 V and $V_{BIAS} \ge$ 2.2 V), V_{OUT} (target) = V_{IN} – 1.6 V, I_{OUT} = 1 mA, C_{OUT} = 220 µF (a single 220 µF tantalum capacitor is utilized), R_{REF} = 12.0 kΩ, over operating temperature range (T_A = –55°C to 125°C); includes RLAT at T_A = 25°C for RHA devices.

2/ Device type 01 supplied to this drawing have been characterized through all levels M, D, P, L and R of irradiation. Pre and Post-irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see section1.5 herein).

3/ Additionally, $V_{BIAS} \ge V_{IN}$ and VBIAS ≥ VOUT + 1.6 V.

4/ P_D is the internal power dissipation. When P_D exceeds 4 W, the current is lowered to avoid excessive local heating (due to tester limitations).

Table IB. SEP test limits 1/ 2/ 3/ 4/

Device type	Test	
01, 02	SEL	No single vent latch-up (SEL) was observed at effective LET of 75 MeV·cm^2/mg.
01, 02	SEB/SEGR	No SEB/SEGR observed up to effective LET of 75 MeV·cm^2/mg.

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ The heavy-ion test performed at TAMU Cyclotron Radiation Effects Facility. Holmiun (165Ho) ion beam was used at an angle of incidence of 0° at flux of 10^5 ions/cm^2·s, fluences level of 10^7 ions/cm^2 and a temperature of 125°C and no single event latch-up (SEL) was observed at LET of 75 MeV·cm^2/mg. Manufacturer also test Single event burnout (SEB) and Single event gate rupture (SEGR) test with Holmiun (165Ho) ion beam at an angle of incidence of 0°. No SEB/SEGR observed up to LET of 75 MeV·cm^2/mg. For more information on SEE/SEP test please contact device manufacturer.

4/ SEL/SEB/SEGR were tested at the maximum recommended input voltage (VIN) of 7V and the maximum recommended bias voltage (VBIAS) of 14V. SEB/SEGR were tested under both enabled and disabled conditions

Case X

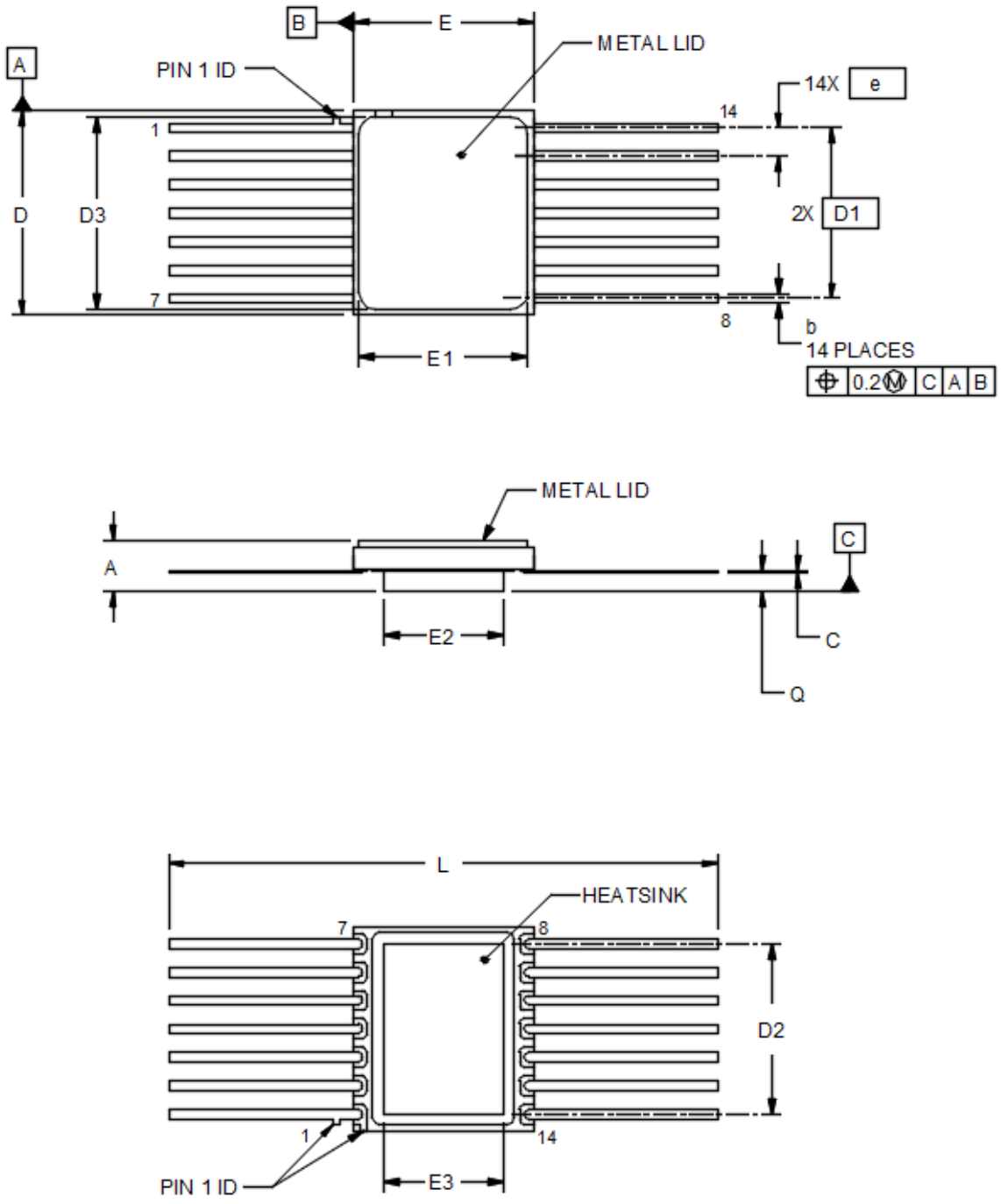


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-21203**
		REVISION LEVEL A	SHEET **11**

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.960	2.527	.0772	.0995
b	.380	.480	.015	.019
c	.100	.180	.004	.007
D	8.87	9.37	.349	.369
D1	7.62 BSC		.300 BSC	
D2	7.448	7.748	.293	.305
D3	8.62 REF		.339 REF	
E	7.78	8.28	.306	.326
E1	7.53 REF		.296 REF	
E2	5.31 REF		.209 REF	
E3	5.157	5.457	.203	.215
e	1.27 BSC		.050 BSC	
L	24.0	25.0	.945	.984
Q	.840	1.04	.033	.041

NOTE:
Controlling dimensions are millimeter, inch dimensions are given for reference only.

FIGURE 1. Case outline – continued.

Case Y

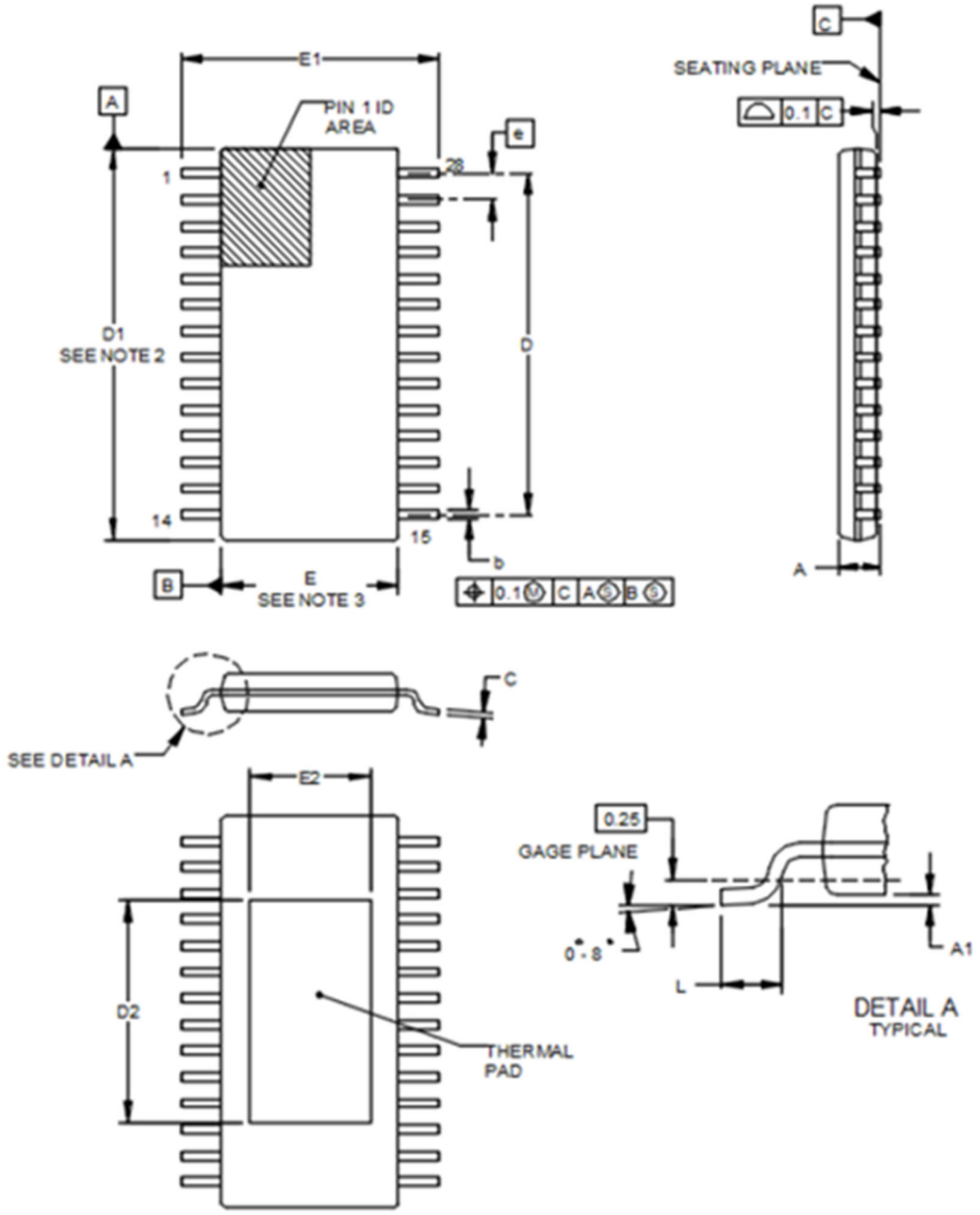


FIGURE 1. Case outline – continued.

Symbol	Dimensions			
	Inches		Millimeter	
	Minimum	Maximum	Minimum	Maximum
A	---	.043	---	1.1
A1	.001	.004	0.02	0.10
b	.007	.012	0.19	0.30
c	.003	.008	0.09	0.20
D	.332 BSC		8.45 BSC	
D1	.378	.386	9.6	9.8
D2	.207	.222	5.25	5.65
E	.169	.177	4.3	4.5
E1	.244	.260	6.2	6.6
E2	.108	.124	2.75	3.15
e	.026 BSC		0.65 BSC	
L	.020	.027	0.5	0.7

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension D1 does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (.006 inch) per side.
3. Dimension E does not include interlead flash. Interlead flash shall not exceed 0.25 mm (.010 inch) per side.

FIGURE 1. Case outline – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	BIAS	I	Bias supply. To support full output current, a separate bias supply is required if the headroom voltage is less than 1.6 V ($V_{headroom} = V_{IN} – V_{OUT} < 1.6$ V). Set the separate bias supply to a voltage at least 1.6 V higher than V_{OUT} for full output current support. A 12 V bias supply will satisfy these conditions (generally a 5 V supply will also suffice). There are no sequencing requirements between V_{BIAS} and V_{IN}. In order to limit noise on BIAS, an RC filter is recommended (typically 10 Ω and 4.7 µF) unless V_{BIAS} is an ultra-clean supply. If a separate bias supply is not used, connect BIAS to V_{IN} (it is also recommended to connect the V_{IN} rail to the BIAS pin through an RC filter).
2	EN	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to IN. Do not float this pin.
3, 4	IN	I	Input power. An input capacitor (nominally 10 µF) near this pin is recommended.
5	CLM	I	Current limit mode. Connect CLM to V_{IN} for brick-wall current limit mode (when current limit is reached, V_{OUT} is regulated to maintain a constant output current until the fault is removed). Connect CLM to GND for turn-off current limit mode (when current limit is reached, V_{OUT} stops regulating until EN is toggled). Do not change the value of this pin when the device is enabled, and do not float this pin.
6	GND	---	Ground
7	PG	O	Power good indicator. This is an open drain pin. Use a pull-up resistor to pull this pin up to V_{OUT} or the desired logic level. It is recommended to pull down PG to ground if unused but it may be left floating.
8	REF	I/O	Reference pin. REF outputs a nominal 1.2 V. Place a high accuracy 12.0 kΩ external resistor from REF to GND to set the internal 100 µA current source.

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
9	SS_SET	I/O	Soft-start and voltage set pin. An external capacitor (nominally 4.7 µF ceramic) is used to slow down the output voltage ramp rate during startup along with filtering internal device noise. Capacitor values less than 4.7 µF will result in marginally higher output noise. There is internal fast start circuitry to enable reasonable soft start times. Additionally, a resistor from SS_SET to GND sets the output voltage. During nominal operation, 100 µA is output on this pin and a resistor from SS_SET to GND sets the output voltage.
10	STAB	I/O	Stability pin. This is an output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Use a series capacitor (C_{COMP}) and resistor (R_{COMP}) of 4.7 nF and 5 kΩ to compensate the device. For different compensation options, see the manufacturer's datasheet. A C0G (NP0) type ceramic dielectric capacitor capable of withstanding the lower of V_{BIAS} or 7.5 V is recommended (for example, a 25 V rated caFBpacitor). See NOTE.
11, 12	OUT	O	Output power pin. The regulated output voltage. A single 220 Mf or two 100 Mf tantalum or tantalum polymer capacitors are recommended. See the manufacturer's datasheet for additional information.
13	OUTS	I	Output sense pin. This pin is used to sense the output voltage for regulation. Connect OUTS to the OUT pin at the desired point of regulation (remote sense).
14	FB_PG	I	Feedback and power good pin. The FB_PG pin enables setting of a configurable power good threshold. This is achieved by feeding the output voltage through a resistor divider to this pin (typical threshold of 300 Mv). When the threshold is reached, PG is asserted. Additionally, when the threshold on this pin is reached, start-up is over and the internal fast start circuitry is disabled. If this pin is connected directly to OUT, fast start operation ceases and PG is asserted as soon as V_{OUT} reaches 300 Mv (typical).
Thermal pad		---	Internally grounded. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation.
Metal lid	Lid	---	The lid is internally connected to the thermal pad and GND through the seal ring.

NOTE: Reference EIA standard RS-198: C0G, C = letter code meaning 0 temperature coefficient, 0 = temperature coefficient multiplier, and G = letter code. NP0 = Negative positive 0ppm/°C.

FIGURE 2. Terminal connections – continued.

Device type	02		
Case outline	Y		
Terminal number	Terminal symbol	I/O	Description
1, 2	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
3	BIAS	I	Bias supply. To support full output current, a separate bias supply is required if the headroom voltage is less than 1.6 V ($V_{headroom} = V_{IN} – V_{OUT} < 1.6$ V). Set the separate bias supply to a voltage at least 1.6 V higher than V_{OUT} for full output current support. A 12 V bias supply will satisfy these conditions (generally a 5 V supply will also suffice). There are no sequencing requirements between V_{BIAS} and V_{IN}. In order to limit noise on BIAS, an RC filter is recommended (typically 10 Ω and 4.7 µF) unless V_{BIAS} is an ultra-clean supply. If a separate bias supply is not used, connect BIAS to V_{IN} (it is also recommended to connect the V_{IN} rail to the BIAS pin through an RC filter).
4	EN	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to IN. Do not float this pin.
5	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
6, 7, 8	IN	I	Input power. An input capacitor (nominally 10 µF) near this pin is recommended.
9	CLM	I	Current limit mode. Connect CLM to V_{IN} for brick-wall current limit mode (when current limit is reached, V_{OUT} is regulated to maintain a constant output current until the fault is removed). Connect CLM to GND for turn-off current limit mode (when current limit is reached, V_{OUT} stops regulating until EN is toggled). Do not change the value of this pin when the device is enabled, and do not float this pin.
10, 11	GND	---	Ground
12	PG	O	Power good indicator. This is an open drain pin. Use a pull-up resistor to pull this pin up to V_{OUT} or the desired logic level. It is recommended to pull down PG to ground if unused but it may be left floating.
13, 14, 15, 16, 17	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.

FIGURE 2. Terminal connections – continued.

Device type	02		
Case outline	Y		
Terminal number	Terminal symbol	I/O	Description
18	REF	I/O	Reference pin. REF outputs a nominal 1.2 V. Place a high accuracy 12.0 kΩ external resistor from REF to GND to set the internal 100 µA current source.
19	SS_SET	I/O	Soft-start and voltage set pin. An external capacitor (nominally 4.7 µF ceramic) is used to slow down the output voltage ramp rate during startup along with filtering internal device noise. Capacitor values less than 4.7 µF will result in marginally higher output noise. There is internal fast start circuitry to enable reasonable soft start times. Additionally, a resistor from SS_SET to GND sets the output voltage. During nominal operation, 100 µA is output on this pin and a resistor from SS_SET to GND sets the output voltage.
20	STAB	I/O	Stability pin. This is an output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Use a series capacitor (C_{COMP}) and resistor (R_{COMP}) of 4.7 nF and 5 kΩ to compensate the device. For different compensation options, see the manufacturer's datasheet. A C0G (NP0) type ceramic dielectric capacitor capable of withstanding the lower of V_{BIAS} or 7.5 V is recommended (for example, a 25 V rated caFBpacitor). See NOTE.
21, 22, 23	OUT	O	Output power pin. The regulated output voltage. A single 220 Mf or two 100 Mf tantalum or tantalum polymer capacitors are recommended. See the manufacturer's datasheet for additional information.
24	NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{BIAS}.
25	OUTS	I	Output sense pin. This pin is used to sense the output voltage for regulation. Connect OUTS to the OUT pin at the desired point of regulation (remote sense).
26	FB_PG	I	Feedback and power good pin. The FB_PG pin enables setting of a configurable power good threshold. This is achieved by feeding the output voltage through a resistor divider to this pin (typical threshold of 300 Mv). When the threshold is reached, PG is asserted. Additionally, when the threshold on this pin is reached, start-up is over and the internal fast start circuitry is disabled. If this pin is connected directly to OUT, fast start operation ceases and PG is asserted as soon as V_{OUT} reaches 300 Mv (typical).
27, 28	NC	---	Output sense pin. This pin is used to sense the output voltage for regulation. Connect OUTS to the OUT pin at the desired point of regulation (remote sense).

NOTE: Reference EIA standard RS-198: C0G, C = letter code meaning 0 temperature coefficient, 0 = temperature coefficient multiplier, and G = letter code. NP0 = Negative positive 0ppm/°C.

FIGURE 2. Terminal connections – continued.

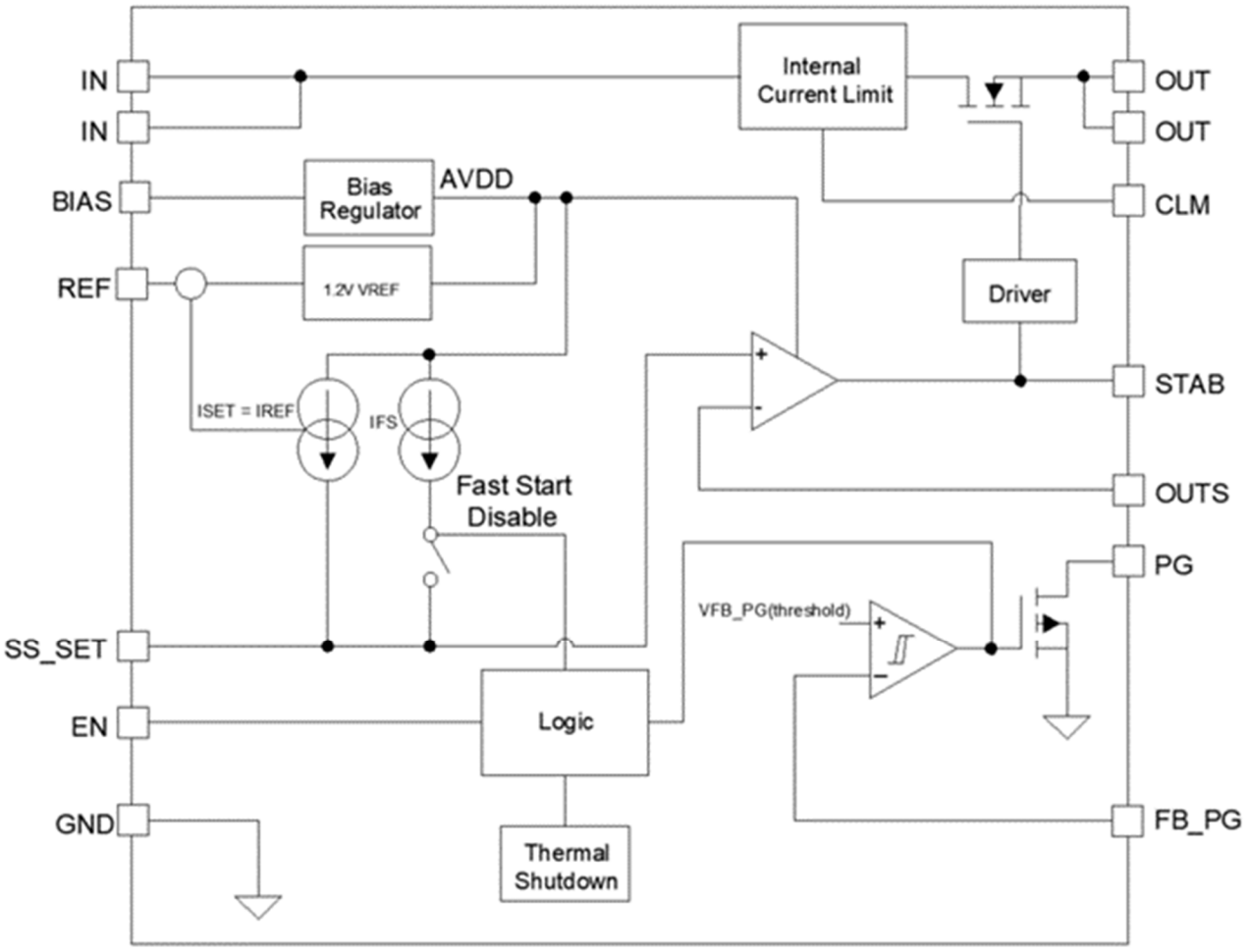
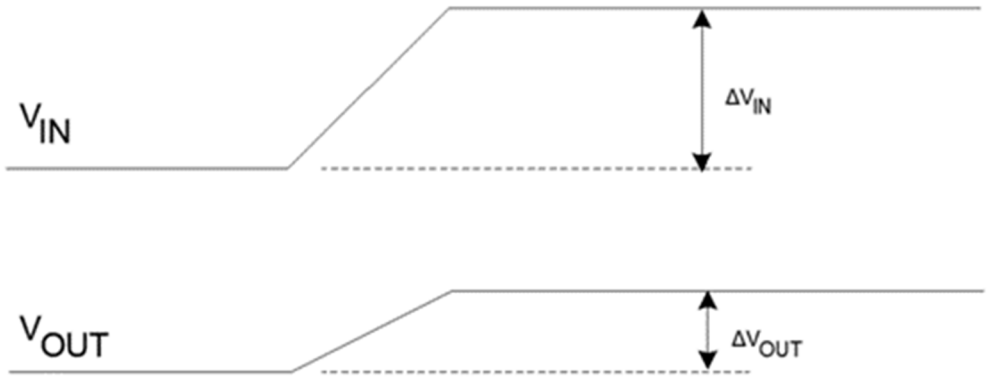
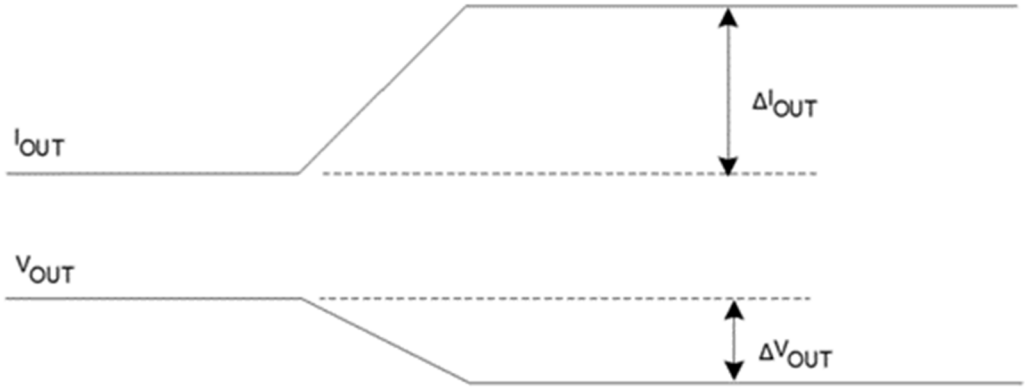


FIGURE 3. Block diagram.



NOTE: $\Delta V_{OUT}/\Delta V_{IN}$ = 3 µV/V. This means for a 1 V change in V_{IN} (ΔV_{IN} = 1 V), there will be a 3 µV change in ΔV_{OUT} (ΔV_{OUT} = 3 µV). Line regulation is a DC parameter; therefore this waveform should only be considered valid after transients die out or for a slow V_{IN} slew rate.

FIGURE 4. Line regulation.



NOTE: $\Delta V_{OUT}/\Delta I_{OUT}$ = 500 µV/V. This means for a 1 A change in I_{OUT} (ΔI_{OUT} = 1 A), there will be a 500 µV change in ΔV_{OUT} (ΔV_{OUT} = 500 µV). Load regulation is a DC parameter; therefore this waveform should only be considered valid after transients die out or for a slow I_{OUT} slew rate.

FIGURE 5. Load regulation.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

Marking for case outline Y:
If any additional information is needed, contact the manufacturer.

```
+------------------+        \T/ = TI LOGO
! \T/YMLLLLSG4     !         YM = YEAR MONTH DATE CODE
! R2120302P        !       LLLL = ASSY LOT CODE
! O  Q MLA  NNNN   !          S = ASSEMBLY SITE CODE PER QSS 005-120
+------------------+       NNNN = Simple sequence decimal serialization
  O - PIN 1 (DIMPLE)      LINE 1 MAXIMUM IS 9 CHARACTERS
                     NOTE: G4     MUST BE SYMBOLIZED
                                  WITH AN UNDERSCORE, IF PRESENT
```

3.5.1 Certification/compliance mark. The certification mark for device classes N, P, Q, Y, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, P, Q, Y, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, P, Q, Y, and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, P, Q, Y and V.

a. Test condition A, B, C and D. Burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Unless otherwise specified in the QM plan, for devices class N, P, Q, Y, and V, dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

c. For devices class P, Y, and V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

4.3 Qualification inspection. Qualification inspection for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, tableIII)				
	Device class N	Device class P	Device class Q	Device class V	Device class Y
Interim (pre burn-in) electrical parameters, (see 4.2)	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9,10, 11
Post burn-in electrical parameters (see 4.2.1)	1,2,3,9,10, 1/ 11	1,2,3,9, 1/ 2/ 10,11	1,2,3,9,10,11 1/	1,2,3,9, 1/ 2/ 10,11	1,2,3,9, 1/ 10,11
Group A (Final electrical) test requirements (see 4.4.1)	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9,10,11	1,2,3,9, 10,11
Group C end-point electrical parameters (see 4.4.2)	1,2,3,9,10,11	1,2,3,9, 2/ 10,11	1,2,3,9,10,11	1,2,3,9,10, 2/ 11	1,2,3,9, 10,11
Group D end-point electrical parameters (see 4.4.3)	1,9	1,9	1,9	1,9	1,9
Group E end-point electrical parameters (see 4.4.4)	1,9	1,9	1,9	1,9	1,9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in Table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. 1/ 2/ 3/

Parameters	Symbol	Device type	Delta limits	Units
Quiescent current	I_{Q_IN}	01, 02	±3	mA
Bias current with no output load	I_{Q_BIAS}	01, 02	±3	mA
Reference voltage	V_{REF}	01, 02	±0.007	V

1/ 240 hour burn in and group C end point electrical parameters.
Deltas are performed at T_A = +25°C.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in electrical limit.
3/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall correspond to the test defined in TABLE I (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table I.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. Preconditioning shall be performed on non-hermetic device classes N, P, and Y surface mount devices as specified in the manufacturer's QM plan. Thermal shock is not applicable to class N, P, and organic class Y.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. RHA levels for device classes N, P, Q, Y, and V, shall be as specified in MIL-PRF-38535 and the end-point electrical parameters subgroups shall be as specified in table IIA herein.

b. For device classes N, P, Q, Y, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 conditions A and D , and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C ±10°C for single event upset testing and at the maximum rated operating temperature ±10°C for single event upset testing.

f. Bias conditions shall be defined by the manufacturer for latch-up measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

4.4.4.3 Neutron /Displacement damaged dosimetry testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at TA = +25°C ±5°C after an exposure of 1 x 10^{13} neutrons/cm^2 (minimum).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply. Sources of supply for device classes N, P, Q, Y, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-12-15

Approved sources of supply for SMD 5962-21203 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R2120301VXC	01295	TPS7H1111-SP
5962R2120302PYE	01295	TPS7H1111-SP(QMLP)

1/ The lead finish shown for each PIN is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243