REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21													
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RAJESH PITHADIA

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
JAMES R. ESCHMEYER

DRAWING APPROVAL DATE
21-08-31

REVISION LEVEL

MICROCIRCUIT, LINEAR, SYNCHRONOUS STEP DOWN CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-20210**

SHEET 1 OF 21

DSCC FORM 2233
APR 97

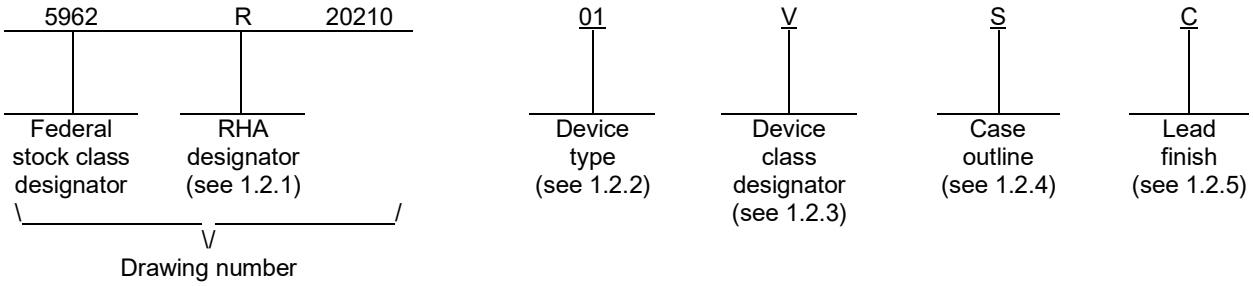
5962-E515-21

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H4002-SP	Radiation hardened, 3 V to 5.5 V input, 3 A, synchronous step down converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
S	CDFP3-F20	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Input voltage:
- Input voltage (V_{IN}) ..... -0.3 V to 7.5 V
- Power input voltage (PV_{IN}) ..... -0.3 V to 7.5 V
- Enable (EN) ..... -0.3 V to 5.5 V
- Sense voltage (V_{SENSE}) ..... -0.3 V to 3.3 V
- Compensation (COMP) ..... -0.3 V to 3.3 V
- Power good fault (PWRGD) ..... -0.3 V to 5.5 V
- Slow start and tracking (SS/TR) ..... -0.3 V to 5.5 V
- Resistor pin (RT) ..... -0.3 V to 5.5 V
- Synchronization (SYNC) ..... -0.3 V to 7.5 V

Output voltage:
- REFCAP ..... -0.3 V to 3.3 V
- Switch phase node (PH) ..... -1 V to 7.5 V
- Switch phase node (PH) 10 ns transient ..... -3 V to 7.5 V

Differential voltage (V_{diff}), GND to exposed thermal pad ..... -0.2 V to 0.2 V

Source current:
- PH ..... Current limit in amps
- RT ..... ±100 μA

Sink current:
- PH ..... Current limits in amps
- PV_{IN} ..... Current limits in amps
- COMP ..... ±200 μA
- PWRGD ..... -0.1 mA to 5 mA

Electrostatic discharge (ESD):
- Human-body model (HBM) ..... ±750 V 2/
- Charged-device model (CDM)..... ±1000 V 3/

Storage temperature ..... -65°C to +150°C

Operating temperature ($T_A = T_J$) ..... -55°C to +150°C

1.4 Recommended operating conditions.

Input voltage (V_{IN}) ..... 3 V to 5.5 V

Power input voltage (P_{VIN}) : ..... 3 V to 5.5 V

Operating temperature ($T_A = T_J$) ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (high dose rate = 50-300 rad(Si)/s) ..... 100 krads(Si) 4/ 5/

Maximum total dose available (low dose rate = 10 mrad(Si)/s) ..... 100 krads(Si) 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

3/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krad(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krads(Si).

5/ Device type 01 also irradiated extended room temperature anneal 168 hours per MIL-STD-883, method 1019, condition A, section 3.11.2 and observed devices electrical parametric limit bounce back to specification limit after 168 hours annealing.

1.6 Thermal characteristics.

Thermal resistance, junction to ambient (θ_{JA})	25°C/W
Thermal resistance, junction to case $(\theta_{JC})_{TOP}$	7.5°C/W
Thermal resistance, junction to case $(\theta_{JC})_{BOT}$	0.57°C/W
Thermal resistance, junction to board (θ_{JB})	8.3°C/W
Characterization parameter, junction-to-top (Ψ_{JT})	1.6°C/W
Characterization parameter, junction-to-board (Ψ_{JB})	8.2°C/W

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP155 – Recommended ESD Target Levels for HBM/MM Qualification.

JEP157 – Recommended ESD-CDM Target Levels.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply voltage (V_{IN} and PV_{IN} pins)							
PV_{IN} operating input voltage			1, 2, 3	01	3.0	5.5	V
V_{IN} operating input voltage			1, 2, 3	01	3.0	5.5	V
V_{IN} internal UVLO threshold		V_{IN} rising	1, 2, 3	01		3.0	V
V_{IN} shutdown supply current		V_{EN} = 0 V	1, 2, 3	01		3.0	mA
V_{IN} operating – non switching supply current		$V_{SENSE} = V_{BG}$	1, 2, 3	01		5.0	mA
Enable and UVLO (EN pin)							
Enable threshold		Rising	1, 2, 3	01		1.18	V
		Falling			1.05		
Voltage reference							
Voltage reference		0 A ≤ I_{OUT} ≤ 3 A,	3	01	0.795	0.817	V
			1		0.796	0.818	
			2		0.797	0.819	
Error amplifier							
Error amplifier transconductance 4/	$G_{(m)}$	-2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V	9, 10, 11	01	900	1900	µs
Error amplifier source current 4/		$V_{(COMP)}$ = 1 V, 100 mV input overdrive	1, 2, 3	01	85	185	µA
Error amplifier sink current 4/		$V_{(COMP)}$ = 1 V, 100 mV input overdrive	1, 2, 3	01	85	185	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal switching frequency							
Internally set frequency		R_T = Open	4, 5, 6	01	395	585	kHz
Externally set frequency		R_T = 100 kΩ (1%)	4, 5, 6	01	395	585	kHz
		R_T = 487 kΩ (1%)	4, 5, 6		80	115	
		R_T = 47 kΩ (1%)	4, 5, 6		900	1100	
External synchronization							
SYNC out low-to-high rise time (10%/90%)		C_{LOAD} = 25 pF	9, 10, 11	01		130	ns
SYNC out high-to-low fall time (90%/10%)		C_{LOAD} = 25 pF	9. 10. 11	01		15.5	ns
SYNC out high level threshold		I_{OH} = 50 µA	1, 2, 3	01	V_{IN} – 0.3		V
SYNC out low level threshold		I_{OH} = 50 µA	1, 2, 3	01		600	mV
SYNC in low level threshold		$PV_{IN} = V_{IN}$ = 3.0 V	1, 2, 3	01		700	mV
SYNC in high level threshold		$PV_{IN} = V_{IN}$ = 3.0 V	1, 2, 3	01	2.45		V
SYNC in low level threshold		$PV_{IN} = V_{IN}$ = 5.5 V	1, 2, 3	01		700	mV
SYNC1 in high level threshold		$PV_{IN} = V_{IN}$ = 5.5 V	1, 2, 3	01	4.25		V
SYNC in frequency range 5/			4, 5, 6	01	100	1000	kHz
PH (PH pin)							
Minimum on time		Measured at 10% to 90% of V_{IN}, I_{PH} = 2 A	9, 10, 11	01		235	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Slow start and tracking (SS/TR pin)							
SS charge current			1, 2, 3	01	1.5	3.0	µA
SS/TR to V_{SENSE} matching		$V_{(SS/TR)}$ = 0.4 V	1, 2, 3	01		90	mV
Power good (PWRGD pin)							
Output high leakage		$V_{SENSE} = V_{REF}$, $V_{(PWRGD)}$ = 5 V	1, 2, 3	01		181	nA
Output low voltage		$I_{(PWRGD)}$ = 2 mA	1, 2, 3	01		0.3	V
Minimum V_{IN} for valid output		$V_{(PWRGD)}$ < 0.5 V at 100 µA	1, 2, 3	01		1.0	V
Minimum SS/TR voltage for PWRGD			1, 2, 3	01		1.55	V

1/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krad(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krads(Si).

2/ Unless otherwise specified, $V_{IN} = PV_{IN}$ = 3.0 V to 5.5 V.

3/ For production testing of these parameters to the limits in Table I herein, ambient temperature (T_A) equals junction temperature (T_J).

4/ Ensured by design only. Not tested in production.

5/ Parameter is production tested at nominal voltage with $V_{IN} = P_{VIN}$ = 5 V.

Device types	01
Case outline	X
Terminal number	Terminal symbol
1	GND
2	EN
3	RT
4	SYNC
5	V_{IN}
6	PV_{IN}
7	PV_{IN}
8	PGND
9	PGND
10	PGND
11	PH
12	PH
13	PH
14	PH
15	PH
16	REFCAP
17	V_{SENSE}
18	COMP
19	SS/TR
20	PWRGND

FIGURE 1. Terminal connections.

Terminal symbol	I/O	Description
GND	---	Return for control circuitry. See note 1.
EN	I	Enable pin. EN pin is internally pulled up allowing for the pin to be floated to enable the device. Adjust the input undervoltage lockout (UVLO) with two resistors.
RT	I/O	In internal oscillation mode, a resistor is connected between the RT pin and GND to set the switching frequency. Leaving this pin floating sets the internal switching frequency to 500 kHz.
SYNC	I/O	Optional 100 kHz to 1 MHz external system clock input.
V_{IN}	I	Input power for the control circuitry of the switching regulator.
PV_{IN}	I	Input power for the output stage of the switching regulator.
PGND	---	Return for low side power MOSFET.
PH	O	Switch phase node.
REFCAP	O	Required 470 nF external capacitor for internal reference.
V_{SENSE}	I	Inverting input of the transconductance (gm) error amplifier.
COMP	I/O	Error amplifier output and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	I/O	Slow start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
PWRGD	O	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during slow start.

Note:
1. GND (pin 1, analog ground) must be connected to PGND external to the package. Thermal pad must be connected to a heat dissipating layer. Thermal pad is internally connected to the seal ring and GND.

FIGURE 2. Terminal connections – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 9,10,11
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/ 9,10,11	1,2,3,4,5,6 1/ 2/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 2/ 9,10,11
Group D end-point electrical parameters (see 4.4)	1,4	1,4
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in Table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. 1/

Parameter	Device Type	Delta limits	Units
V_{IN} shutdown supply current	01	±0.59	mA
V_{IN} operating non-switching supply current	01	±1.0	mA

1/ 240 hour burn in and group C end point electrical parameters.
Deltas are performed at T_A = +25°C.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D for device type 01 and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

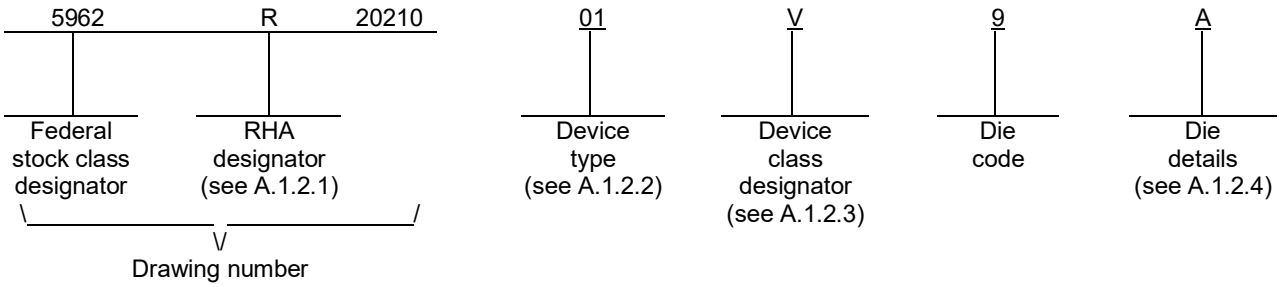
6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-20210

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H4002-SP	Radiation hardened, 3 V to 7 V input, 3 A, synchronous step down converter

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraph 4.4.4, 4.4.4.1, and 4.4.4.1.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime VA and have agreed to this drawing.

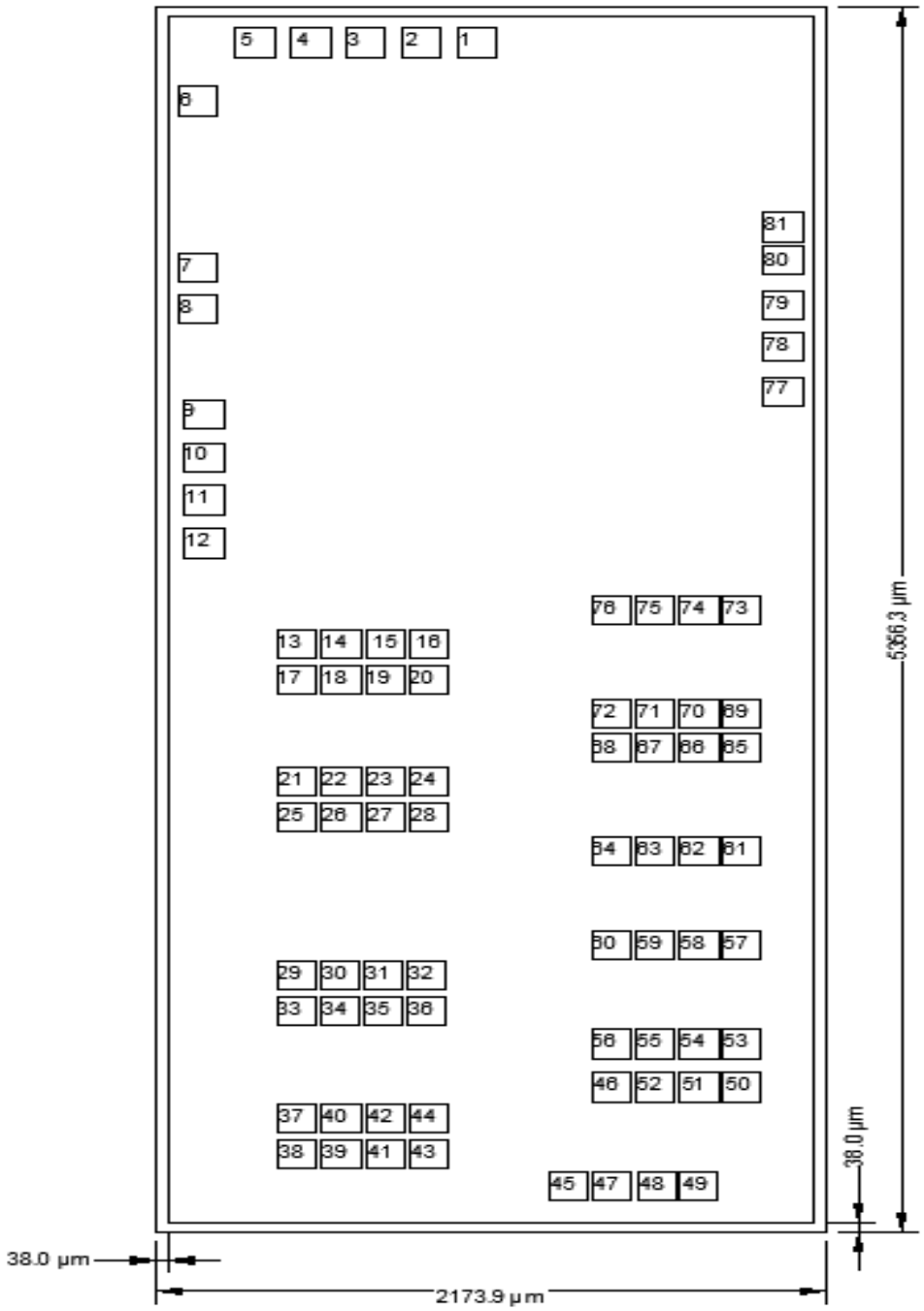


FIGURE A-1. Die bonding pad locations and electrical functions.

Description	Pad number	X MIN (µm)	Y MIN (µm)	X MAX (µm)	Y MAX (µm)
AV_{SS}	1	938.16	5098.41	1064.16	5224.41
AV_{SS}	2	759.06	5098.41	885.06	5224.41
N/C	3	579.96	5098.41	705.96	5224.41
AV_{SS}	4	400.86	5098.41	526.86	5224.41
AV_{SS}	5	221.76	5098.41	347.76	5224.41
EN	6	38.7	4843.98	164.7	4969.98
RT	7	38.7	4115.43	164.7	4241.43
SYNC	8	38.7	3936.33	164.7	4062.33
V_{IN}	9	55.89	3473.865	181.89	3599.865
V_{IN}	10	55.89	3285.765	181.89	3411.765
V_{IN}	11	55.89	3097.665	181.89	3223.665
V_{IN}	12	55.89	2909.565	181.89	3035.565
PV_{IN}	13	360.045	2468.025	486.045	2594.025
PV_{IN}	14	500.805	2468.025	626.805	2594.025
PV_{IN}	15	643.905	2468.025	769.905	2594.025
PV_{IN}	16	782.505	2468.025	908.505	2594.025
PV_{IN}	17	360.045	2312.595	486.045	2438.595
PV_{IN}	18	500.805	2312.595	626.805	2438.595
PV_{IN}	19	643.905	2312.595	769.905	2438.595
PV_{IN}	20	782.505	2312.595	908.505	2438.595
PV_{IN}	21	360.045	1868.265	486.045	1994.265
PV_{IN}	22	500.805	1868.265	626.805	1994.265
PV_{IN}	23	643.905	1868.265	769.905	1994.265
PV_{IN}	24	782.505	1868.265	908.505	1994.265
PV_{IN}	25	360.045	1712.835	486.045	1838.835
PV_{IN}	26	500.805	1712.835	626.805	1838.835
PV_{IN}	27	643.905	1712.835	769.905	1838.835
PV_{IN}	28	782.505	1712.835	908.505	1838.835
PGND	29	360	1004.625	486	1130.625
PGND	30	498.6	1004.625	624.6	1130.625
PGND	31	637.2	1004.625	763.2	1130.625
PGND	32	775.8	1004.625	901.8	1130.625
PGND	33	360	863.955	486	989.955
PGND	34	498.6	863.955	624.6	989.955
PGND	35	637.2	863.955	763.2	989.955
PGND	36	775.8	863.955	901.8	989.955
PGND	37	360	384.525	486	510.525
PGND	38	360	243.855	486	369.855

FIGURE A-1. Die bonding pad locations and electrical functions – continued.

Description	Pad number	X MIN (µm)	Y MIN (µm)	X MAX (µm)	Y MAX (µm)
PGND	39	503.1	243.855	629.1	369.855
PGND	40	503.1	384.525	629.1	510.525
PGND	41	641.7	243.855	767.7	369.855
PGND	42	641.7	384.525	767.7	510.525
PGND	43	775.8	243.855	901.8	369.855
PGND	44	775.8	384.525	901.8	510.525
PH	45	1239.66	97.425	1365.66	223.425
PH	46	1374.66	529.965	1500.66	655.965
PH	47	1378.26	97.425	1504.26	223.425
PH	48	1516.86	97.425	1642.86	223.425
PH	49	1657.26	97.425	1783.26	223.425
PH	50	1790.46	529.965	1916.46	655.965
PH	51	1651.86	529.965	1777.86	655.965
PH	52	1513.26	529.965	1639.26	655.965
PH	53	1790.46	718.515	1916.46	844.515
PH	54	1651.86	718.515	1777.86	844.515
PH	55	1513.26	718.515	1639.26	844.515
PH	56	1374.66	718.515	1500.66	844.515
PH	57	1790.46	1150.065	1916.46	1276.065
PH	58	1651.86	1150.065	1777.86	1276.065
PH	59	1513.26	1150.065	1639.26	1276.065
PH	60	1374.66	1150.065	1500.66	1276.065
PH	61	1795.365	1565.1	1921.365	1691.1
PH	62	1655.865	1565.1	1781.865	1691.1
PH	63	1515.465	1565.1	1641.465	1691.1
PH	64	1376.865	1565.1	1502.865	1691.1
PH	65	1795.365	2016	1921.365	2142
PH	66	1655.865	2016	1781.865	2142
PH	67	1515.465	2016	1641.465	2142
PH	68	1376.865	2016	1502.865	2142
PH	69	1795.365	2164.86	1921.365	2290.86
PH	70	1655.865	2164.86	1781.865	2290.86
PH	71	1515.465	2164.86	1641.465	2290.86
PH	72	1376.865	2164.86	1502.865	2290.86
PH	73	1795.365	2615.76	1921.365	2741.76
PH	74	1655.865	2615.76	1781.865	2741.76
PH	75	1515.465	2615.76	1641.465	2741.76
PH	76	1376.865	2615.76	1502.865	2741.76
REFCAP_NU	77	1933.245	3572.46	2059.245	3698.46
V_{SENSE}	78	1933.245	3770.415	2059.245	3896.415
COMP	79	1933.245	3949.515	2059.245	4075.515
SS	80	1933.2	4149.135	2059.2	4275.135
PWRGND	81	1933.2	4292.325	2059.2	4418.325

FIGURE A-1. Die bonding pad locations and electrical functions – continued.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 2174 µm x 5358 µm
Die thickness: 15 mils

Interface materials.
Top metallization: AlCu
Backside metallization: Silicon with backgrind

Glassivation.
Type: Compressed Oxy-Nitride

Substrate: P <100> 0.4D, 0.014 - 0.02 Ω-cm
Assembly related information.
Substrate potential: Gnd
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-08-31

Approved sources of supply for SMD 5962-20210 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R2021001VSC	01295	TPS7H4002-RHA
5962R2021001V9A	01295	TPS7H4002-RHA-KGD

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243