

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	VEN added device 02. Update to Section 508 Compliance and current MIL-PRF-38535 requirements. - rep	23-10-26	James Eschmeyer



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

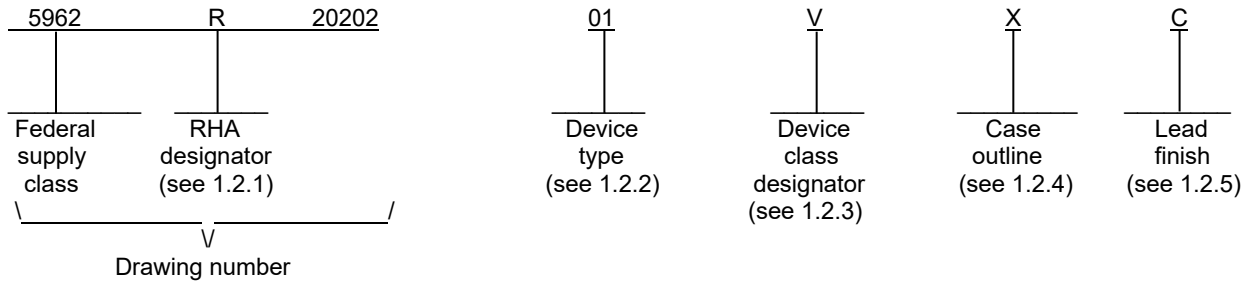
REV	A	A	A	A	A	A	A	A															
SHEET	23	24	25	26	27	28	29	30															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

PMIC N/A		PREPARED BY Laura Leeper Branham		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE		CHECKED BY Laura Leeper Branham				
		APPROVED BY James R. Eschmeyer				
		DRAWING APPROVAL DATE 20-04-10				
AMSC N/A		REVISION LEVEL A		SIZE A	CAGE CODE 67268	5962-20202
				SHEET	1 OF 30	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Data retention</u>	<u>Access time</u>
01	1061G30	1M X 16-bit Radiation-Hardened SRAM	Yes	10 ns
02	1069G30	2M X 8-bit Radiation-Hardened SRAM	Yes	10 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	54	Ceramic TSOP
Y	See figure 1	36	Ceramic Flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V _{DD}).....	-0.5 V dc to +6.0 V dc
DC input voltage.....	-0.5 V dc to V _{DD} + 0.5 V dc
Voltage range on any output pin.....	-0.5 V dc to V _{DD} + 0.5 V dc
Storage temperature range.....	-65°C to +150°C
Case temperature range, (T _C).....	-55°C to +125°C
Junction temperature (T _J).....	+150°C <u>2/</u>
Lead temperature (soldering, 10 seconds).....	+260°C
Thermal resistance, junction-to-case (θ _{JC}):	
Case X (device 01).....	3.38°C/W <u>3/</u>
Case Y (device 02).....	3.6°C/W <u>3/</u>
Maximum power dissipation (P _D).....	0.88 W
Maximum operating frequency (F _{MAX}).....	100 MHz
Current into output (Low).....	20 mA

1.4 Recommended operating conditions.

Supply voltage range (V _{DD}).....	3.0 V dc to 3.6 V dc
Supply voltage (V _{SS}).....	0 V
Input high voltage range (V _{IH}).....	2.0 V dc to V _{DD} + 0.3 V dc
Input low voltage range (V _{IL}).....	-0.3 V dc to +0.8 V dc
Case operating temperature range (T _C).....	-55°C to +125°C
Slew rate (All inputs, 90% - 10%).....	1 V/ns

1.5 Radiation features.

Maximum total ionizing dose (TID) available:	
High dose rate = 50-300 rad(Si)/s.....	100 krads(Si) <u>4/</u>
Low dose rate = 5.98 mrad(Si)/s.....	100 krads(Si) <u>4/</u>
Single event phenomenon (SEP):	
No SEL occurs at normal incident LET(see 4.4.4.4).....	≤ 60 MeV-cm ² /mg <u>5/</u>
SEU observed at on set LET (see 4.4.4.4).....	≤ 1.3 MeV-cm ² /mg <u>5/</u>
(Single event upset rate = 3.17 x 10 ⁻¹² errors/bit-day)	
Dose rate induced upset.....	3.0 x 10 ⁸ rad(Si)/sec <u>5/</u>
Dose rate induced latch-up survivability.....	5.0 x 10 ¹⁰ rad(Si)/sec <u>6/</u>
Neutron irradiation.....	1.5 x 10 ¹¹ n/cm ² <u>6/</u>

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
- 3/ Tested initially and after any design or process changes that may affect these parameters.
- 4/ Device types 01 and 02 have been tested for total ionizing dose (TID) in accordance with MIL-STD-883, method 1019, condition A and D to a maximum total ionizing dose (TID) level of 200 krads(Si) and 100 krads(Si) respectively. However, device types 01 and 02 are marked to standard 100 krads(Si) of RHA TID level R.
- 5/ Heavy ion single event effect (SEE) test was performed at Texas A&M University Cyclotron facility and observed no single event latch-up (SEL) occurs at normal incident angles LET= 60 MeV/(mg/cm²) at 95°C. However, this device observed SEL at LET= 60 MeV/(mg/cm²) at 98°C with fluence level 8x10⁶ ions/cm². For more information on SEE test please contact the device manufacturer.
- 6/ Manufacturer also performed Dose rate induced latch-up survivability and Neutron irradiation (Displacement damage) test. For more information on these tests please contact the device manufacturer.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at [https://quicksearch.dla.mil/.](https://quicksearch.dla.mil/))

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at [https://www.astm.org.](https://www.astm.org))

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at [https://www.jedec.org.](https://www.jedec.org))

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in Table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table IIA. The electrical tests for each subgroup are defined in Table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C 3.0 V ≤ V _{DD} ≤ 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output HIGH Voltage	V _{OH}	V _{DD} = Min., I _{OH} = -4.0 mA	1, 2, 3	All	2.4		V
Output LOW Voltage	V _{OL}	V _{DD} = Min., I _{OL} = 8.0 mA	1, 2, 3	All		0.4	V
Input Leakage Current	I _{LK}	GND ≤ V _I ≤ V _{DD}	1, 2, 3	All	-5	+5	μA
Output Leakage Current	I _{OLK}	GND ≤ V _{OUT} ≤ V _{DD} , Output Disabled	1, 2, 3	All	-5	+5	μA
V _{DD} Operating Supply Current	I _{DD}	V _{DD} = Max. f = f _{MAX} = 1/t _{RC}	1, 2, 3	All		160	mA
Automatic CE Power Down Current – TTL Inputs	I _{SB1}	Max. V _{DD} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} , or V _{IN} ≤ V _{IL} , f = f _{MAX}	1, 2, 3	All		60	mA
Automatic CE Power Down Current – CMOS Inputs	I _{SB2}	Max. V _{DD} , $\overline{CE} \geq V_{DD} - 0.3V$, V _{IN} ≥ V _{DD} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	1, 2, 3	All		50	mA
Input capacitance <u>4/</u>	C _{IN}	T _A = 25°C, f = 1 MHz, V _{DD} = 3.3 V	4	All		10	pF
Input / Output Capacitance <u>4/</u>	C _{OUT}	T _A = 25°C, f = 1 MHz, V _{DD} = 3.3 V	4	All		10	pF
Functional tests		See 4.4.1c, T _C = 25°C	7, 8A, 8B	All			
V _{DD} for Data Retention	V _{DR}	<u>5/</u>	1, 2, 3	All	1.0		V
Data Retention Current	I _{DDDR}	V _{DD} = V _{DR} = 2.0 V, $\overline{CE} \geq V_{DD} - 0.3 V$, V _{IN} ≥ V _{DD} - 0.3 V, or V _{IN} ≤ 0.3 V <u>5/</u>	1, 2, 3	All		50	mA
Read Cycle Time	t _{RC}	See figure 5 as applicable	9, 10, 11	All	10		ns
Address to Data Valid	t _{AA}		9, 10, 11	All		10	ns
Data Hold from Address Change	t _{OHA}		9, 10, 11	All	3		ns
\overline{CE} LOW to Data Valid	t _{ACE}		9, 10, 11	All		10	ns
\overline{OE} LOW to Data Valid	t _{DOE}		9, 10, 11	All		5	ns
\overline{OE} LOW to Low Z <u>6/ 7/</u>	t _{LZOE}		9, 10, 11	All	0		ns
\overline{OE} HIGH to High Z <u>6/ 7/ 8/</u>	t _{HZOE}		9, 10, 11	All		5	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C 3.0 V ≤ V _{DD} ≤ 3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
\overline{CE} LOW to Low Z <u>6/ 7/</u>	t _{LZCE}	See figure 5 as applicable	9, 10, 11	All	3		ns
\overline{CE} HIGH to High Z <u>6/ 7/ 8/</u>	t _{HZCE}		9, 10, 11	All		5	ns
Write Cycle Time <u>9/ 10/</u>	t _{WC}		9, 10, 11	All	10		ns
\overline{CE} LOW to Write End	t _{SCE}		9, 10, 11	All	7		ns
Address Set-Up to Write End	t _{AW}		9, 10, 11	All	7		ns
Address Hold from Write End	t _{HA}		9, 10, 11	All	0		ns
Address Set-Up from Write Start	t _{SA}		9, 10, 11	All	0		ns
\overline{WE} Pulse Width	t _{PWE}		9, 10, 11	All	7		ns
Data Set-Up to Write End	t _{SD}		9, 10, 11	All	5		ns
Data Hold from Write End	t _{HD}		9, 10, 11	All	0		ns
\overline{WE} HIGH to Low Z <u>6/ 7/ 10/</u>	t _{LZWE}		9, 10, 11	All	3		ns
\overline{WE} LOW to High Z <u>6/ 7/ 8/</u>	t _{HZWE}		9, 10, 11	All		5	ns
Chip Deselect to Data Retention Time <u>4/ 7/</u>	t _{CDR}		See figure 5 as applicable V _{DD} = V _{DR} = 2.0 V, CE ≥ V _{DD} - 0.3 V, V _{IN} ≥ V _{DD} - 0.3 V, or V _{IN} < 0.3 V <u>2/ 3/ 4/</u>	9, 10, 11	All	0	
Operation Recovery Time <u>7/ 11/</u>	t _R	See figure 5 as applicable	9, 10, 11	All	t _{RC}		ns

- 1/ RHA parts supplied to this drawing have been characterized TID through all levels of M, D, P, L, R and F of irradiation in accordance with MIL-STD-883, method 1019, condition A and D to a maximum total ionizing dose (TID) level of 200 krad(Si) and 100 krad(Si) respectively. However, device type 01 is marked to standard 100 krad(Si) of RHA TID level R. Pre and post-irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
- 2/ AC characteristics (except High-Z) are tested using the load conditions shown in Circuit A of Figure 4. High-Z characteristics are tested for all speeds using the test load shown in Circuit B of Figure 4.
- 3/ Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- 4/ Tested initially and after any design or process changes that may affect these parameters.
- 5/ No input may exceed V_{CC} + 0.3 V.
- 6/ At a given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- 7/ Parameter, if not tested, shall be guaranteed to the limits specified in Table IA.
- 8/ t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with the load capacitance of 5 pF as in Circuit B of Figure 4. Transition is measured when outputs enter a high impedance state.
- 9/ The internal Write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- 10/ The minimum Write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.
- 11/ Full device operation requires linear V_{DD} ramp from V_{DR} to V_{DD(MIN)} ≥ 50 μs or stable at V_{DD(MIN)} ≥ 50 μs.

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Table IB. SEP test limits 1/ 2/

Device Type	Single Event Upset 3/ V _{DD} = 5.0 V		Single Event Latch-up (SEL) test Bias V _{DD} = 5.5V
	Single event upsets observed at Onset LET	Maximum device Cross section (cm ²)	Normal incident angle LET No SEL occurs 4/
<u>All</u>	1.3 MeV/(mg/cm ²)	7.0 x 10 ⁻⁸	60 MeV/(mg/cm ²)

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ For single event upset error rate = 3.17×10^{-12} errors/bit-day. For more information on SEE test please contact the device manufacturer.

4/ Heavy ion single event effect (SEE) test was performed at Texas A&M University Cyclotron facility and observed no single event latch-up(SEL) occurs at normal incident angles LET= 60 MeV/(mg/cm²) at 95°C. However, this device observed SEL at LET= 60 MeV/(mg/cm²) at 98°C with fluence level 8×10^6 ions/cm². For more information on SEE test please contact the device manufacturer.

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Case X

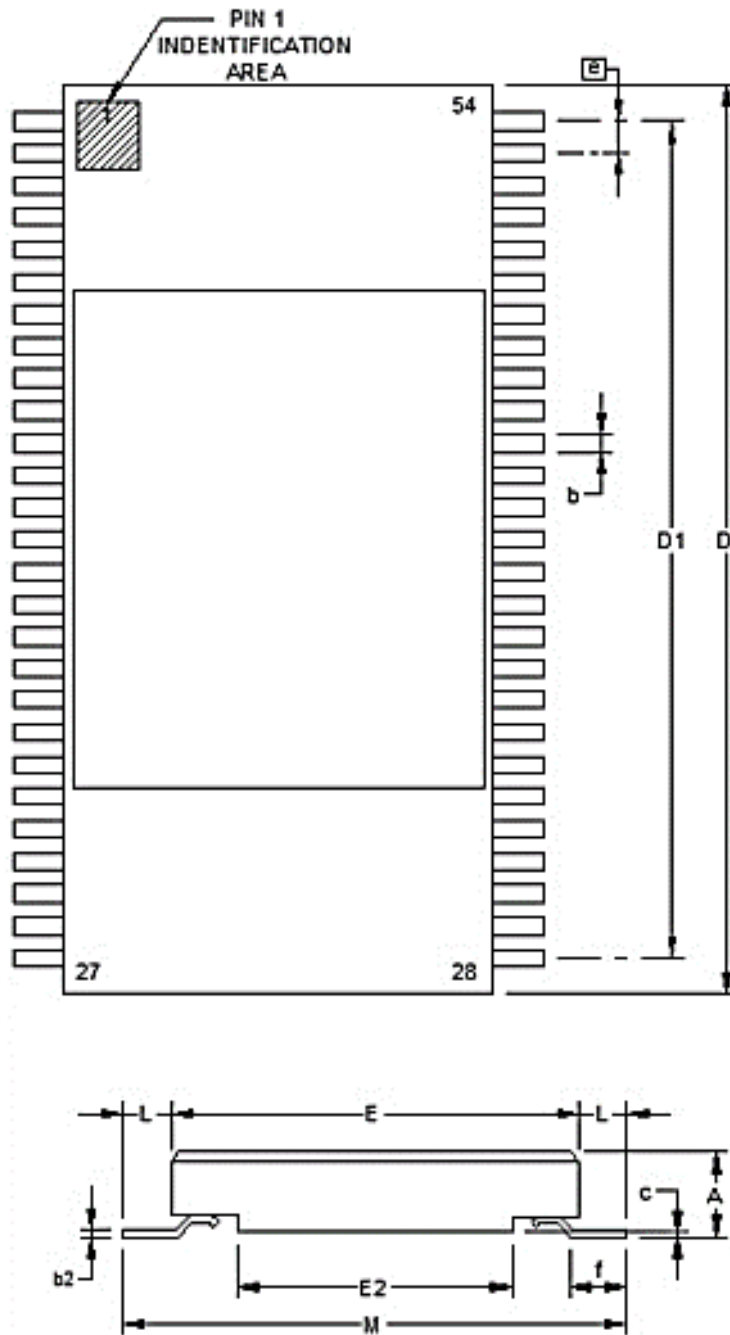


FIGURE 1. Case outlines.

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Case X

Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.416	3.038	0.095	0.120
b	0.3	0.4	0.012	0.016
b2	0.15	0.25	0.006	0.010
c	0.073	---	0.003	---
D	22.173	22.633	0.873	0.891
D1	20.60	21.00	0.811	0.827
E	11.636	12.036	0.458	0.474
E2	7.00	7.40	0.276	0.291
e	0.80 BSC		0.0315 BSC	
f	1.588	2.096	0.063	0.083
L	1.233 NOM (ref)		0.04854 NOM (ref)	
M	14.173	14.427	0.558	0.568
N	54		54	

NOTES:

1. Item was originally designed in millimeters.
2. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
3. The seal ring and lid are electrically connected to V_{ss}.
4. Lead finish is in accordance with MIL-PRF-38535.
5. Package material: opaque 90% minimum Alumina ceramic.

FIGURE 1. Case outlines – Continued.

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Case Y

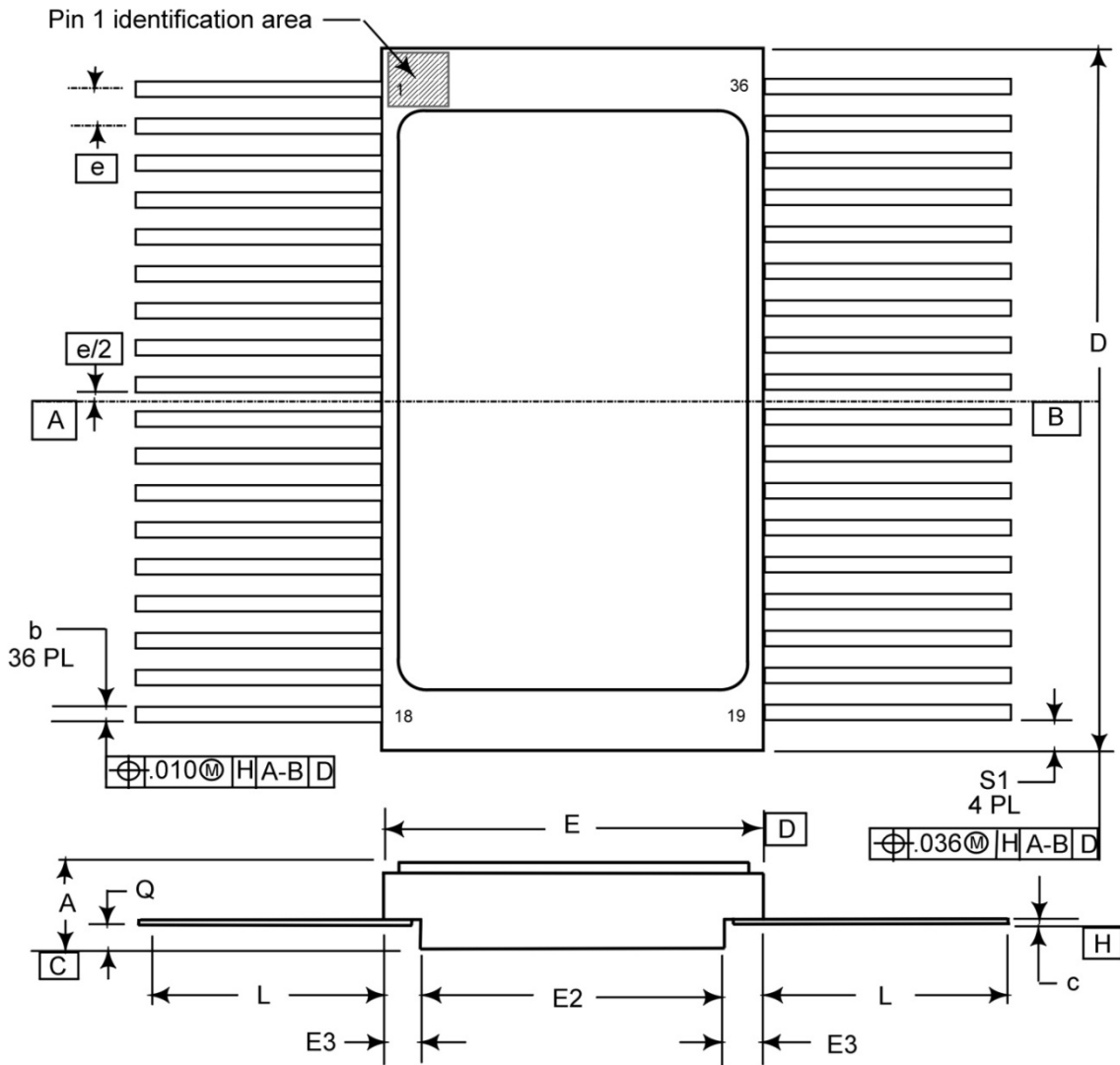


FIGURE 1. Case outlines – Continued.

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Case Y

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.40	2.99	0.094	0.118
b	0.38	0.48	0.015	0.019
c	0.102	0.152	0.004	0.006
D	23.12	23.62	0.910	0.930
E	11.99	12.39	0.472	0.488
E2	9.96	10.36	0.392	0.408
E3	0.082	1.22	0.003	0.048
e	1.19	1.35	0.047	0.053
L	10.19	10.64	0.401	0.419
Q	0.64	---	0.025	---
S1	0.13	---	0.51	---

NOTES:

1. Item was originally designed in millimeters.
2. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
3. The seal ring and lid are electrically connected to V_{ss}.
4. Lead finish is in accordance with MIL-PRF-38535.
5. Package material: opaque 90% minimum Alumina ceramic.

FIGURE 1. Case outlines – Continued.

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DEVICE TYPE 01

Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	I/O ₁₂	19	A ₁₇	37	A ₁₁
2	V _{CC}	20	A ₁₆	38	A ₁₀
3	I/O ₁₃	21	A ₁₅	39	$\overline{\text{BLE}}$
4	I/O ₁₄	22	I/O ₀	40	NC
5	V _{SS}	23	V _{CC}	41	V _{SS}
6	I/O ₁₅	24	I/O ₁	42	$\overline{\text{CE}}$
7	A ₄	25	I/O ₂	43	NC
8	A ₃	26	V _{SS}	44	A ₉
9	A ₂	27	I/O ₃	45	A ₈
10	A ₁	28	I/O ₄	46	A ₇
11	A ₀	29	V _{CC}	47	A ₆
12	$\overline{\text{BHE}}$	30	I/O ₅	48	A ₅
13	$\overline{\text{CE}}$	31	I/O ₆	49	I/O ₈
14	V _{CC}	32	V _{SS}	50	V _{CC}
15	$\overline{\text{WE}}$	33	I/O ₇	51	I/O ₉
16	CE ₂	34	A ₁₄	52	I/O ₁₀
17	A ₁₉	35	A ₁₃	53	V _{SS}
18	A ₁₈	36	A ₁₂	54	I/O ₁₁

NOTES:

1. NC pins are no connect and are not connected on the die.

DEVICE TYPE 02

Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	A ₀	19	A ₁₀
2	A ₁	20	A ₁₁
3	A ₂	21	A ₁₂
4	A ₃	22	A ₁₃
5	A ₄	23	A ₁₄
6	$\overline{\text{CE}}$	24	A ₁₅
7	I/O ₀	25	I/O ₄
8	I/O ₁	26	I/O ₅
9	V _{CC}	27	V _{CC}
10	V _{SS}	28	V _{SS}
11	I/O ₂	29	I/O ₆
12	I/O ₃	30	I/O ₇
13	$\overline{\text{WE}}$	31	$\overline{\text{OE}}$
14	A ₅	32	A ₁₆
15	A ₆	33	A ₁₇
16	A ₇	34	A ₁₈
17	A ₈	35	A ₁₉
18	A ₉	36	A ₂₀

FIGURE 2. Terminal connections.

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DEVICE TYPE 01								
\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O0 – I/O7	I/O8 – I/O15	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write all bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

DEVICE TYPE 02					
\overline{CE}	\overline{OE}	\overline{WE}	I/O0 – I/O7	Mode	Power
H	X	X	High-Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write all bits	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

FIGURE 3. Truth tables.

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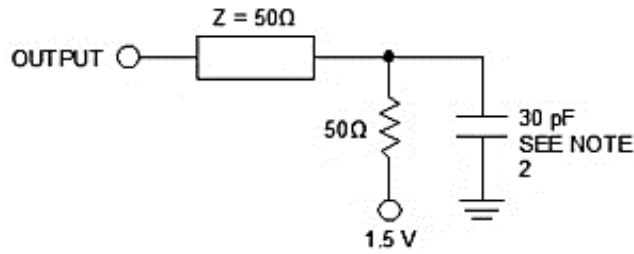
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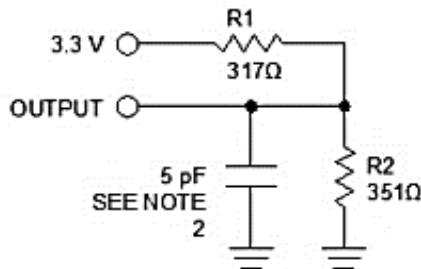
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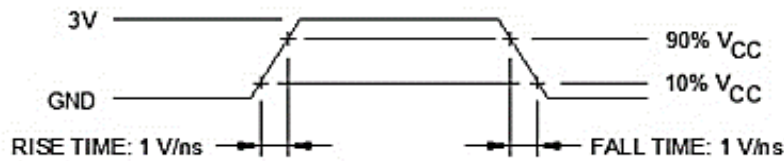


CIRCUIT A



CIRCUIT B

ALL INPUT PULSES



AC test conditions

Input pulse levels	V _{SS} to 3.0 V
Input rise, fall time	3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

NOTES:

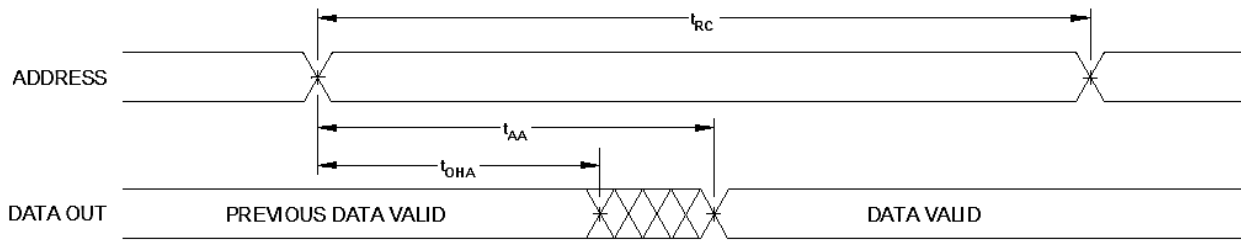
1. Use these output load circuits or equivalent for testing.
2. Including scope and jig.
3. Minimum of 5 pF for t_{HZCE}, t_{HZWE}, and t_{HZOE}.

FIGURE 4. Output load circuits.

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DEVICE TYPE 01

Read Cycle Number 1 (see notes 1 and 2 at end of Figure 5)



Read Cycle Number 2 (\overline{OE} controlled, see notes 2 and 3 at end of Figure 5)

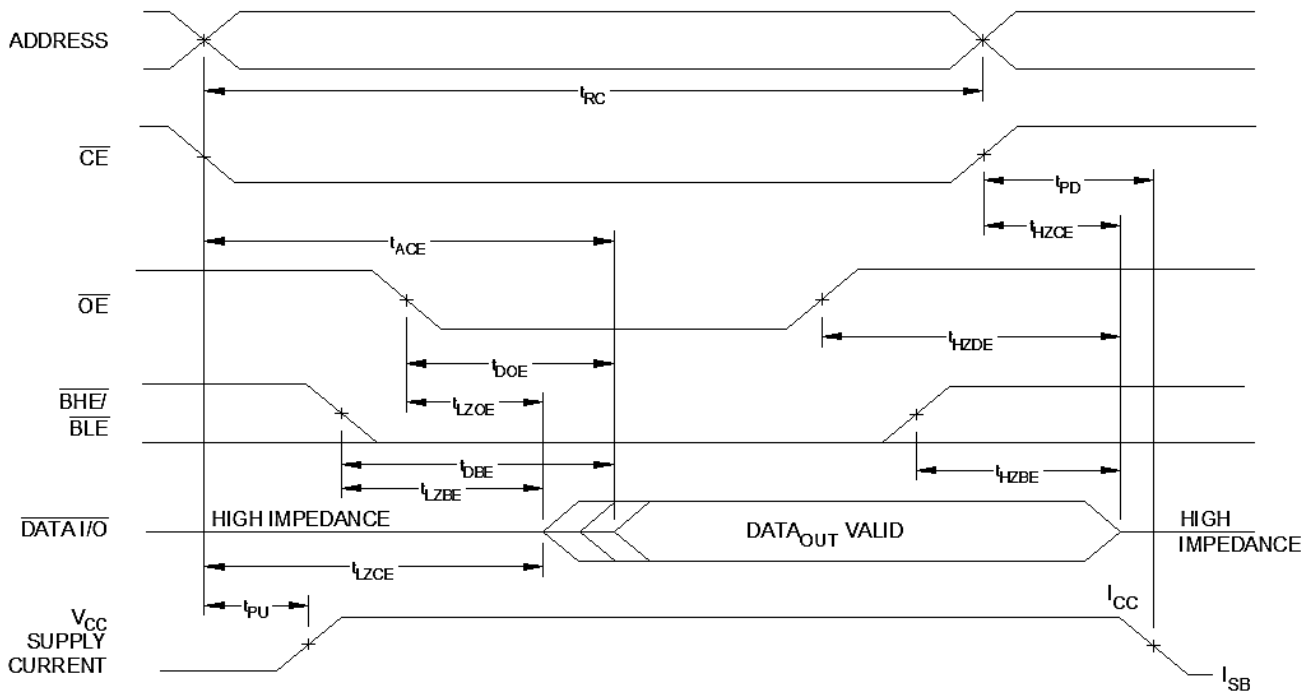


FIGURE 5. Timing waveforms.

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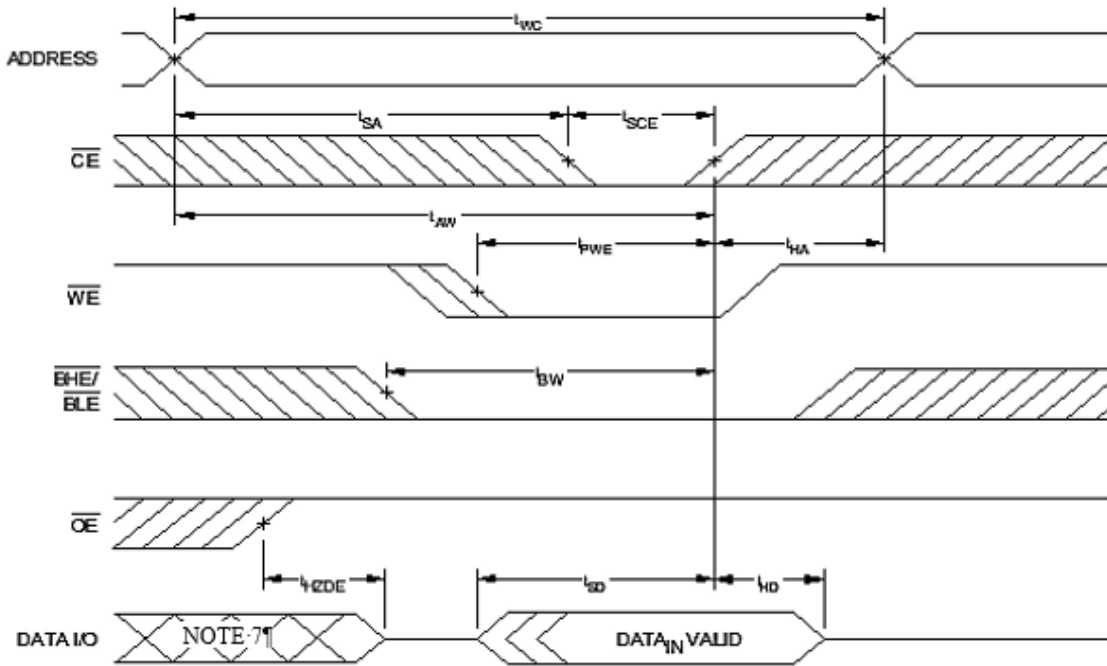
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SHEET **16**

DEVICE TYPE 01

Write Cycle Number 1 (\overline{CE} controlled, see notes 4 and 5 at end of Figure 5)



Write Cycle Number 2 (\overline{WE} controlled, \overline{OE} HIGH during write, see notes 4 and 5 at end of Figure 5)

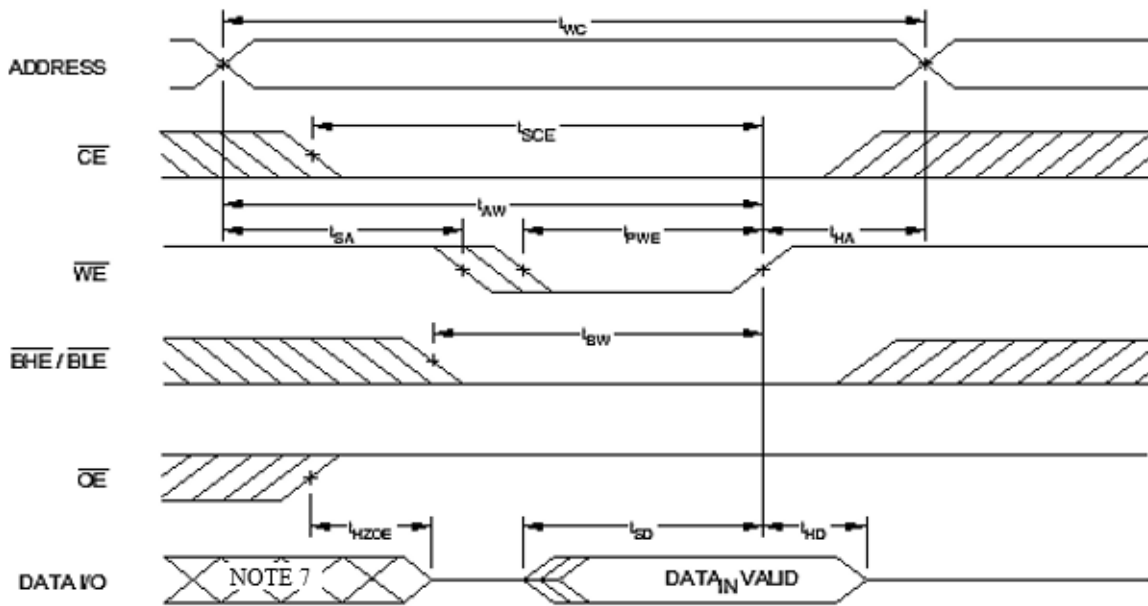


FIGURE 5. Timing waveforms – Continued.

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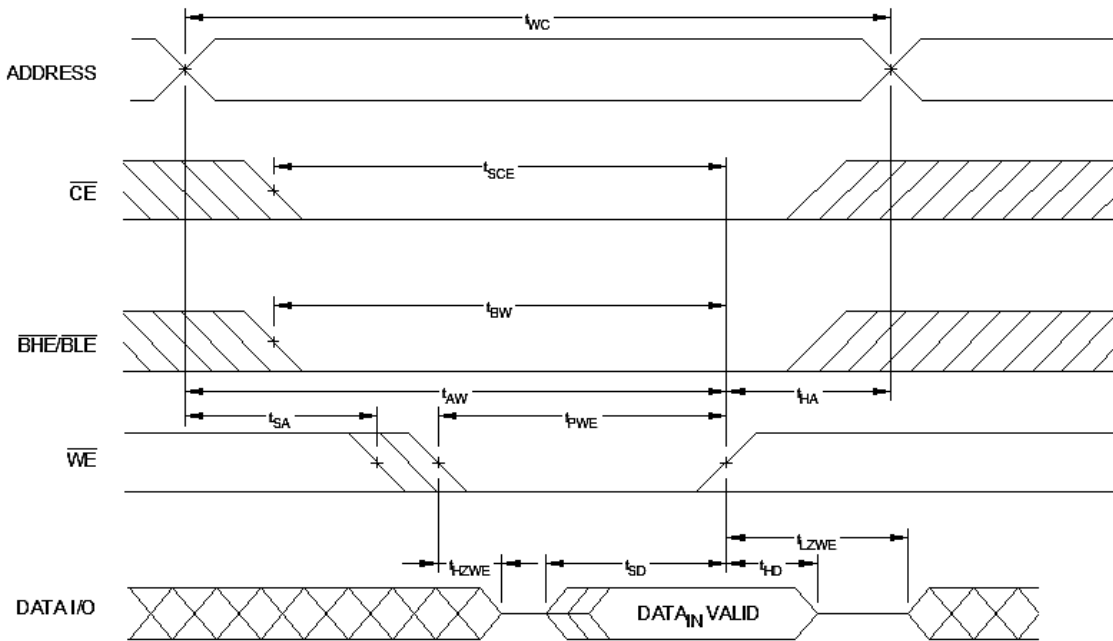
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SHEET **17**

DEVICE TYPE 01

Write Cycle Number 3 (\overline{WE} controlled, \overline{OE} LOW, see note 6 at end of Figure 5)



Write Cycle Number 4 (\overline{BHE} or \overline{BLE} controlled, see notes 4 and 5 at end of Figure 5)

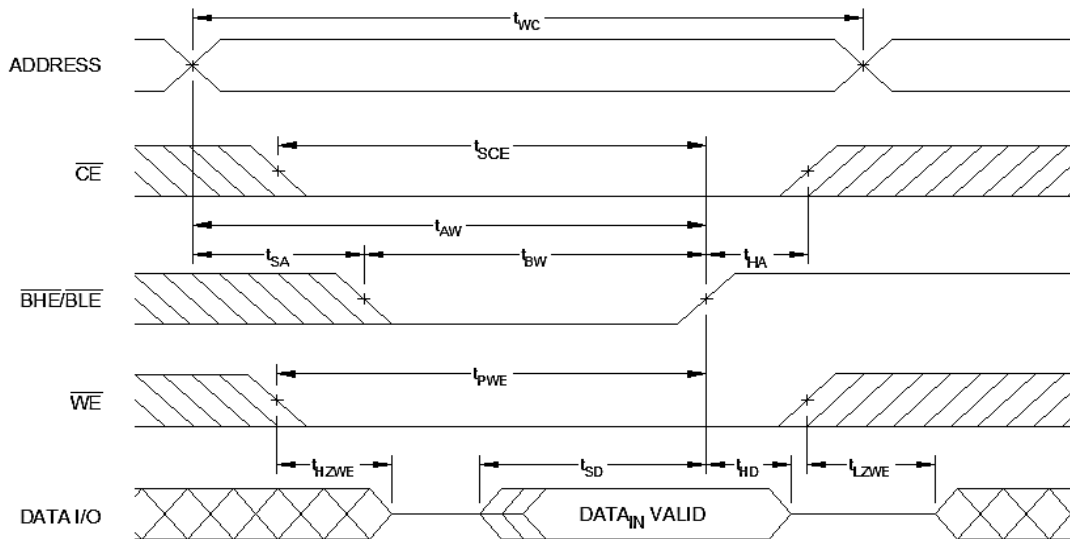


FIGURE 5. Timing waveforms – Continued.

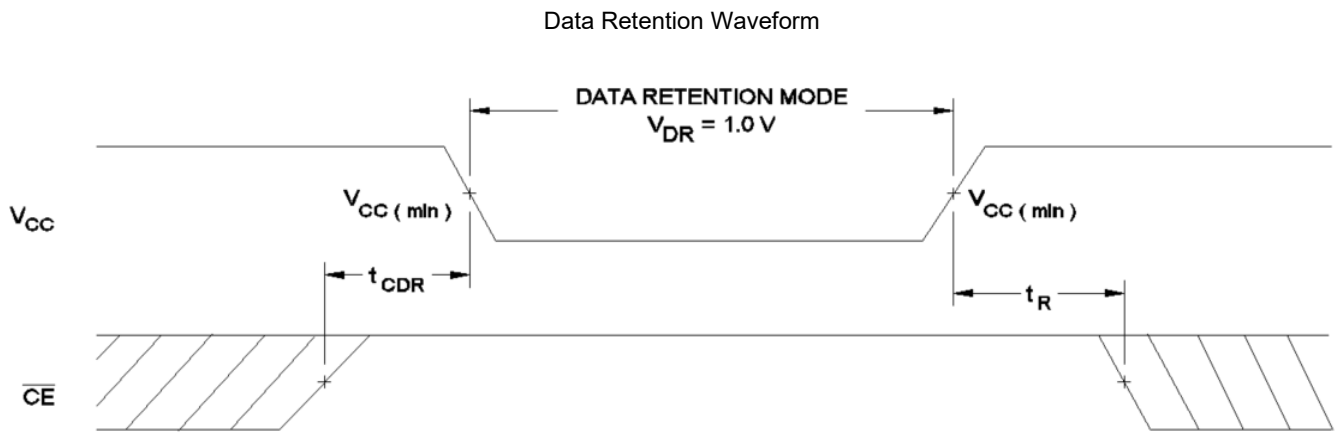
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NOTES:

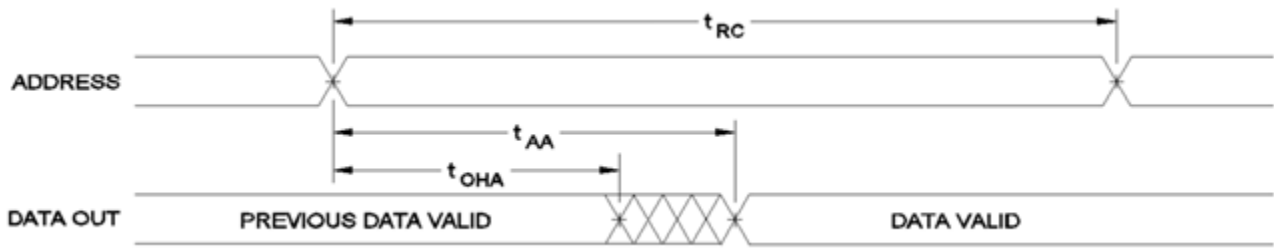
1. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{OL} .
2. WE is HIGH for read cycle.
3. Address valid prior to or coincident with \overline{CE} transition LOW.
4. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$ and $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
5. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
6. The minimum write cycle width should be sum of t_{HZWE} and t_{SD} .
7. During this period the I/Os are in output state. Do not apply signals.

FIGURE 5. Timing waveforms – Continued.

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DEVICE TYPE 02

Read Cycle Number 1 (see notes 1 and 2 at end of Figure 5)



Read Cycle Number 2 (\overline{OE} controlled, see notes 3 and 4 at end of Figure 5)

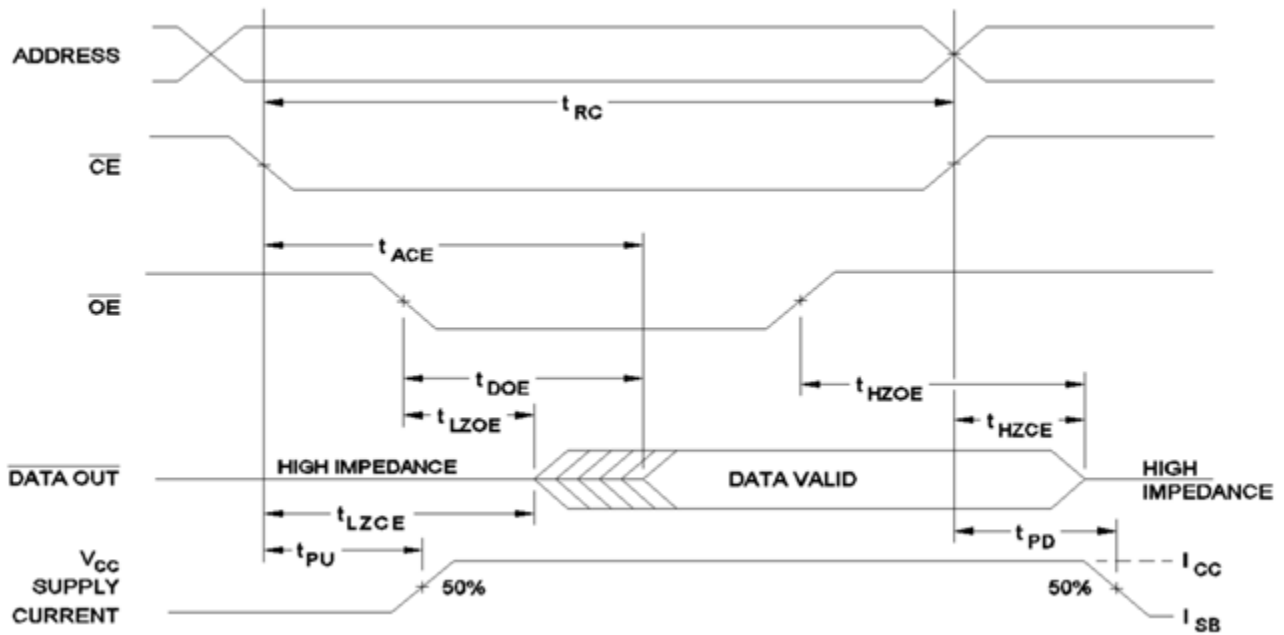


FIGURE 5. Timing waveforms – Continued.

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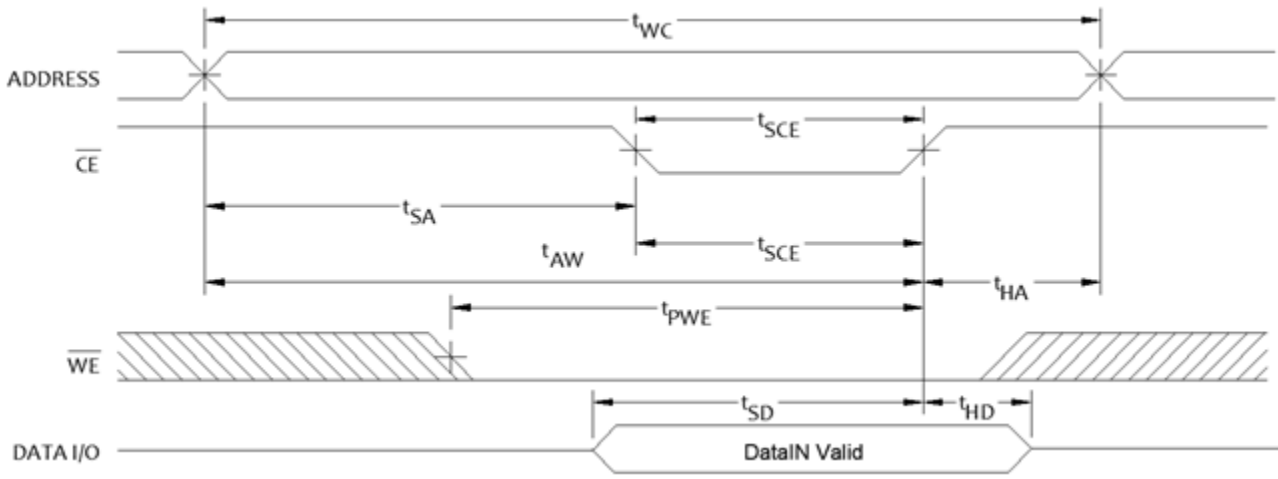
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SHEET **20**

DEVICE TYPE 02

Write Cycle Number 1 (\overline{CE} controlled, see notes 4 and 5 at end of Figure 5)



Write Cycle Number 2 (\overline{WE} controlled, \overline{OE} HIGH during write, see notes 4, 5 and 6 at end of Figure 5)

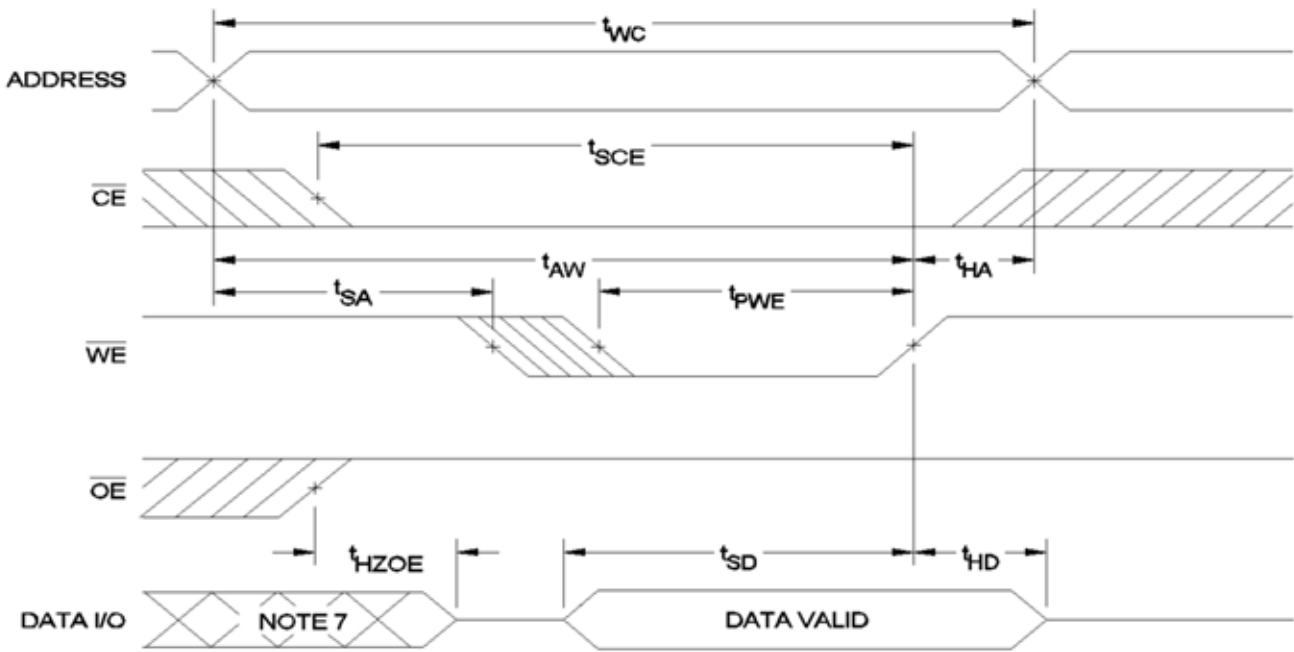


FIGURE 5. Timing waveforms – Continued.

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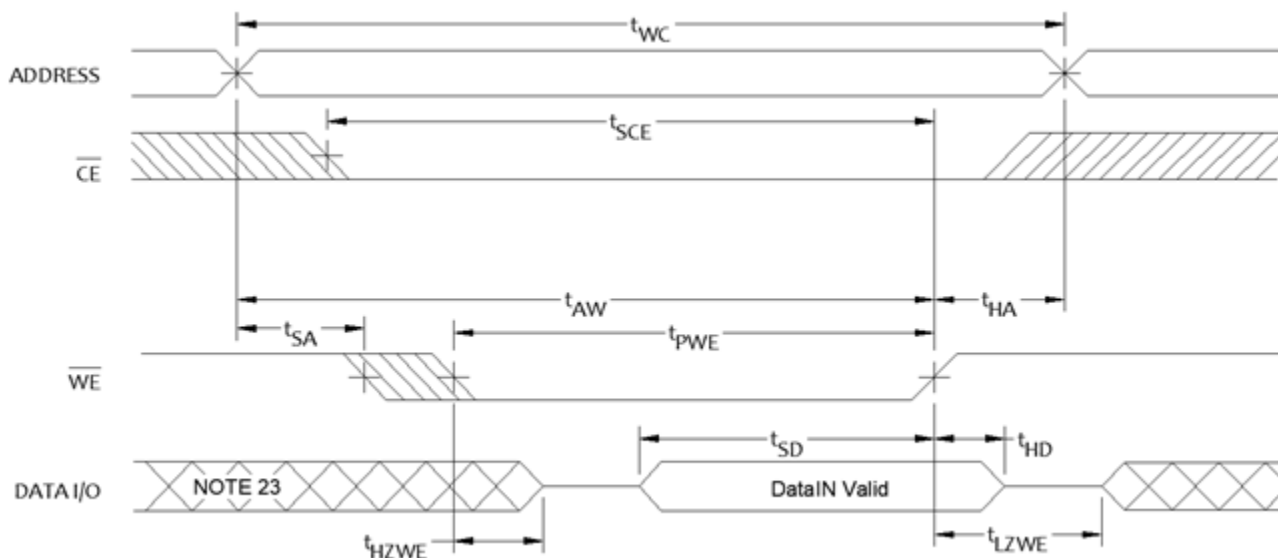
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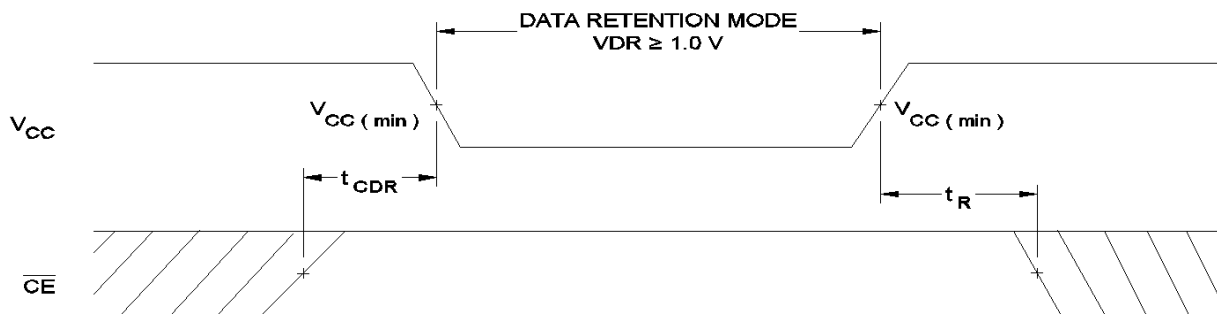
SHEET **21**

DEVICE TYPE 02

Write Cycle Number 3 (\overline{WE} controlled, \overline{OE} LOW, see note 6 at end of Figure 5)



Data Retention Waveform



NOTES:

1. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
2. \overline{WE} is HIGH for read cycle.
3. Address valid prior to or coincident with \overline{CE} transition LOW.
4. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$ and $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
5. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.
6. The minimum write cycle width should be sum of t_{HZWE} and t_{SD} .
7. During this period, the I/Os are in output state. Do not apply input signal.

FIGURE 5. Timing waveforms – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.
 - (1) For class Q devices, the burn-in test operating frequency shall be greater than or equal to 0.5 MHz.
- b. Interim and final electrical test parameters shall be as specified in Table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.
- d. Additional screening performed for device class Q:
 - (1) Wafer Lot Acceptance Test for all lots in accordance with MIL-STD-883, method 5007.
 - (2) 100% internal visual in accordance with MIL-STD-883, method 2010, Condition A.
 - (3) 100% Non-destructive Bond Pull Alternative Method in accordance with MIL-STD-883, method 2023.
 - (4) 100% PIND in accordance with MIL-STD-883, method 2020, Condition A.
 - (5) Serialization.
 - (6) Burn-in Test in accordance with MIL-STD-883, method 1015 for 240 Hours at 125°C.
 - (7) 3% defective allowable calculation (PDA) (Functional Parameters at 25°C).
 - (8) Radiography (X-Ray) in accordance with MIL-STD-883, method 2012 for two views.
- e. Additional screening performed for device class V:
 - (1) Fine Leak and Gross Leak tests.
 - (2) 100% Electrical tests at 25°C.
 - (3) Static Burn-in Test in accordance with MIL-STD-883, method 1015 for 144 Hours at 125°C.
 - (4) 100% External Visuals in accordance with MIL-STD-883, method 2009.

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4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in Table IIA herein.
- b. Subgroups 5 and 6 of Table IA of method 5005 of MIL-STD-883 shall be omitted.
- c. For device classes Q and V subgroups 7, 8A, and 8B shall include verifying the functionality of the device.
- d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in Table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in Table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in Table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and D, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

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4.4.4.2 Dose rate induced latch-up testing. When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.5).

- a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices.
- b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM Standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° < angle < 60°). No shadowing of the ion beam due to fixturing or package related effects are allowed.
- b. The fluence shall be > 100 errors or > 10⁷ ions/cm².
- c. The flux shall be between 10² and 10⁵ ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be > 20 microns in silicon.
- e. The test temperature shall be +25°C ±10°C for single event upset testing and at the maximum rated operating temperature +10°C for single event upset testing.
- f. Bias conditions shall be defined by the manufacturer for latch-up measurements.
- g. Test four devices with zero failures.

4.4.4.5 Neutron irradiation testing. Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.5). All device classes must meet the post irradiation end-point electrical parameter limits as defined in Table IA, for the subgroups specified in Table IIA herein at T_A = +25°C ± 5°C.

4.5 Delta measurements for device class V. Delta measurements, as specified in Table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in Table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line No	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		1*, 7*, 9 Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1*, 7*, 9 Δ	1*, 7*, 9 Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

- 1/ Blank spaces indicate tests are not applicable.
 2/ Any or all subgroups may be combined when using high-speed testers.
 3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
 4/ * indicates PDA applies to subgroup 1 and 7.
 5/ ** see 4.4.1e.
 6/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (lines 1 and 3).
 7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	All device types
I _{DD} , I _{SB1} , I _{SB2}	±10% of measured value
I _{LK} , I _{OLK}	±1 μA
V _{OH} , V _{OL}	±10% of measured value

- 1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

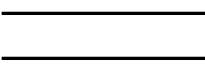



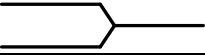
6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA test conditions of SEP.
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Occurrence of latchup (SEL).

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APPENDIX A
Appendix A forms a part of SMD 5962-20202

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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APPENDIX A – Continued.
Appendix A forms a part of SMD 5962-20202

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-10-26

Approved sources of supply for SMD 5962-20202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard Microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R2020201VXC	65786	CYRS1061G30-10GGMB
5962R2020202VYC	65786	CYRS1069G30-10FZMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

65786

Vendor name
and address

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1506

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.