REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Revision Status of Sheets

REV																					
SHEET																					
REV																					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16					

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
22-03-28

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR, PRECISION, CMOS INPUT, RRIO, WIDE SUPPLY RANGE AMPLIFIERS, MONOLITHIC SILICON

AMSC N/A

REVISION LEVEL

SIZE	CAGE CODE	
A	**67268**	**5962-19206**

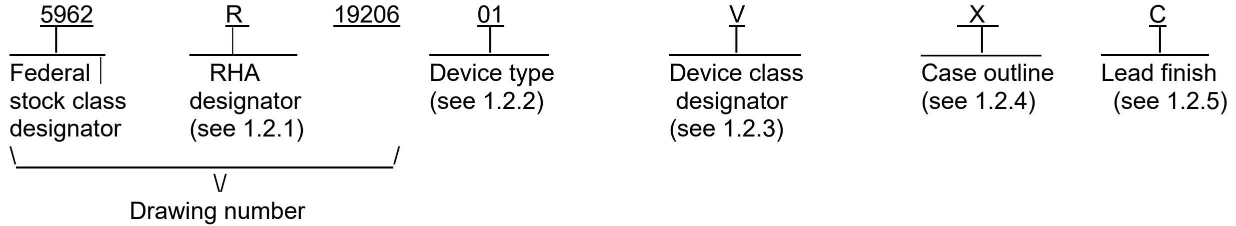
SHEET 1 OF 16

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LMP7704-SP	Precision, CMOS input, rail to rail input and output (RRIO), wide supply range amplifiers

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	14	Ceramic flat pack with metal lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_S) = (+V) – (-V) .... 13.2 V
Signal input pins
Common mode voltage .... -V – 0.3 V to +V + 0.3 V
Differential voltage .... +V – (-V + 3 V)
Current .... ±10 mA
Output short circuit .... Continuous 2/
Junction temperature (T_J) .... +150°C
Storage temperature range .... -65°C to +150°C
Operating temperature range (T_A) .... -55°C to +150°C
Electrostatic discharge (ESD) rating:
Human body model (HDM), per JEDEC JS-001 .... ±2000 V 3/
Charge device model (CDM), per JEDEC JESD22-C101 .... ±1000 V 4/

1.4 Recommended operating conditions.

Supply voltage V_S = (+V) – (-V) .... 2.7 V to 12 V
Specified temperature range (T_A) .... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	37.5	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	20.6	°C/W
Thermal resistance, junction-to-board	θ_{JB}	21.3	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	12.9	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	21.0	°C/W

1.6 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) .... 100 krads(Si) 5/
Single event phenomena (SEP):
No single event latchup (SEL) occurs at effective LET (see 4.4.4.2) .... ≤ 85 MeV/(mg/cm^2) 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Short circuit to ground, one amplifier per package.
3/ JEDEC document JEP155 states that 550 V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
5/ The manufacturer supplying devices technology has been performed total ionizing dose (TID) characterization testing in accordance with MIL-STD-883 method 1019, condition A and D at a dose level of 100 krads(Si). However, device type 01 has been performed radiation lot acceptance test (RLAT) with high dose rate condition A as specified in MIL-STD-883, method 1019. The radiation end points limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si).
6/ Manufacturer performed Heavy ion single event effects (SEE) test at the TAMU Cyclotron Radiation Effects facility using a superconducting cyclotron and an advanced electron cyclotron resonance (ECR) ion source. No single event latch-up (SEL) was observed to an effective LET of 85 MeV(mg/cm2). For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of this documents are available online at https://www.astm.org.)

JEDEC Solid State Technology Association

JEDEC JS-001 - Human Body Model Testing of Integrated Circuits
JESD22-C101 - Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC JEP 155 - Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 - Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ -55°C ≤ T_A ≤ +125°C V_S = 5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V_{OS}		1	01		±260	μV
			2, 3			±520	
Input offset voltage drift	$\Delta V_{OS}/T$		2, 3	01		±5	μV/°C
Power supply rejection ratio	PSRR	2.7 V < V_S <12 V	1	01	86		dB
			2, 3		82		
Input bias current							
Input bias current	I_B		1	01		±10	pA
			2, 3			±400	
Input voltage							
Common mode voltage range	V_{CM}		1, 2, 3	01	-V – 0.2	+V + 0.2	V
Common mode rejection ratio	CMRR	-V < V_{CM} < +V	4	01	85		dB
			5, 6		81		
Open loop gain							
Open loop voltage gain	A_{OL}	-V + 0.3 V < V_{OUT} < +V – 0.3 V, R_L = 2 kΩ	4	01	100		dB
			5, 6		94		
		-V + 0.2 V < V_{OUT} < +V – 0.2 V, R_L = 10 kΩ	4		100		
			5, 6		96		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \leq T_A \leq +125°C$ $V_S = 5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail,	V_O	Positive rail, $R_L = 2$ kΩ to $V_S/2$	1	01		120	mV
			2, 3			200	
		Positive rail, $R_L = 10$ kΩ to $V_S/2$	1			60	
			2, 3			120	
		Negative rail, $R_L = 2$ kΩ to $V_S/2$	1			120	
			2, 3			190	
		Negative rail, $R_L = 10$ kΩ to $V_S/2$	1			50	
			2, 3			100	
Power supply							
Total quiescent current	I_Q		1	01		3.7	mA
			2, 3			5.1	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 3/ -55°C ≤ T_A ≤ +125°C V_S = 10 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Offset voltage							
Input offset voltage	V_{OS}		1	01		±260	μV
			2, 3			±520	
Input offset voltage drift	$\Delta V_{OS}/T$		2, 3	01		±5	μV/°C
Power supply rejection ratio	PSRR	2.7 V < V_S < 12 V	1	01	86		dB
			2, 3		82		
Input bias current							
Input bias current	I_B		1	01		±10	pA
			2, 3			±400	
Input voltage							
Common mode voltage range	V_{CM}		1, 2, 3	01	-V – 0.2	+V + 0.2	V
Common mode rejection ratio	CMRR	-V < V_{CM} < +V	4	01	90		dB
			5, 6		86		
Open loop gain							
Open loop voltage gain	A_{OL}	-V + 0.3 V < V_{OUT} < +V – 0.3 V, R_L = 2 kΩ	4	01	100		dB
			5, 6		94		
		-V + 0.2 V < V_{OUT} < +V – 0.2 V, R_L = 10 kΩ	4		100		
			5, 6		97		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \leq T_A \leq +125°C$ $V_S = 10$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail,	V_O	Positive rail, $R_L = 2$ kΩ to $V_S/2$	1	01		120	mV
			2, 3			200	
		Positive rail, $R_L = 10$ kΩ to $V_S/2$	1			60	
			2, 3			120	
		Negative rail, $R_L = 2$ kΩ to $V_S/2$	1			120	
			2, 3			190	
		Negative rail, $R_L = 10$ kΩ to $V_S/2$	1			50	
			2, 3			100	
Power supply							
Total quiescent current	I_Q	$I_O = 0$ A	1	01		4.2	mA
			2, 3			5.7	

1/ Devices supplied to this drawing have been characterized to levels M, D, P, L and R of irradiation. However, device type 01 has been performed radiation lot acceptance test (RLAT) with high dose rate condition A as specified in MIL-STD-883, method 1019 to TID level 100 krads(Si). Pre and Post irradiation values are identical unless otherwise specified in Table IA.
When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ Unless otherwise specified, $V_S = +V - -V = 5$ V, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10$ kΩ connected to $V_S/2$.

3/ Unless otherwise specified, $V_S = +V - -V = 10$ V, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10$ kΩ connected to $V_S/2$.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP	Supply voltages	Effective linear energy transfer (LET)
01	No SEL	2.7 V and 12 V	LET ≤ 85 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by technical review board and qualifying activity.

3/ Tested for single event latch up at worse case temperature, $T_C = +125°C \pm 10°C$.

Case X

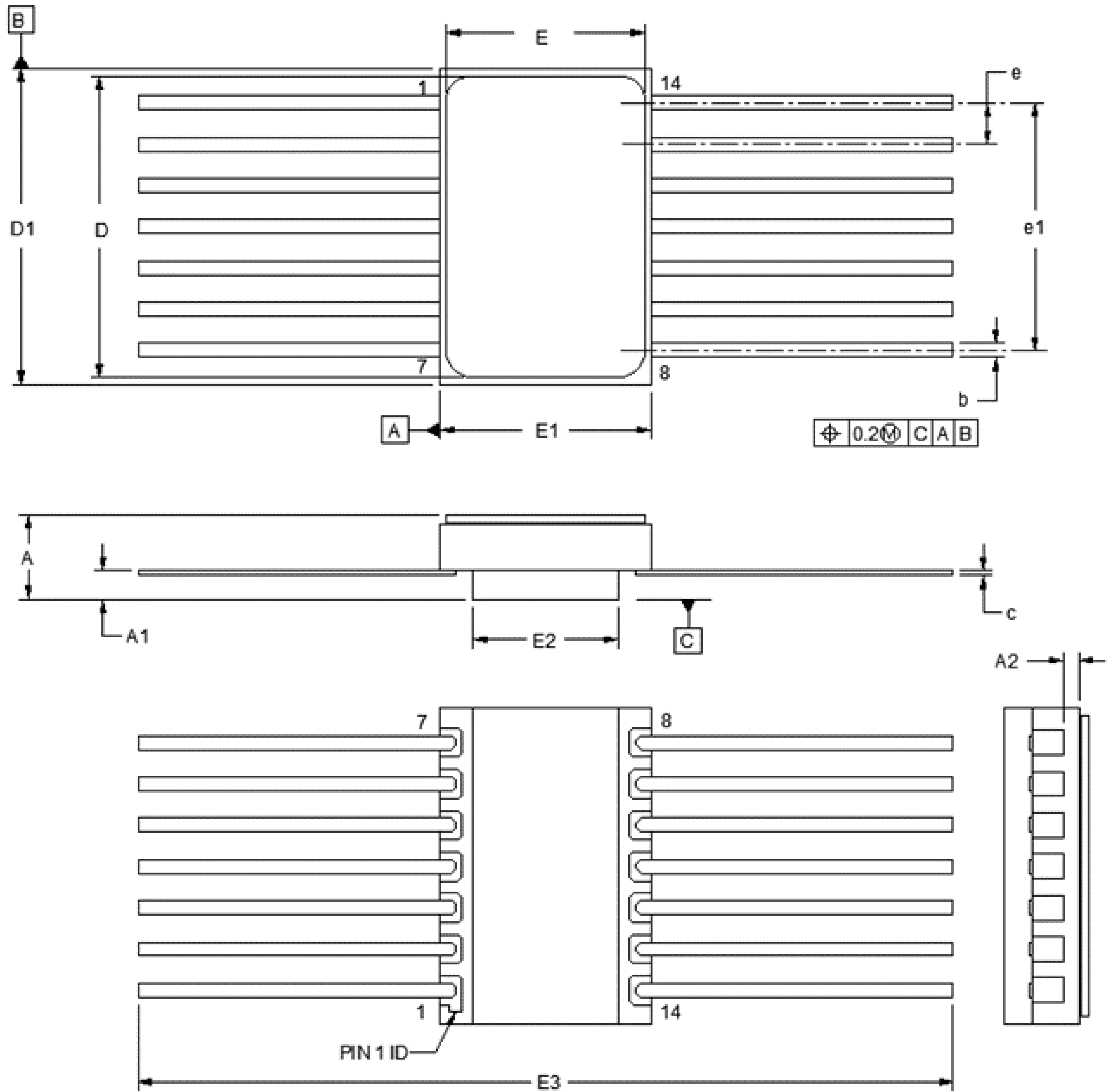


FIGURE 1. Case outline.

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.113	---	2.874
A1	---	.017	---	0.43
A2	.007	---	0.18	---
b	.015	.019	0.382	0.482
c	.004	.007	0.10	0.18
D	.365 REF		9.27 REF	
D1	.376	.390	9.55	9.91
e	.050 BSC		1.27 BSC	
e1	.300 BSC		7.62 BSC	
E	.240 REF		6.09 REF	
E1	.248	.262	6.30	6.65
E2	.175 REF		4.45 REF	
E3	---	.984	---	25

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
3. The leads are gold plated.

FIGURE 1. Case outline - continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	OUT A	O	Output for amplifier A.
2	IN -A	I	Inverting input for amplifier A.
3	IN +A	I	Noninverting input for amplifier A.
4	+V	P	Power supply.
5	IN +B	I	Noninverting input for amplifier B
6	IN –B	I	Inverting input for amplifier B
7	OUT B	O	Output for amplifier B
8	OUT C	O	Output for amplifier C
9	IN -C	I	Inverting input for amplifier C
10	IN +C	I	Noninverting input for amplifier C
11	-V	P	Negative supply
12	IN +D	I	Noninverting input for amplifier D
13	IN –D	I	Inverting input for amplifier D
14	OUT D	O	Output for amplifier D

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535 table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,2,3,4,5,6	1,2,3,4,5,6
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3,4,5,6 1/ 2/
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6 2/
Group D end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group E end-point electrical parameters (see 4.4)	---	1,4

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Delta limit	Units
Input offset voltage	V_{OS}	5 V	10.761	μV
		10 V	11.158	
Total quiescent current	I_Q	5 V, I_O = 0 A	0.013	mA
		10 V, I_O = 0 A	0.014	
Input bias current	I_B	5 V	0.325	pA
		10 V	0.376	
Short circuit current	I_{SC}	5 V, V_{OUT} = V_S/2, V_{IN} = 100 mV	0.322	mA
		10 V, V_{OUT} = V_S/2, V_{IN} = 100 mV	0.409	
Low level leakage current	I_{LVL}		0.200	mA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C.

4.4.4.2. Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing.
The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be the maximum rated operating temperature 125°C for the latchup measurements.

f. Bias conditions shall be supply voltage at 2 V for the latchup measurements.

g. Test four devices with zero failures.

h. See Table IB for SEP limits.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latch ups (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-03-28

Approved sources of supply for SMD 5962-19206 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1920601VXC	01295	LMP7704-SP
5962R1920601VXC	01295	LMP7704-SP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.