REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changed Appendix A (FUNCTIONAL ALGORITHMS) to Appendix B. VEN add die. Updated previous revision to add paragraph 3.1.1 and Appendix A comprises die requirements. Update references to Appendices. -rep	23-12-04	James Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	A	A	A	A																		
SHEET	23	24	25	26																		
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
23-04-21

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

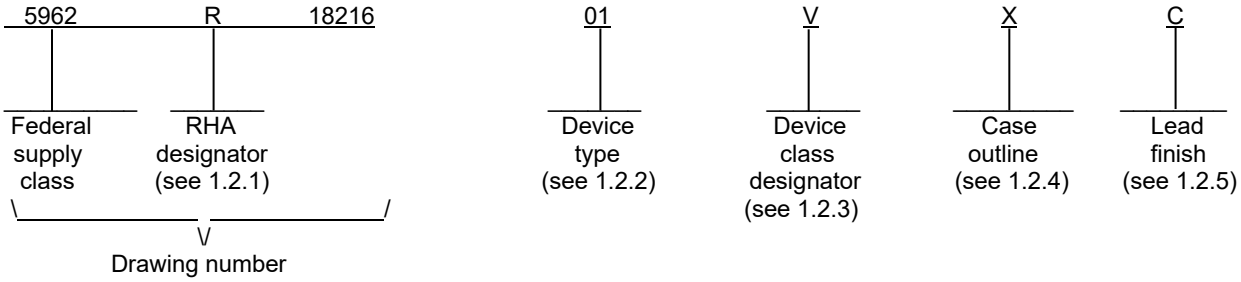
MICROCIRCUIT, MEMORY, DIGITAL, CMOS RADIATION HARDENED, 256K x 8-BIT FERROELECTRIC RANDOM ACCESS MEMORY (FRAM), MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL A	SIZE A	CAGE CODE **67268**	**5962-18216**
		SHEET	1 OF 26	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function	Access Time	Endurance
01	CYRS15B102	SPI with ECC, 2.0-3.6 Volt, Radiation Hardened, FRAM	25MHz	1 x 10^{13} cycles

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	16	Ceramic Small Outline Package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-1.0 V dc to +4.5 V dc
DC input voltage range (V_{IN})	-1.0 V dc to +4.5 V dc and $V_{IN} < V_{DD}$ +1.0 V dc 2/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{DD} + 0.5 V dc 2/
Storage temperature range	-65ºC to +150ºC
Case operating free-air temperature range, (T_C)	-55ºC to +125ºC
Lead temperature (soldering 3 seconds)	+260ºC
Thermal resistance, junction to case (θ_{JC})	17.04ºC/W
Maximum power dissipation	0.036 W @ 25 MHz
Maximum junction temperature (T_J)	130ºC
Data retention:	
T_C = 125ºC	11k hours
T_C = 105ºC	11 years
T_C = 85ºC	121 years
Write cycle endurance	1 x 10^{13} cycles 3/

1.4 Recommended operating conditions. 2/ 3/ 4/

Supply voltage range (V_{DD})	2.0 V dc to 3.6 V dc
Supply voltage reference (GND)	0.0 V dc
High level input voltage range (V_{IH})	1.4 V to V_{DD}
Low level input voltage range (V_{IL})	0.0 V dc to 1.0 V dc
Case operating temperature range (T_C)	-55ºC to +125ºC

1.5 Radiation features.

Maximum total ionizing dose available (High dose rate = 50 - 300 rads(Si)/s)	= 100 krad(Si) 5/
Maximum total ionizing dose available (Reduced dose rate = 10 rads(Si)/s)	= 100 krad(Si) 5/
Single event phenomenon (SEP):	
No SEL cours at effective LET (see 4.4.4.4) at 115ºC	≤ 114 MeV-cm^2/mg) 6/
Single event upset (SEU) error rate at in-situ LET 2.5 MeV-cm^2/mg.....	= 1.34 x 10^{-4} error /dev-day 6/
No dose rate induced upset - static.....	≤ 1.1 x 10^{11} rad(Si)/sec 7/
Dose rate induced functional upset – R/W.....	= 1.1 x 10^8 rad(Si)/sec 7/
Dose rate survivabilty (RS)	= 1.1 x 10^{11} rad(Si)/sec 7/
Neutron irradiation (1 MeV equivalent)	= 2 x 10^{14} neutrons/cm^2

———

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum or minimum levels may degrade performance and affect reliability.
2/ All voltage are reference to GND and maximum applied voltage shall not exceed +4.5 V.
3/ Endurance assumes a 50% write 1's and 50% write 0's.
4/ Power shall be applied to the device only in the following sequences to prevent damage due to excessive currents. Power-up sequence: GND, V_{DD}, Inputs. Power-down sequence: Inputs, V_{DD}, GND.
5/ Manufacturer supplying device type 01 has performed total ionizing dose (TID) testing in accordance with MIL-STD-883, method 1019, condition A to a maximum TID level of 150 krads(Si) and condition C to a maximum TID level of 200 krads(Si). However, devices are marked to standard 100 krads(Si) of RHA TID level R. For details concerning the TID test report, please contact the manufacturer.
6/ For detailed heavy ion single event effects (SEE) test report, contact the device manufacturer. For single event upset error rate = 1.34 x 10^{-4} errors/dev-day consider SEU error rate calculation CREME96 Geosynchronous orbit.
7/ Flash X-ray (FXR) test and detailed test reports can be requested by the customer through the purchase order.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.
MIL-HDBK-814 - Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following documents form a part of this document to the specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

JESD 22-A117E - Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test.

JESD 47L - Stress-Test-Driven Qualification of Integrated Circuits.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The read and write cycle timing waveforms shall be as specified on figure 4.

3.2.5 Irradiation bias circuit for total dose. The irradiation bias circuit for total dose shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.6 Functional tests. Various functional tests used to test this device are contained in the appendix B. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Write cycle endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific but shall guarantee the number of program/erase endurance cycles listed in section 1.3 here in over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data. Testing may be done per JESD 22-A117 and JESD 47.

3.9 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific but shall guarantee the number of years listed in section 1.3 herein over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data. Testing may be done per JESD 22-A117 and JESD 47.

3.10 Write protection. A write protection test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect the operation in PROM mode. The methods and procedures may be vendor specific but shall guarantee that when V_{PP} is 0 V and / or the write protect signal is low, the memory is disabled for write operations while maintaining the read operation availability over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $2.0\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Supply Current	I_{DD}	F_{SCK} = 25 MHz SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V.		1, 2, 3	All		10	mA
Supply Current (Standby)	I_{SB}	$\overline{CS}$ = V_{DD} All other inputs V_{SS} or V_{DD}	TID = 0 Krad	1, 2, 3	All	--	850	µA
			TID = 150 Krad	1, 2, 3	All	--	6	mA
Supply Current (Sleep)	I_{ZZ}	$\overline{CS}$ = V_{DD} All other inputs V_{SS} or V_{DD}	TID = 0 Krad	1, 2, 3	All	--	25	µA
			TID = 150 Krad	1, 2, 3	All	--	8	mA
Low level output voltage	V_{OL}	I_{OL} = 2 mA, V_{DD} = 2.7 V		1, 2, 3	All	--	0.4	V
		I_{OL} = 150 µA					0.2	
High level output Voltage	V_{OH}	I_{OH} = -1 mA, V_{DD} = 2.7 V		1, 2, 3	All	2.4		V
		I_{OH} = -100 µA				V_{DD} - 0.2V		
High level input voltage	V_{IH}			1, 2, 3	All	0.7 x V_{DD}	V_{DD} + 0.3V	V
Low level input voltage	V_{IL}			1, 2, 3	All	-0.3 V	0.3 x V_{DD}	V
Input leakage current	I_{ILK}	$V_{SS} < V_{IN} < V_{DD}$		1, 2, 3	All	-10	10	µA
Output leakage current	I_{OLK}	$V_{SS} < V_{OUT} < V_{DD}$		1, 2, 3	All	-10	10	µA
Input capacitance	C_{IN}	See 4.4.1e		4	All		6	pF
Output capacitance	C_{OUT}			4	All		8	pF
Functional tests		See 4.4.1c		7, 8A, 8B	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $2.0\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Specification							
SCK clock frequency	f_{SCK}		9, 10, 11	All	0	25	MHz
Clock HIGH time	t_{CH}		9, 10, 11	All	18	--	ns
Clock LOW time	t_{CL}		9, 10, 11	All	18	--	ns
Chip select setup	t_{CSU}		9, 10, 11	All	12	--	ns
Chip select hold	t_{CSH}		9, 10, 11	All	12	--	ns
Output disable time 3/ 4/	t_{OD}		9, 10, 11	All	--	20	ns
Output data valid	t_{ODV}		9, 10, 11	All	--	16	ns
Output hold time	t_{OH}		9, 10, 11	All	0	--	ns
Deselect time	t_D		9, 10, 11	All	60	--	ns
Data in rise time 5/ 6/	t_R		9, 10, 11	All	--	50	ms
Data in fall time 5/ 6/	t_F		9, 10, 11	All	--	50	ns
Data setup time	t_{SD}		9, 10, 11	All	8	--	ns
Data hold time	t_{HD}		9, 10, 11	All	8	--	ns
$\overline{\text{HOLD}}$ setup time	t_{HS}		9, 10, 11	All	12	--	ns
$\overline{\text{HOLD}}$ hold time	t_{HH}		9, 10, 11	All	12	--	ns
$\overline{\text{HOLD}}$ LOW to HI-Z 3/ 4/	t_{HHZ}		9, 10, 11	All	--	25	ns
$\overline{\text{HOLD}}$ HIGH to data active 4/	t_{HLZ}		9, 10, 11	All	--	25	ns

1/ RHA devices supplied to this drawing have been characterized through all level M, D, P, L and R of irradiation. However, this device is only tested at the "R" level at the dose rate conditions A and C. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25ºC.

2/ Test conditions are defined at inception of test. The device is first stabilized at the desired temperature in an unpowered state to ensure that the module is at the desired case temperature (T_C) before parameters are measured. The case temperature (T_C) is maintained during testing at the specified temperature by a forced air test environment.

Test conditions for AC measurements are listed below.
Input Levels: $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$
Input rise and fall time: < 3.0 ns
Input and output timing reference levels: $0.5 \times V_{DD}$
Output load capacitance: 30pF

3/ t_{OD} and t_{HZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
4/ Characterized but not 100% tested in production.
5/ Rise and fall times measured between 10% and 90% of waveform.
6/ These parameters are guaranteed by design and are not tested.

Table IB. SEP test limits 1/ 2/

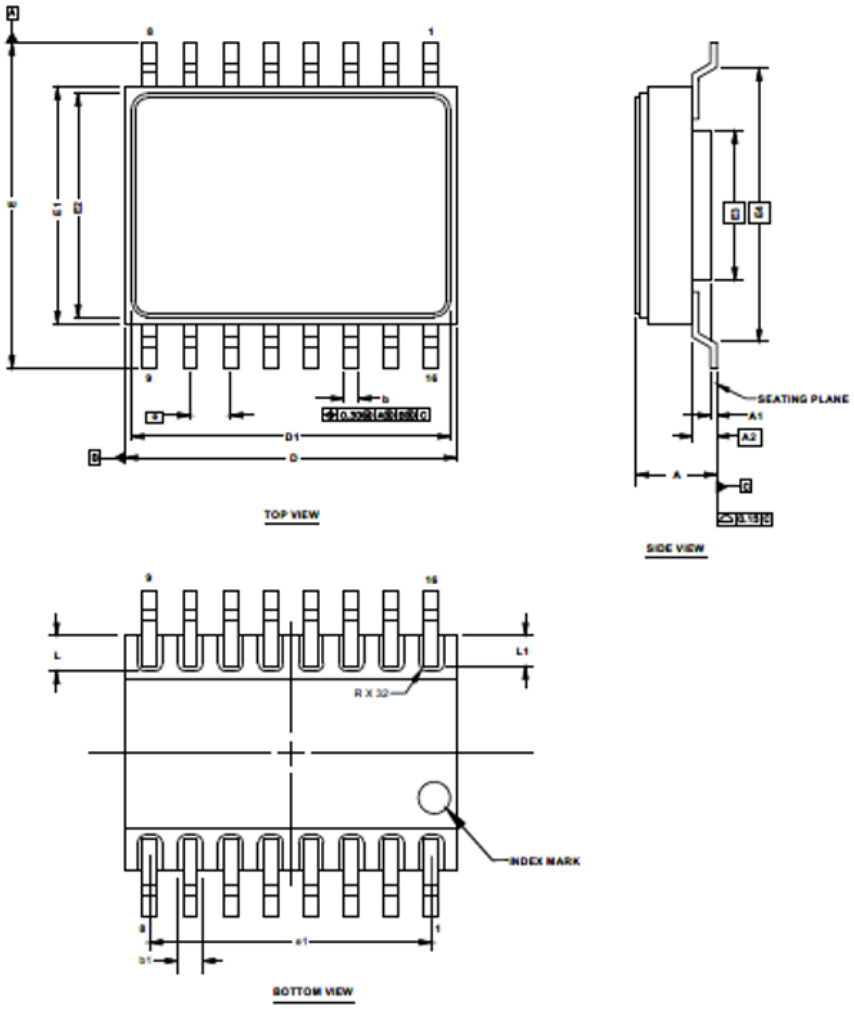
Device type	Single event upset error rate V_{DD} = 2.0 V and T_A = +25°C	Single Event Latch-up (SEL) test Bias V_{DD} = 3.6 V
	Single evet upsets error rate at Onset LET =2.5 MeV/(mg/cm^2) 3/	Effective LET No SEL occurs 3/
All	1.34 x 10^{-4} upsets/dev-day	114 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Heavy ion single event effects (SEE) test was performed at the Texas A&M Cyclotron facility. For single event upset error rate = 1.34 x 10^{-4} errors/dev-day consider SEU error rate calculation CREME96 Geosynchronous orbit. For SEL test worst case test temperature T_A = +115°C and for details SEE test report contact the device manufacturer.

Case outline X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		2.90	E4	9.00 BSC	
A1	0.17	0.23	b	0.37	0.47
A2	0.55 BSC		b1	0.81	1.07
D	10.30	10.60	L	1.2 BSC	
D1	9.84	10.24	L1	1.0 BSC	
E	10.11	10.41	e	1.14	1.40
E1	7.30	7.60	e1	8.74	9.04
E2	6.84	7.24	N	16	
E3	4.7 BSC		R	0.30 TYP	

Notes: 1. Terminal one shall be identified by a mechanical index in the lead or body, or a mark on the top surface.
2. Terminal identification numbers need not appear on the package.

FIGURE 1. Case outline.

Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	NC
2	$\overline{CS}$
3	SO
4	$\overline{WP}$
5	V_{SS}
6	V_{SS}
7	V_{SS}
8	V_{SS}
9	NC
10	NC
11	SI
12	SCK
13	$\overline{HOLD}$
14	V_{DD}
15	V_{DD}
16	V_{DD}

Note: 1. NC labeled connections are not internally connected to the die and floating.

FIGURE 2. Terminal connections.

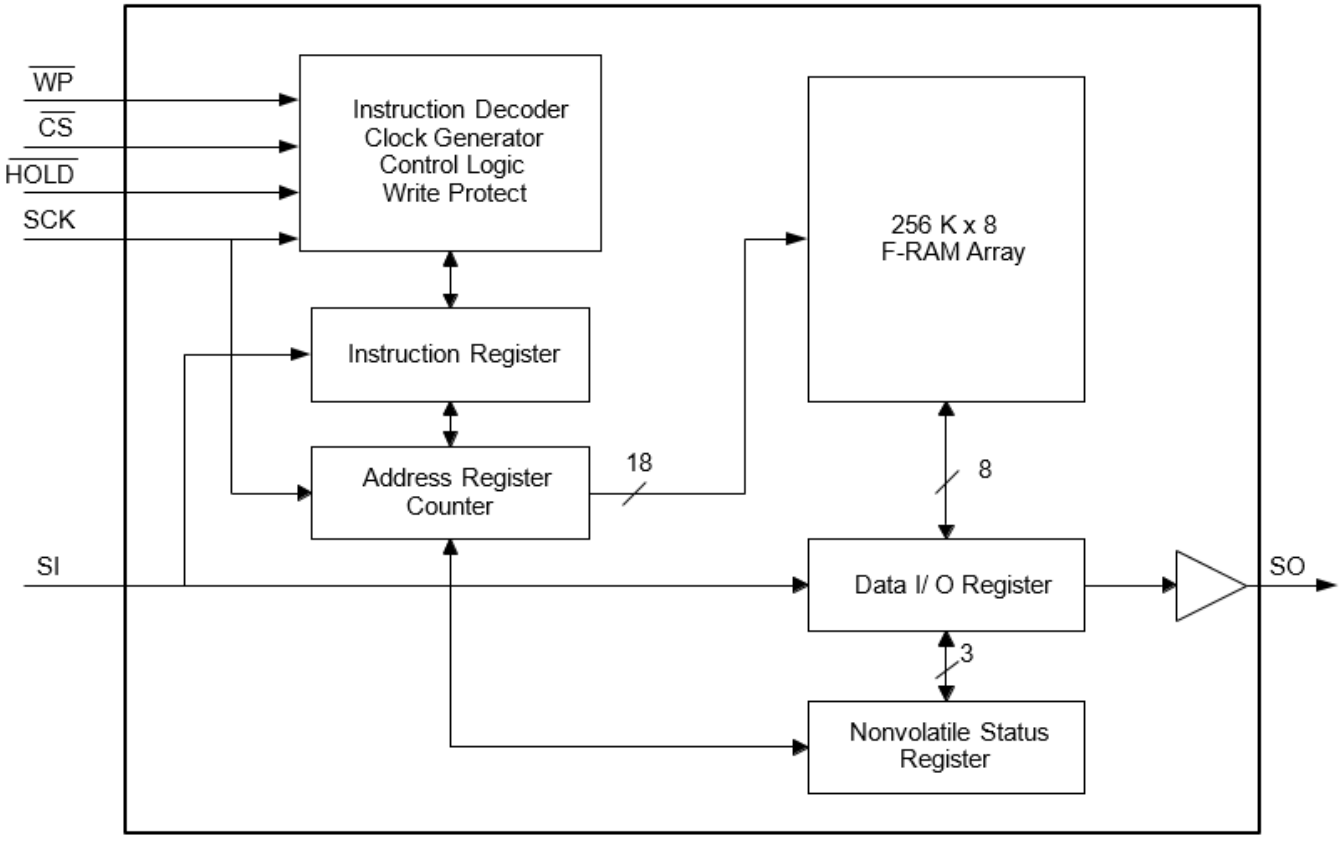
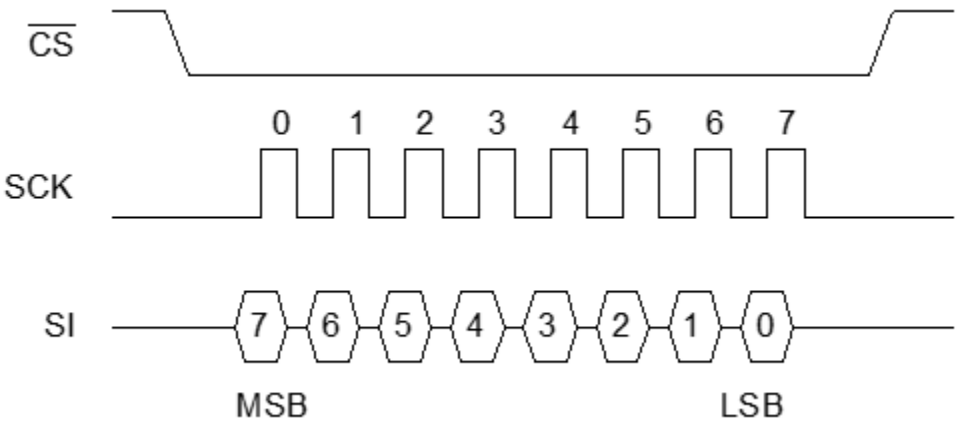


FIGURE 3. Block diagram.

SPI Mode 0



SPI Mode 3

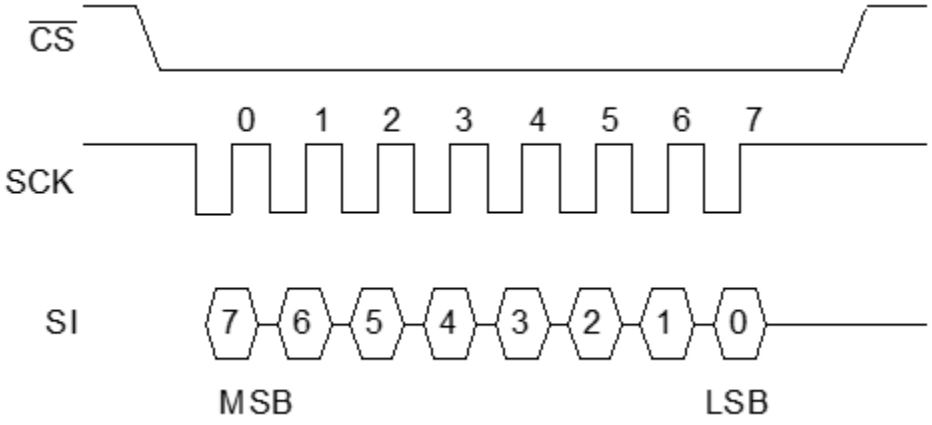
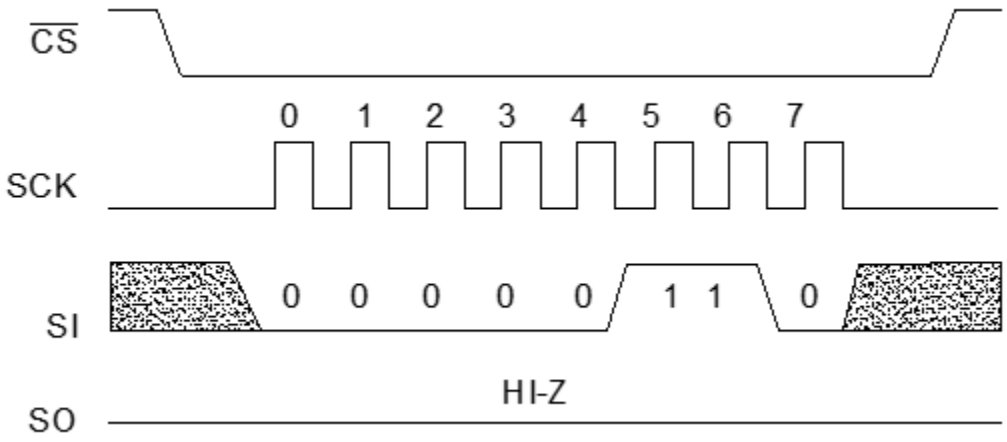


FIGURE 4. Timing waveforms.

WREN Bus Configuration



WRDI Bus Configuration

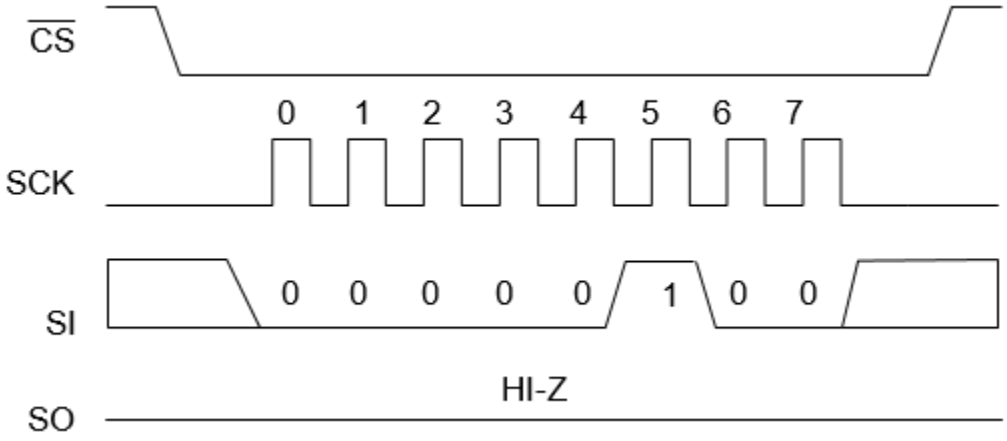


FIGURE 4. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device 01 shall include:

(1) 100% X-ray per MIL-STD-883, method 2012

(2) Increased burn-in (240 hours) dynamic burn-in

(3) Optional interim room temperature electrical test

(4) 144 hours static burn-in with tightened class V PDA

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table IA of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. In addition, special test structures may be used for latch-up characterization in place of using product. If test structures are used, testing shall be on five wafers. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1*, 7*, 9
Static burn-in (method 1015)	Not Required	Required
Same as line 1		1*, 7*, 9 Δ
Dynamic burn-in (method 1015)	Required	Required
Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ
Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

Table IIB. Delta limits at +25ºC.

Parameter 1/	Limits	Units
I_{DD}	± 10% of the measured value	mA
I_{SB}, I_{ZZ}	± 10% of the measured value	µA
I_{ILK}, I_{OLK}	± 1	µA
V_{OH}, V_{OL}	± 10% of the measured value	mV

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and condition C as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25ºC +5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60º to the normal, inclusive (i.e. 0º ≤ angle ≤ 60º). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25 ºC ±10 ºC. The latch-up test temperature shall be at 115ºC.

f. Bias conditions shall be V_{DD} maximum = 2.0 V dc for the upset measurements and V_{DD} max = 3.6 V dc for the latch-up measurements.

g. For SEP test limits, see table IB herein.

4.4.4.5 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at TA = +25 ºC ±5 ºC after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

a. RHA test conditions of SEP.

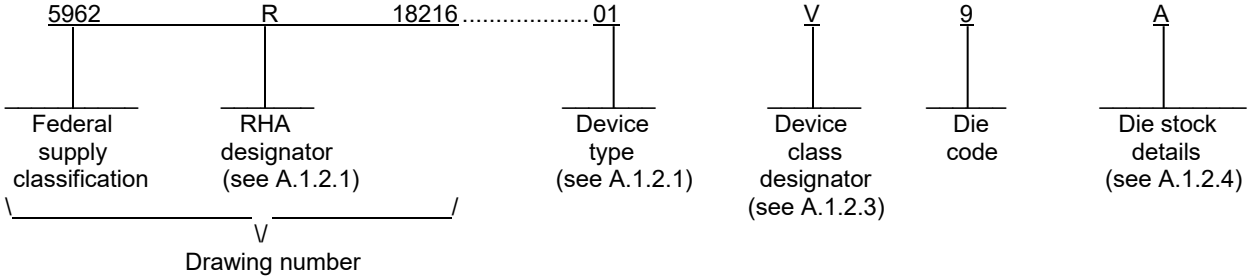
b. Number of upsets (SEU).

c. Occurrence of latch-up (SEL).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	CYRS15B102Q-1X11I	2Mbit SPI FRAM

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad locations and related electrical functions, interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.2.4.5 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.3 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 – Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 – Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 – List of Standard Microcircuit Drawings.
MIL-HDBK-780 – Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

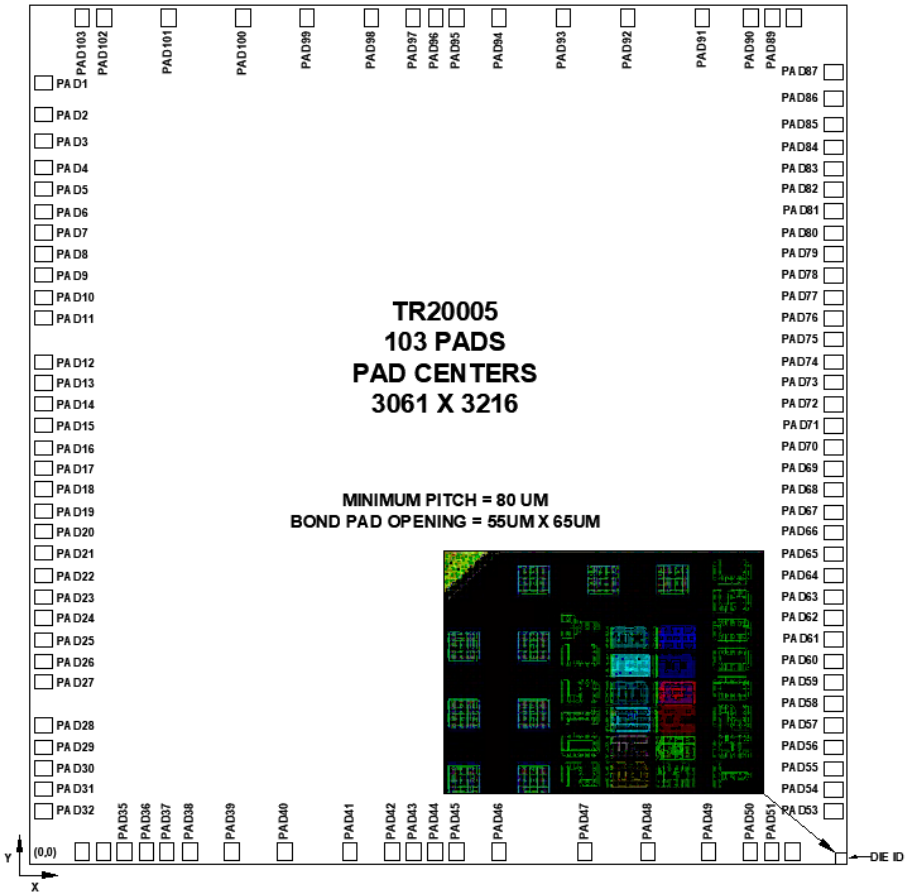
A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions



Die physical dimensions.
- Die size: 3061 x 3216 µm
- Die thickness: 11 mil

Interface materials.
- Top metallization: AlCu: 10kÅ ± 1500Å
- Backside metallization: None: chemical etch

Glassivation.
- Type: SiN/SiON/Oxide/SiN
- Thickness: 8kÅ ± 960Å / 1.5kÅ ± 360Å / 4kÅ ± 480Å / 500Å ± 50Å

Substrate: Single crystal silicon

Assembly related information.
- Substrate potential: Substrate internally tied to V_{SS}
- Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

APPENDIX B
Appendix A forms a part of SMD 5962-18216
FUNCTIONAL ALGORITHMS

B.1 SCOPE

B.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 1.4 herein.

B.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

B.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

B.3 ALGORITHMS

B.3.1 Algorithm A (pattern 1).

B.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

B.3.2 Algorithm B (pattern 2).

B.3.2.1 March Left-Right.

Step 1. Increment address from minimum to maximum writing each address with solid data pattern (xFF).
Step 2. Increment address from minimum to maximum while performing 2a and 2b.
Step 2a. Read and verify an address.
Step 2b. Write the address with complement data.
Step 3. Increment address from minimum to maximum while performing 3a, 3b, 3c, 3d.
Step 3a. Read and verify an address.
Step 3b. Write the address with complement data.
Step 3c. Read and verify the address.
Step 3d. Write the address with complement data.

B.3.3 Algorithm C (pattern 3).

B.3.3.1 Solid.

Step 1. Write x55 data pattern to all addresses from minimum to maximum.
Step 2. Read and verify x55 data pattern at all addresses.
Step 3. Write xAA data pattern to all addresses from minimum to maximum.
Step 4. Read and verify xAA data pattern at all addresses.
Step 5. Write xFF data pattern to all addresses from minimum to maximum.
Step 6. Read and verify xFF data pattern at all addresses.
Step 7. Write x00 data pattern to all addresses from minimum to maximum.
Step 8. Read and verify x00 data pattern at all addresses.

B.3.4 Algorithm D (pattern 4).

B.3.4.1 Control Signals Functional Verification.

Each test performed independently.
Write Protect Functional test: Write data with /WP = V_{IH}, read data with /WP = V_{IL} confirm no data change.
Hold Functional test: Write with /HOLD = V_{IL}, read data with /HOLD = V_{IH} and confirm no change in device state.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-12-04

Approved sources of supply for SMD 5962-18216 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1821601VXC	65786	CYRS15B102Q-GGMB
5962R1821601V9A	65786	CYRS15B102Q-1X11I

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 198 Champion Court San Jose, CA 95134-1709