| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Make correction to footnote 12/ in section 1.5 and footnote 3/ in Table IB by deleting "inside a vacuum chamber". -rrp | 20-06-24 | J. ESCHMEYER |
| B | Add case outline Y. -rrp | 21-02-09 | J. ESCHMEYER |

| REV | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | B | B | B | B | B | B | B | B | B | B | B | B | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | | | | | | | | |

| REV STATUS | REV | B | B | B | B | B | B | B | B | B | B | B | B | B |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
RAJESH PITHADIA

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**https://www.dla.mil/LandandMaritime**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
JAMES R. ESCHMEYER

DRAWING APPROVAL DATE
20-03-16

REVISION LEVEL
B

MICROCIRCUIT, DIGITAL-LINEAR, 12 BIT, RF SAMPLING, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-18209** |

SHEET 1 OF 26

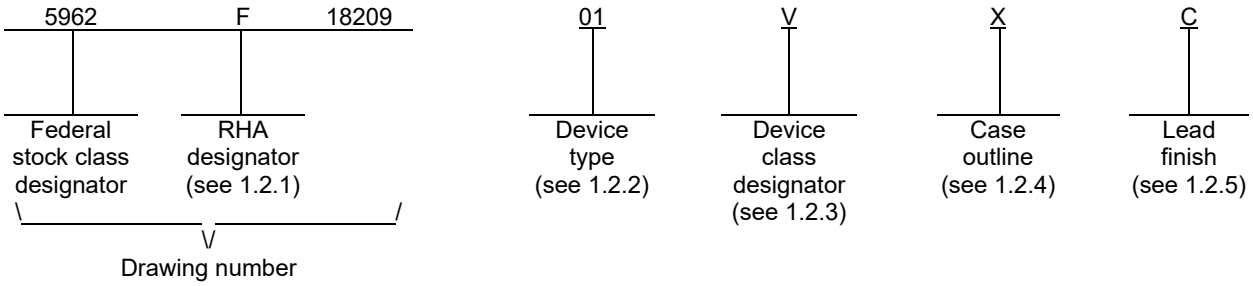
DSCC FORM 2233
APR 97

5962-E179-21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | ADC12DJ3200 | 12 Bit, 6.4 giga samples per second, single channel, or 3.2 giga samples per second, dual channel, RF sampling, analog-to-digital converter |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | See figure 1 | 196 | Ceramic Land Grid Array (LGA) |
| Y | See figure 1 | 196 | Ceramic Column Grid Array (CGA) |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage range ($V_{DD}$): | |
| VA19 2/ | -0.3 V to +2.35 V |
| VA11 2/ | -0.3 V to +1.32 V |
| VD11 3/ | -0.3 V to +1.32 V |
| Voltage between VD11 and VA11 | -1.32 V to +1.32 V |
| Voltage between AGND and DGND | -0.1 V to +0.1 V |
| Terminal voltage range: | |
| DA0...7+, DA0...7-, DB0...7+, DB0...7-,TMSTP+, TMSTP– 3/ 4/ | -0.5 V to (VD11 + 0.5) V |
| CLK+, CLK–, SYSREF+, SYSREF– 2/ 5/ | -0.5 V to (VA11 + 0.5) V |
| BG, TDIODE+, TDIODE– 2/ 6/ | -0.5 V to (VA19 + 0.5) V |
| INA+, INA–, INB+, INB– 2/ | -1 V to 1 V |
| CALSTAT, CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, ORA0, ORA1, ORB0, ORB1, PD, SCLK, SDI, SDO, $\overline{\text{SYNCSE}}$, $\overline{\text{SCS}}$ 2/ 6/ | -0.5 V to (VA19 + 0.5) V |
| Peak input current range (any input except INA+, INA–, INB+, INB–) | -25 mA to 25 mA |
| Peak input current range (INA+, INA–, INB+, INB–) | -50 mA to 50 mA |
| Peak RF input power (INA+, INA–, INB+, INB–): | |
| Single-ended with $Z_{S\text{-}SE}$ = 50 Ω or differential with $Z_{S\text{-}DIFF}$ = 100 Ω | 16.4 dBm |
| Peak total input current: | |
| Sum of absolute value of all currents forced in or out, not including power supply current | 100 mA |
| Storage temperature range | -65°C to +150°C |
| Maximum junction temperature | +150°C |
| Thermal resistance, junction-to-case top ($\theta_{JCTOP}$): | |
| Cases X and Y | 16.5°C/W |
| Thermal resistance, junction-to-case bottom ($\theta_{JCBOTTOM}$): | |
| Cases X and Y | 6.5°C/W 7/ |
| Thermal resistance, junction-to-ambient ($\theta_{JA}$): | |
| Cases X and Y | 24.7°C/W |
| Electrostatic discharge (ESD) ratings: | |
| Human body model (HBM) 8/ | -2,500 V to +2,500 V |
| Charged device model (CDM) 9/ | -500 V to +500 V |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Measured to AGND.
3/ Measured to DGND.
4/ Maximum voltage not to exceed VD11 absolute maximum rating.
5/ Maximum voltage not to exceed VA11 absolute maximum rating.
6/ Maximum voltage not to exceed VA19 absolute maximum rating.
7/ The case bottom temperature was taken at the bottom of the solder columns on a fixed temperature PCB. This parameter only applies when solder columns are attached to the device.
8/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
9/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{DD}$): | |
| VA19, analog 1.9 V supply 2/ | +1.8 V to +2.0 V |
| VA11, analog 1.1 V supply 2/ | +1.05 V to +1.15 V |
| VD11, digital 1.1 V supply 3/ | +1.05 V to +1.15 V |
| Input common mode voltage ($V_{CMI}$): | |
| INA+, INA–, INB+, INB– 2/ | -50 mV to 100 mV |
| CLK+, CLK–, SYSREF+, SYSREF– 2/ 10/ | 0.0 V to 0.55 V |
| TMSTP+, TMSTP- 2/ 11/ | 0.0 V to 0.55 V |
| Input voltage, peak-to-peak differential ($V_{ID}$): | |
| CLK+ to CLK-, SYSREF+ to SYSREF-, TMSTP+ to TMSTP- | 0.4 $V_{PP-DIFF}$ to 2.0 $V_{PP-DIFF}$ |
| INA+ to INA-, INB+ to INB- 10/ | 1.0 $V_{PP-DIFF}$ max 6/ |
| High level input voltage ($V_{IH}$): | |
| CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, PD, SCLK, $\overline{SCS}$, SDI, $\overline{SYNCSE}$ 2/ | 0.7 V min |
| Low level input voltage ($V_{IH}$): | |
| CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, PD, SCLK, $\overline{SCS}$, SDI, $\overline{SYNCSE}$ 2/ | 0.45 V max |
| Temperature diode input current ($I_{C\_TD}$): | |
| TDIODE+ to TDIODE- | 100 µA |
| BG maximum load capacitance ($C_L$) | 50 pF |
| BG maximum output current ($I_{OUT}$) | 100 µA |
| Input clock duty cycle range (DC) | 30% min to 70% max |
| Operating temperature range ($T_A = T_J$) | -55°C to +125°C |

1.5 Radiation features.

| | |
|---|---|
| Maximum total dose available (dose rate = 50 – 300 rad(Si)/s) | 300 krad(Si) 12/ |
| Single event phenomenon (SEP): | |
| No Single event latchup (SEL) occurs at effective LET (see 4.4.4.2) | ≤ 120 MeV/(mg/cm$^2$) 13/ |
| No Single event functional interrupt occurs at an effective LET (see 4.4.4.2) | ≤ 120 MeV/(mg/cm$^2$) 13/ |

10/ It is strongly recommended that CLK+/– be AC coupled with DEVCLK_LVPECL_EN set to 0 to allow CLK+/– to self bias to the optimal input common mode voltage for best performance. Manufacturer recommends AC coupling for SYSREF+/– unless DC coupling is required, in which case LVPECL input mode must be used (SYSREF_LVPECL_EN = 1).

11/ TMSTP+/– does not have internal biasing which requires TMSTP+/– to be biased externally whether AC coupled with TMSTP_LVPECL_EN = 0 or DC coupled with TMSTP_LVPECL_EN = 1.

12/ Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.

13/ Heavy ion testing facility was K500 Cyclotron Facility at TAMU and ion beam energy used 15 MeV/nucleon exposure. No single event latch-up (SEL) or single-event functional interrupt (SEFI) was observed when irradiated with ions beam at fluence 1x10$^7$ ions/cm$^2$ at angle with bias maximum operating voltage corresponding to an effective LET of 120 MeV·cm$^2$/mg. For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD204 – Serial Interface Standard for Data Converters.

JEP155 – Recommended ESD Target Levels for HBM/MM Qualification.

JEP157 – Recommended ESD-CDM Target Levels.

(Copies of these documents are available online at https://www.jedec.org).

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org).

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Analog inputs (INA+, INA–, INB+, INB–) | | | | | | | |
| Analog differential input full scale range | $V_{IN\_FSR}$ | Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) | 1, 2, 3 | 01 | 750 | 850 | $mV_{P-P}$ |
| Single-ended input resistance to AGND | $R_{IN}$ | Each input pin is terminated to AGND, measured at $T_A = 25°C$ | 1 | 01 | 48 | 52 | Ω |
| SERDES outputs (DA0+/DA0–...DA7+/DA7–, DB0+/DB0–...DB7+/DB7–) | | | | | | | |
| Differential output voltage, peak to peak | $V_{OD}$ | 100 Ω load | 1, 2, 3 | 01 | 550 | 650 | $mV_{P-P}$ |
| CMOS interface: SCLK, SDI, SDO, $\overline{SCS}$, PD, NCOA0, NCOA1, NCOB0, NCOB1, CALSTAT, CALTRIG, ORA0, ORA1, ORB0, ORB1, $\overline{SYNCSE}$ | | | | | | | |
| High level input current | $I_{IH}$ | | 1, 2, 3 | 01 | | 40 | µA |
| Low level input current | $I_{IL}$ | | 1, 2, 3 | 01 | -40 | | µA |
| High level output voltage | $V_{OH}$ | $I_{LOAD}$ = –400 µA | 1, 2, 3 | 01 | 1.65 | | V |
| Low level output voltage | $V_{OL}$ | $I_{LOAD}$ = +400 µA | 1, 2, 3 | 01 | | 150 | mV |
| Power consumption | | | | | | | |
| 1.9 V analog supply current | $I_{VA19}$ | Power mode 2: Single channel mode, JMODE 0 (8 lanes, DDC bypassed), foreground calibration | 1, 2, 3 | 01 | | 1000 | mA |
| 1.1 V analog supply current | $I_{VA11}$ | | 1, 2, 3 | 01 | | 650 | mA |
| 1.1 V digital supply current | $I_{VD11}$ | | 1, 2, 3 | 01 | | 850 | mA |
| Power dissipation | $P_D$ | | 1, 2, 3 | 01 | | 3.5 | W |
| AC specifications (Dual channel mode) | | | | | | | |
| Signal to noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs | SNR | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 51 | | dBFS |
| Signal to noise and distortion ratio, large signal, excluding DC and $F_S/2$ fixed spurs | SINAD | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 50 | | dBFS |
| Effective number of bits, large signal, excluding DC and $F_S/2$ fixed spurs | ENOB | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 8.0 | | bits |
| Spurious free dynamic range, large signal, excluding DC and $F_S/2$ fixed spurs | SFDR | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 58 | | dBFS |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $T_A = T_J$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| AC specifications (Dual channel mode) – continued. | | | | | | | |
| $F_S/2$ fixed interleaving spur, independent of input signal | $F_S/2$ | No input | 4, 5, 6 | 01 | | -50 | dBFS |
| Second order harmonic | HD2 | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -58 | dBFS |
| Third order harmonic | HD3 | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -58 | dBFS |
| $F_S/2$-$F_{IN}$ interleaving spur, signal dependent | $F_S/2$-$F_{IN}$ | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -58 | dBFS |
| Worst harmonic fourth order or higher | SPUR | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -60 | dBFS |
| AC specifications (Single channel mode) | | | | | | | |
| Signal to noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs | SNR | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 51 | | dBFS |
| Signal to noise and distortion ratio, large signal, excluding DC and $F_S/2$ fixed spurs | SINAD | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 43.9 | | dBFS |
| Effective number of bits, large signal, excluding DC and $F_S/2$ fixed spurs | ENOB | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 7.0 | | bits |
| Spurious free dynamic range, large signal, excluding DC, $F_S/4$ and $F_S/2$ fixed spurs | SFDR | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | 45 | | dBFS |
| $F_S/4$ fixed interleaving spur, independent of input signal | $F_S/4$ | No input | 4, 5, 6 | 01 | | -50 | dBFS |
| Second order harmonic | HD2 | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -58 | dBFS |
| Third order harmonic | HD3 | $f_{IN}$ = 2,482 MHz, $A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -58 | dBFS |

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

| Test | Symbol | Conditions 1/ 2/ 3/<br>$-55°C \le T_A \le +125°C$<br>$T_A = T_J$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| AC specifications (Single channel mode) – continued. | | | | | | | |
| $F_S/2-F_{IN}$ interleaving spur, signal dependent | $F_S/2-F_{IN}$ | $f_{IN}$ = 2,482 MHz,<br>$A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -45 | dBFS |
| $F_S/4\pm F_{IN}$ interleaving spurs, signal dependent | $F_S/4\pm F_{IN}$ | $f_{IN}$ = 2,482 MHz,<br>$A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -58 | dBFS |
| Worst harmonic fourth order or higher | SPUR | $f_{IN}$ = 2,482 MHz,<br>$A_{IN}$ = –1 dBFS | 4, 5, 6 | 01 | | -60 | dBFS |
| Device (sampling) clock (CLK+, CLK–) | | | | | | | |
| Maximum Input clock frequency (CLK+, CLK–), both single channel and dual channel modes 4/ | $f_{CLK, MAX}$ | | 4, 5, 6, 7, 8, 9, 10, 11 | 01 | | 3200 | MHz |
| Minimum Input clock frequency (CLK+, CLK–), both single channel and dual channel modes 4/ | $f_{CLK, MIN}$ | | 7, 9 | 01 | 800 | | MHz |
| Serial data outputs (DA0+...DA7+, DA0–...DA7–, DB0+...DB7+, DB0–...DB7–) | | | | | | | |
| Serialized output bit rate | $f_{SERDES}$ | | 9, 10, 11 | 01 | | 12.8 | Gbps |
| Serialized output unit interval | UI | | 9, 10, 11 | 01 | 78.125 | | ps |
| Serial programming interface (SDO) | | | | | | | |
| Delay from falling edge of SCLK cycle during read operation to SDO valid | $t_{(OD)}$ | | 9, 10, 11 | 01 | 1 | 10 | ns |

1/ Minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the Recommended Operating Conditions table; VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A =FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, $f_{IN}$ = 347 MHz, $A_{IN}$ = –1dBFS, $f_{CLK}$ =maximum-rated clock frequency, filtered 1-$V_{PP}$ sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted).

2/ For production testing of these parameters to the limits in Table I herein, ambient temperature ($T_A$) = junction temperature ($T_J$).

3/ Devices supplied to this drawing have been characterized through all levels M, P, L, R, and F of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C (see 1.5 herein).

4/ Unless functionally limited to a smaller range, based on programmed JMODE.

TABLE IB. SEP test limits. 1/ 2/ 3/

| Device type | SEP | Temperature | Effective Linear energy transfer (LET) |
|---|---|---|---|
| 01 | No SEL | 125°C | LET ≤ 120 MeV/(mg/cm$^2$) |
| | No SEFI | 125°C | LET ≤ 120 MeV/(mg/cm$^2$) |

1/ For single event phenomena (SEP) test conditions, see 4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Heavy ion testing facility was K500 Cyclotron Facility at TAMU and ion beam energy used 15 MeV/nucleon exposure. No single event latch-up (SEL) or single-event functional interrupt (SEFI) was observed when irradiated with ions beam at fluence 1x10$^7$ ions/cm$^2$ at angle with bias maximum operating voltage corresponding to an effective LET of 120 MeV·cm$^2$/mg. For more information on SEP test results, customers are requested to contact the manufacturer.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

Case X

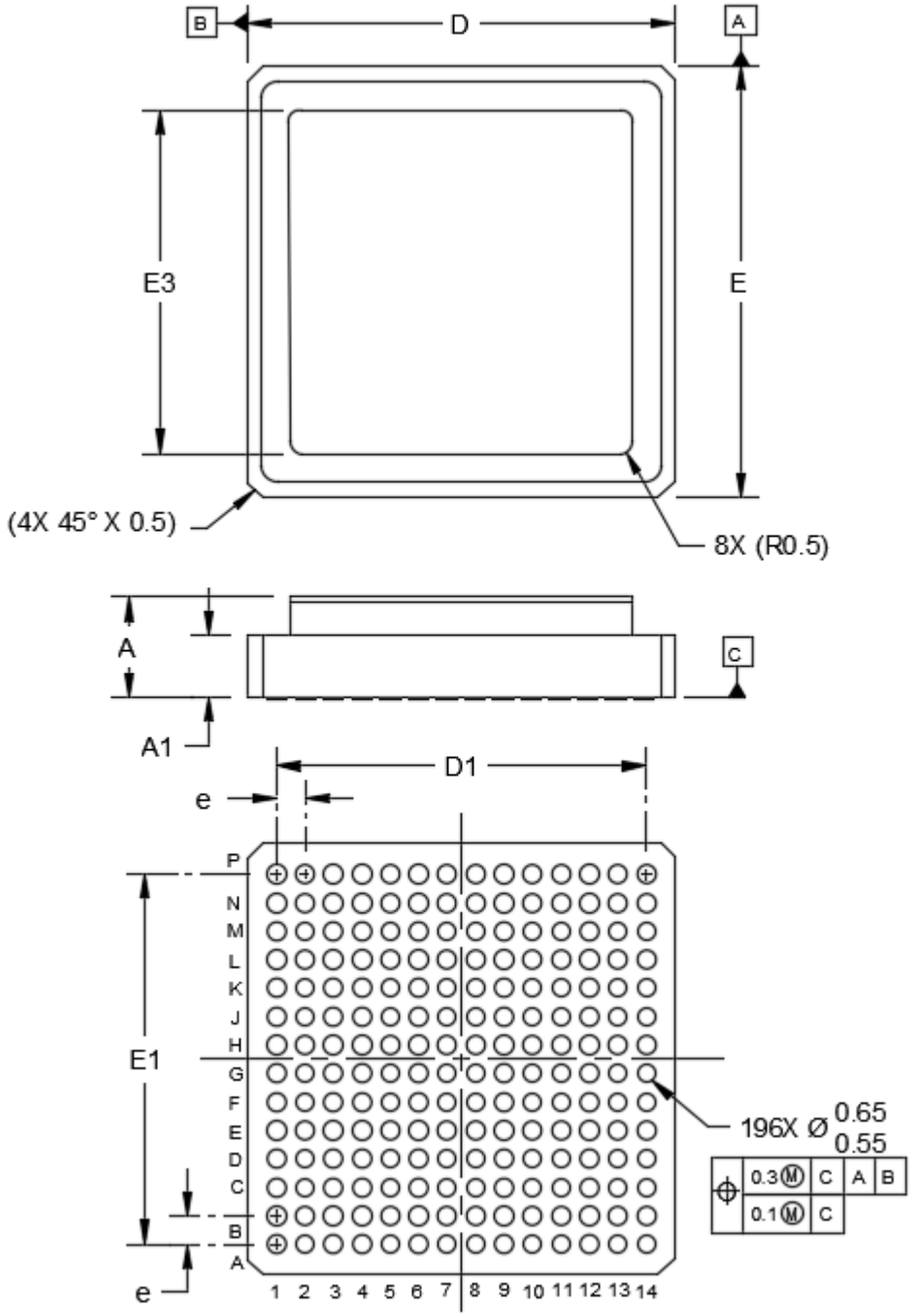



FIGURE 1. Case outline.

| STANDARD MICROCIRCUIT DRAWING<br>DLA LAND AND MARITIME<br>COLUMBUS, OHIO 43218-3990 | SIZE<br>A | | 5962-18209 |
|---|---|---|---|
| | | REVISION LEVEL<br>B | SHEET<br>10 |

Case X

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| A | ---- | 3.844 |
| A1 | 2.00 | 2.40 |
| D/E | 14.85 | 15.15 |
| D1/E1 | 13.00 BSC | |
| E3 | 11.85 | 12.15 |
| e | 1.000 BSC | |

FIGURE 1. Case outline – continued.

Case Y

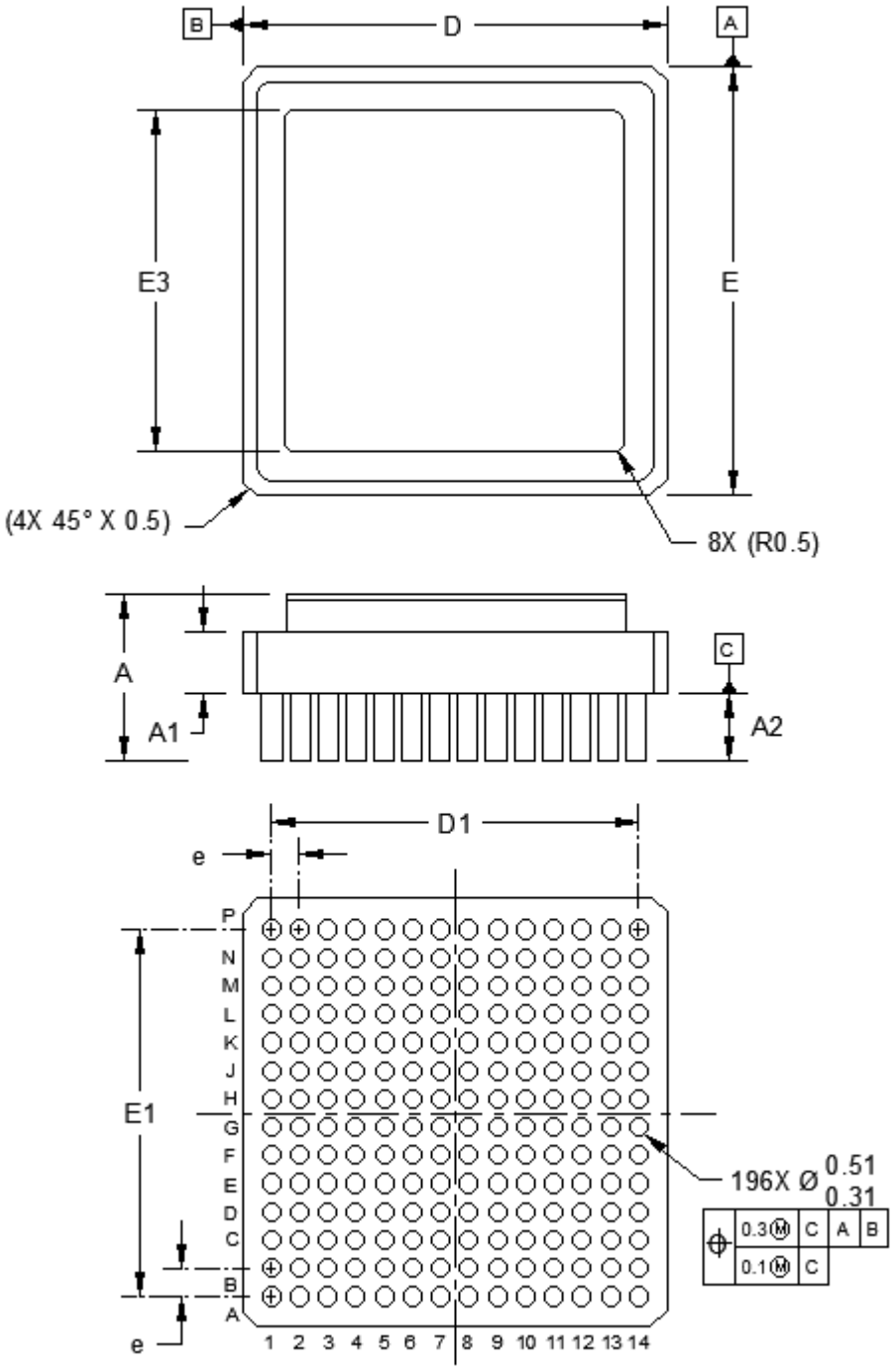



FIGURE 1. Case outline – continued.

Case Y

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| A | ---- | 6.194 |
| A1 | 2.00 | 2.40 |
| A2 | 2.05 | 2.35 |
| D/E | 14.85 | 15.15 |
| D1/E1 | 13.00 BSC | |
| E3 | 11.85 | 12.15 |
| e | 1.000 BSC | |

FIGURE 1. Case outline – continued.

| Device Type | 01 | Device Types | 01 | Device Types | 01 |
|---|---|---|---|---|---|
| Case Outline | X and Y | Case Outline | X and Y | Case Outline | X and Y |
| Terminal Symbol | Terminal Number | Terminal Symbol | Terminal Number | Terminal Symbol | Terminal Number |
| AGND | A1 | TMSTP- | D1 | CLK+ | G1 |
| BG | A2 | VA19 | D2 | AGND | G2 |
| AGND | A3 | VA11 | D3 | VA11 | G3 |
| INA+ | A4 | AGND | D4 | AGND | G4 |
| INA- | A5 | AGND | D5 | AGND | G5 |
| AGND | A6 | AGND | D6 | AGND | G6 |
| NCOA0 | A7 | AGND | D7 | AGND | G7 |
| ORA0 | A8 | DGND | D8 | DGND | G8 |
| CALTRIG | A9 | DGND | D9 | DGND | G9 |
| DA3+ | A10 | DGND | D10 | DGND | G10 |
| DA3- | A11 | DGND | D11 | DGND | G11 |
| DA2+ | A12 | VD11 | D12 | VD11 | G12 |
| DA2- | A13 | DA5- | D13 | $\overline{SCS}$ | G13 |
| DGND | A14 | DA1- | D14 | SCLK | G14 |
| AGND | B1 | VA19 | E1 | CLK- | H1 |
| $\overline{SYNCSE}$ | B2 | VA19 | E2 | AGND | H2 |
| AGND | B3 | VA11 | E3 | VA11 | H3 |
| AGND | B4 | AGND | E4 | AGND | H4 |
| AGND | B5 | AGND | E5 | AGND | H5 |
| AGND | B6 | AGND | E6 | AGND | H6 |
| NCOA1 | B7 | AGND | E7 | AGND | H7 |
| ORA1 | B8 | DGND | E8 | DGND | H8 |
| CALSTAT | B9 | DGND | E9 | DGND | H9 |
| DA7+ | B10 | DGND | E10 | DGND | H10 |
| DA7- | B11 | DGND | E11 | DGND | H11 |
| DA6+ | B12 | VD11 | E12 | VD11 | H12 |
| DA6- | B13 | DA4+ | E13 | SDI | H13 |
| DGND | B14 | DA0+ | E14 | SDO | H14 |
| TMSTP+ | C1 | AGND | F1 | AGND | J1 |
| VA19 | C2 | VA11 | F2 | VA11 | J2 |
| VA19 | C3 | VA11 | F3 | VA11 | J3 |
| VA19 | C4 | AGND | F4 | AGND | J4 |
| VA19 | C5 | AGND | F5 | AGND | J5 |
| AGND | C6 | AGND | F6 | AGND | J6 |
| AGND | C7 | AGND | F7 | AGND | J7 |
| DGND | C8 | DGND | F8 | DGND | J8 |
| DGND | C9 | DGND | F9 | DGND | J9 |
| VD11 | C10 | DGND | F10 | DGND | J10 |
| VD11 | C11 | DGND | F11 | DGND | J11 |
| VD11 | C12 | VD11 | F12 | VD11 | J12 |
| DA5+ | C13 | DA4- | F13 | DB4- | J13 |
| DA1+ | C14 | DA0- | F14 | DB0- | J14 |

FIGURE 2. Terminal connections.

| Device Type | 01 | Device Types | 01 |
|---|---|---|---|
| Case Outline | X and Y | Case Outline | X and Y |
| Terminal Symbol | Terminal Number | Terminal Symbol | Terminal Number |
| VA19 | K1 | AGND | N1 |
| VA19 | K2 | TDIODE+ | N2 |
| VA11 | K3 | AGND | N3 |
| AGND | K4 | AGND | N4 |
| AGND | K5 | AGND | N5 |
| AGND | K6 | AGND | N6 |
| AGND | K7 | NCOB1 | N7 |
| DGND | K8 | ORB1 | N8 |
| DGND | K9 | DGND | N9 |
| DGND | K10 | DB7+ | N10 |
| DGND | K11 | DB7- | N11 |
| VD11 | K12 | DB6+ | N12 |
| DB4+ | K13 | DB6- | N13 |
| DB0+ | K14 | DGND | N14 |
| SYSREF+ | L1 | AGND | P1 |
| VA19 | L2 | TDIOD- | P2 |
| VA11 | L3 | AGND | P3 |
| AGND | L4 | INB+ | P4 |
| AGND | L5 | INB- | P5 |
| AGND | L6 | AGND | P6 |
| AGND | L7 | NCOB0 | P7 |
| DGND | L8 | ORB0 | P8 |
| DGND | L9 | PD | P9 |
| DGND | L10 | DB3+ | P10 |
| DGND | L11 | DB3- | P11 |
| VD11 | L12 | DB2+ | P12 |
| DB5- | L13 | DB2- | P13 |
| DB1- | L14 | DGND | P14 |
| SYSREF- | M1 | | |
| VA19 | M2 | | |
| VA19 | M3 | | |
| VA19 | M4 | | |
| VA19 | M5 | | |
| AGND | M6 | | |
| AGND | M7 | | |
| DGND | M8 | | |
| DGND | M9 | | |
| VD11 | M10 | | |
| VD11 | M11 | | |
| VD11 | M12 | | |
| DB5+ | M13 | | |
| DB1+ | M14 | | |

FIGURE 2. Terminal connections – Continued.

| PIN | | I/O | Description |
|---|---|---|---|
| Terminal symbol | Terminal number | | |
| AGND | A1, A3, A6, B1, B3, B4, B6, B6, C6, C7, D4, D5, D6, D7, E4, E5, E6, E7, F1, F4, F5, F6, F7, G2, G4, G5, G6, G7, H2, H4, H5, H6, H7, J1, J4, J5, J6, J7, K4, K5, K6, K7, L4, L5, L6, L7, M6, M7, N1, N3, N4, N5, N6, P1, P3, P6 | — | Analog supply ground. AGND and DGND should be directly connected on circuit board. |
| DGND | A14, B14, C8, C9, D8, D9, D10, D11, E8, E9, E10, E11, F8, F9, F10, F11, G8, G9, G10, G11, H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, M8, M9, N9, N14, P14 | — | Digital supply ground. AGND and DGND should be directly connected on circuit board. |
| BG | A2 | O | Bandgap voltage output. This pin is capable of sourcing 100 µA and can drive a load up to 80 pF. See manufacturer's datasheet for more details. This pin can be left disconnected if not used. |
| CALSTAT | B9 | O | Foreground calibration status output or device alarm output. Functionality is programmed through CAL_STATUS_SEL. This pin can be left disconnected if not used. |
| CALTRIG | A9 | I | Foreground calibration trigger input. This pin is only used if hardware calibration triggering is selected in CAL_TRIG_EN, otherwise software triggering is performed using CAL_SOFT_TRIG. This pin should be tied to GND if not used. |

FIGURE 2. Terminal connections – Continued.

| PIN | | I/O | Description |
|---|---|---|---|
| Terminal symbol | Terminal number | | |
| CLK+ | G1 | I | Device (sampling) clock positive input. The clock signal must be AC coupled to this input. In single-channel mode, the analog input signal is sampled on both rising and falling edges. In dual-channel mode, the analog signal is sampled on the rising edge. This differential input has an internal untrimmed 100-Ω differential termination and is self-biased to the optimal input common mode voltage. |
| CLK- | H1 | I | Device (sampling) clock negative input. Must be AC coupled. |
| DA0+ | E14 | O | High-speed serialized-data output for channel A, lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA0- | F14 | O | High-speed serialized-data output for channel A, lane 0, negative connection. This pin can be left disconnected if not used. |
| DA1+ | C14 | O | High-speed serialized-data output for channel A, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA1- | D14 | O | High-speed serialized-data output for channel A, lane 1, negative connection. This pin can be left disconnected if not used. |
| DA2+ | A12 | O | High-speed serialized-data output for channel A, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA2- | A13 | O | High-speed serialized-data output for channel A, lane 2, negative connection. This pin can be left disconnected if not used. |
| DA3+ | A10 | O | High-speed serialized-data output for channel A, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA3- | A11 | O | High-speed serialized-data output for channel A, lane 3, negative connection. This pin can be left disconnected if not used. |
| DA4+ | E13 | O | High-speed serialized-data output for channel A, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA4- | F13 | O | High-speed serialized-data output for channel A, lane 4, negative connection. This pin can be left disconnected if not used. |
| DA5+ | C13 | O | High-speed serialized-data output for channel A, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA5- | D13 | O | High-speed serialized-data output for channel A, lane 5, negative connection. This pin can be left disconnected if not used. |
| DA6+ | B12 | O | High-speed serialized-data output for channel A, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA6- | B13 | O | High-speed serialized-data output for channel A, lane 6, negative connection. This pin can be left disconnected if not used. |

FIGURE 2. Terminal connections – Continued.

| PIN | | I/O | Description |
|---|---|---|---|
| Terminal symbol | Terminal number | | |
| DA7+ | B10 | O | High-speed serialized-data output for channel A, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DA7- | B11 | O | High-speed serialized-data output for channel A, lane 7, negative connection. This pin can be left disconnected if not used. |
| DB0+ | K14 | O | High-speed serialized-data output for channel B, lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB0- | J14 | O | High-speed serialized-data output for channel B, lane 0, negative connection. This pin can be left disconnected if not used. |
| DB1+ | M14 | O | High-speed serialized-data output for channel B, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB1- | L14 | O | High-speed serialized-data output for channel B, lane 1, negative connection. This pin can be left disconnected if not used. |
| DB2+ | P12 | O | High-speed serialized-data output for channel B, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB2- | P13 | O | High-speed serialized-data output for channel B, lane 2, negative connection. This pin can be left disconnected if not used. |
| DB3+ | P10 | O | High-speed serialized-data output for channel B, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB3- | P11 | O | High-speed serialized-data output for channel B, lane 3, negative connection. This pin can be left disconnected if not used. |
| DB4+ | K13 | O | High-speed serialized-data output for channel B, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB4- | J13 | O | High-speed serialized-data output for channel B, lane 4, negative connection. This pin can be left disconnected if not used. |
| DB5+ | M13 | O | High-speed serialized-data output for channel B, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB5- | L13 | O | High-speed serialized-data output for channel B, lane 5, negative connection. This pin can be left disconnected if not used. |

FIGURE 2. Terminal connections – Continued.

| PIN | | I/O | Description |
|---|---|---|---|
| Terminal symbol | Terminal number | | |
| DB6+ | N12 | O | High-speed serialized-data output for channel B, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100 Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB6- | N13 | O | High-speed serialized-data output for channel B, lane 6, negative connection. This pin can be left disconnected if not used. |
| DB7+ | N10 | O | High-speed serialized-data output for channel B, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. |
| DB7- | N11 | O | High-speed serialized-data output for channel B, lane 7, negative connection. This pin can be left disconnected if not used. |
| INA+ | A4 | I | Channel A analog input positive connection. The differential full-scale input range is determined by the full-scale voltage adjust register. The input common mode voltage should be set to AGND. This input is terminated to ground through a 50 Ω termination resistor. Use of INA is recommended for single-channel mode due to optimized performance. This pin can be left disconnected if not used. |
| INA- | A5 | I | Channel A analog input negative connection. This input is terminated to ground through a 50 Ω termination resistor. Use of INA is recommended for single-channel mode due to optimized performance. This pin can be left disconnected if not used. |
| INB+ | P4 | I | Channel B analog input positive connection. The differential full-scale input range is determined by the full-scale voltage adjust register. The input common mode voltage should be set to AGND. This input is terminated to ground through a 50 Ω termination resistor. This pin can be left disconnected if not used. |
| INB- | P5 | I | Channel B analog input negative connection. This input is terminated to ground through a 50 Ω termination resistor. This pin can be left disconnected if not used. |
| NCOA0 | A7 | I | NCO accumulator selection control LSB for DDC A. NCOA0 and NCOA1 select which NCO, of a possible four NCOs, is used for digital mixing. The remaining unselected NCOs continue to run to maintain phase coherency and can be swapped in by changing the values of NCOA0 and NCOA1. This is an asynchronous input. This pin should be tied to GND if not used. |
| NCOA1 | B7 | I | NCO accumulator selection control MSB for DDC A. This pin should be tied to GND if not used. |
| NCOB0 | P7 | I | NCO accumulator selection control LSB for DDC B. NCOB0 and NCOB1 select which NCO, of a possible four NCOs, is used for digital mixing. The remaining unselected NCOs continue to run to maintain phase coherency and can be swapped in by changing the values of NCOB0 and NCOB1. This is an asynchronous input. This pin should be tied to GND if not used. |
| NCOB1 | N7 | I | NCO accumulator selection control MSB for DDC B. This pin should be tied to GND if not used. |
| ORA0 | A8 | O | Fast over range detection status for channel A for T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used. |

FIGURE 2. Terminal connections – Continued.

| PIN | | I/O | Description |
|---|---|---|---|
| Terminal symbol | Terminal number | | |
| ORA1 | B8 | O | Fast over range detection status for channel A for T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used. |
| ORB0 | P8 | O | Fast over range detection status for channel B for T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used. |
| ORB1 | N8 | O | Fast over range detection status for channel B for T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used. |
| PD | P9 | I | Power down input. This pin disables all analog circuits and serializer outputs when set high to save power. This pin should be tied to AGND if not used. Important note: Power Down (via PD input or MODE setting) cannot be used for extended periods of time unless the powered down channels will never be used. Long term use of Power Down will degrade the JESD204B serializer clock path and prevent operation at high bit rates. 1/ |
| SCLK | G14 | I | Serial interface clock. This pin functions as the serial-interface clock input which clocks the serial programming data in and out. See manufacturer's datasheet for more information. Supports 1.1 V and 1.8 V CMOS levels. |
| $\overline{SCS}$ | G13 | I | Serial interface chip select active low input. See manufacturer's datasheet for more information. Supports 1.1 V and 1.8 V CMOS levels. This pin has an 82 kΩ pull-up resistor to VD11. |
| SDI | H13 | I | Serial interface data input. See manufacturer's datasheet for more information. Supports 1.1 V and 1.8 V CMOS levels. |
| SDO | H14 | O | Serial interface data output. See manufacturer's datasheet for more information. This pin is high impedance during normal device operation. This pin outputs 1.9 V CMOS levels during serial interface read operations. This pin can be left disconnected if not used. |

1/ Powering down the high-speed data outputs (DA0± ... DA7±, DB0± ... DB7±) for extended times may damage the output serializers, especially at high data rates. Powering down the serializers occurs when the PD pin is held high, the MODE register is programmed to a value other than 0x00 or 0x01, the PD_ACH or PD_BCH registers settings are programmed to 1, or when the JMODE register setting is programmed to a mode that uses less than the 16 total lanes that the device allows. For instance, JMODE 0 uses eight total lanes and therefore the four highest-indexed lanes for each JESD204B link (DA4± ... DA7±, DB4± ... DB7±) are powered down in this mode. When the PD pin is held high or the MODE register is programmed to a value other than 0x00 or 0x01, all output serializers are powered down. When the PD_ACH or PD_BCH register settings are programmed to 1, the associated ADC channel and lanes are powered down. To prevent unreliable operation, the PD pin and MODE register must only be used for brief periods of time to measure temperature diode offsets and not used for long-term power savings. Furthermore, using a JMODE that uses fewer than 16 lanes results in unreliable operation of the unused lanes. If the system will never use the unused lanes during the lifetime of the device, then the unused lanes do not cause issues and can be powered down. If the system may make use of the unused lanes at a later time, the reliable operation of the serializer outputs can be maintained by enabling JEXTRA_A and JEXTRA_B, which results in the VD11 power consumption to increase and the output serializers to toggle.

FIGURE 2. Terminal connections – Continued.

| PIN | | I/O | Description |
|---|---|---|---|
| Terminal symbol | Terminal number | | |
| $\overline{\text{SYNCSE}}$ | B2 | I | JESD204B SYNC signal single-ended active low input. This pin provides the JESD204B- required synchronization request input. A logic low applied to this input initiates code group synchronization and the initial lane alignment sequence. The choice of single-ended or differential $\overline{\text{SYNC}}$ (using TMSTP+ and TMSTP- pins) is selected by programming SYNC_SEL. This pin should be tied to GND if differential $\overline{\text{SYNC}}$ (TMSTP±) is as the JESD204B SYNC signal. |
| SYSREF+ | L1 | I | SYSREF positive input used to achieve synchronization and deterministic latency across the JESD204B interface. This differential input (SYSREF+ to SYSREF–) has an internal untrimmed 100-Ω differential termination. It is self-biased when AC coupled (SYSREF_LVPECL_EN must be set to 0), but can be DC coupled by setting SYSREF_LVPECL_EN to 1 which changes the internal termination to untrimmed 50 Ω single-ended termination to ground on each SYSREF+ and SYSREF- input. The common mode voltage must be within the recommended range when DC coupled. |
| SYSREF- | M1 | I | SYSREF negative input. |
| TDIODE+ | N2 | I | Temperature diode positive (anode) connection. An external temperature sensor can be connected to TDIODE+ and TDIODE- to monitor the junction temperature of the device. This pin can be left disconnected if not used. |
| TDIODE- | P2 | I | Temperature diode negative (cathode) connection. This pin can be left disconnected if not used. |
| TMSTP+ | C1 | I | Timestamp input positive connection or differential JESD204B $\overline{\text{SYNC}}$ positive connection. This input is used as the timestamp input when SYNC_SEL is set to use $\overline{\text{SYNCSE}}$ as the JESD204B SYNC signal. This input is used as the JESD204B SYNC signal when SYNC_SEL is set to use TMSTP+ and TMSTP- as the JESD204B SYNC signal. For additional usage information as timestamp input, see manufacturer's datasheet. This pin can be left disconnected if $\overline{\text{SYNCSE}}$ is used and timestamp is not required. |
| TMSTP- | D1 | I | Timestamp input positive connection or differential JESD204B $\overline{\text{SYNC}}$ negative connection. This pin can be left disconnected if $\overline{\text{SYNCSE}}$ is used and timestamp is not required. |
| VA11 | D3, E3, F2, F3, G3, H3, J2, J3, K3, L3 | I | 1.1-V analog supply. |
| VA19 | C2, C3, C4, C5, D2, E1, E2, K1, K2, L2, M2, M3, M4, M5 | I | 1.9-V analog supply. |
| VD11 | C10, C11, C12, D12, E12, F12, G12, H12, J12, K12, L12, M10, M11, M12 | I | 1.1-V digital supply. |

FIGURE 2. Terminal connections – Continued.

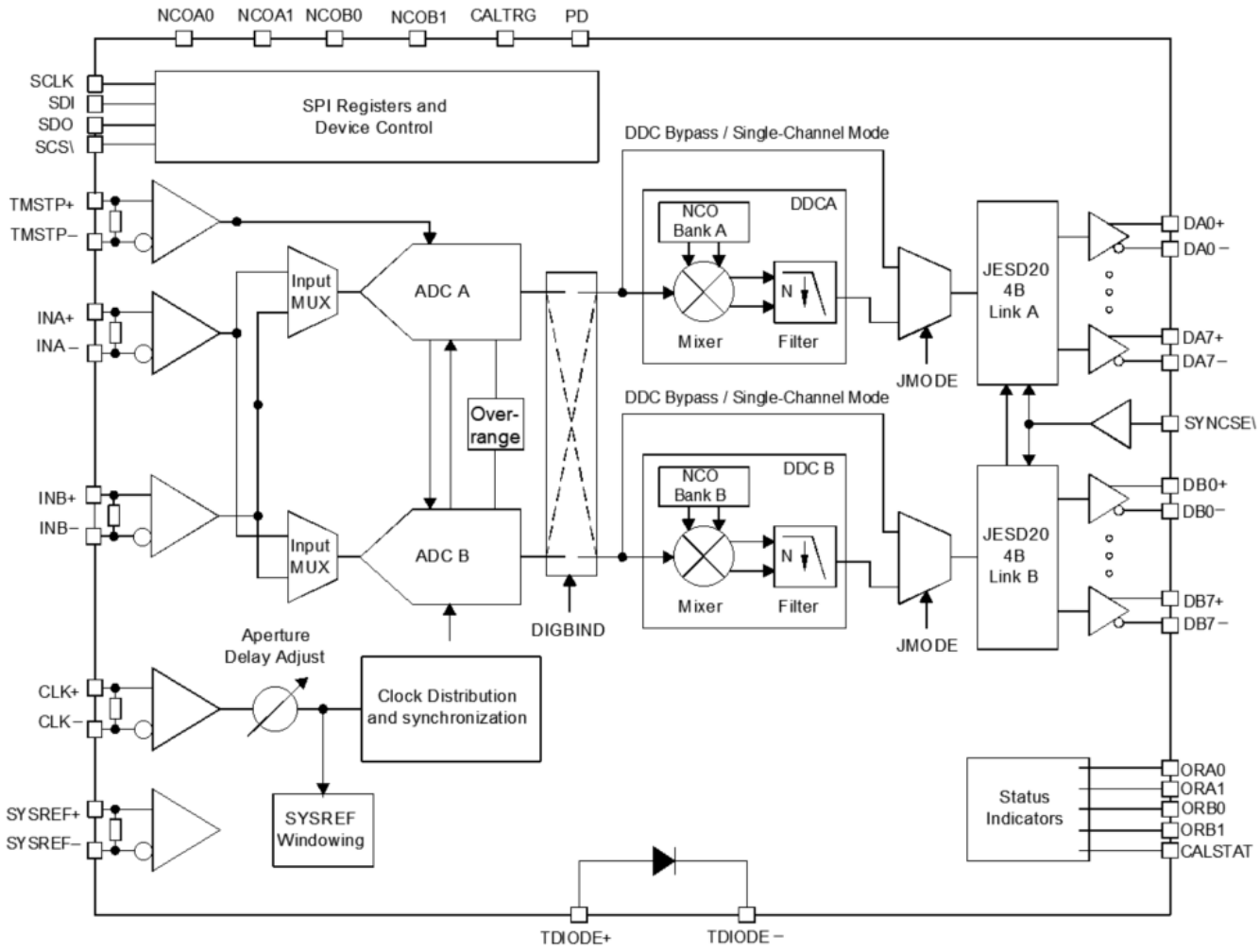



FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|
| | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | 1,4,7,9 | 1,4,7,9 |
| Final electrical parameters (see 4.2) | 1,2,3,4,5,6,7,8, 9,10,11 1/ 2/ | 1,2,3,4,5,6,7,8,9, 10,11 1/ 2/ |
| Group A test requirements (see 4.4) | 1,2,3,4,5,6,7,8, 9,10,11 2/ | 1,2,3,4,5,6,7,8,9, 10,11 2/ |
| Group C end-point electrical parameters (see 4.4) | 1,2,3,4,5,6,7,8, 9,10,11 2/ | 1,2,3,4,5,6,7,8,9, 10,11 2/ |
| Group D end-point electrical parameters (see 4.4) | 1,4,7,9 | 1,4,7,9 |
| Group E end-point electrical parameters (see 4.4) | 1,4,7,9 | 1,4,7,9 |

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in Table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. 1/

| Parameters | Symbol | Typical Value | Delta limits |
|---|---|---|---|
| VA19 Supply Current, Power Mode 2 | $I_{VA19, PM2}$ | 890 mA | +/- 25 mA |
| VA11 Supply Current, Power Mode 2 | $I_{VA11, PM2}$ | 500 mA | +/- 25 mA |
| VD11 Supply Current, Power Mode 2 | $I_{VD11, PM2}$ | 595 mA | +/- 25 mA |
| SNR, Single Channel Mode | $SNR_{SINGLE}$ | 55 dBFS | +/- 2 dBFS |
| SNR, Dual Channel Mode | $SNR_{DUAL}$ | 54.9 dBFS | +/- 2 dBFS |
| High level input current (SCSb) | $I_{IH, SCSb}$ | +15 µA | +/- 1 µA |
| High level input current (All other CMOS pins) | $I_{IH}$ | +100 nA | +/- 10 nA |
| Low level input current (SCSb) | $I_{IL, SCSb}$ | -15 µA | +/- 1 µA |
| Low level input current (All other CMOS pins) | $I_{IL}$ | -100 nA | +/- 10 nA |

1/ 240 hour burn in and group C end point electrical parameters.
Deltas are performed at $T_A$ = +25°C.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ $10^7$ ions/cm$^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/cm$^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be $T_J$=125°C for SEL test.

f. For SEL test limits, see table IB herein.

g. For SEFI test limits, see table IB herein

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-02-09

Approved sources of supply for SMD 5962-18209 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/ .

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962F1820901VXC | 01295 | ADC12DJ3200-SP |
| 5962F1820901VYF | 01295 | ADC12DJ3200-SP |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Ln.<br>PO Box 660199<br>Dallas, TX 75243 |