REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current MIL-PRF-38535 requirements. - rrp	24-01-22	J. ESCHMEYER

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

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COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
18-12-13

REVISION LEVEL
A

MICROCIRCUIT, CMOS DIGITAL-LINEAR, DUAL CHANNEL, 14 BIT, 40 MSPS ANALOG FRONT END WITH LVDS OUTPUT, MONOLITHIC SILICON

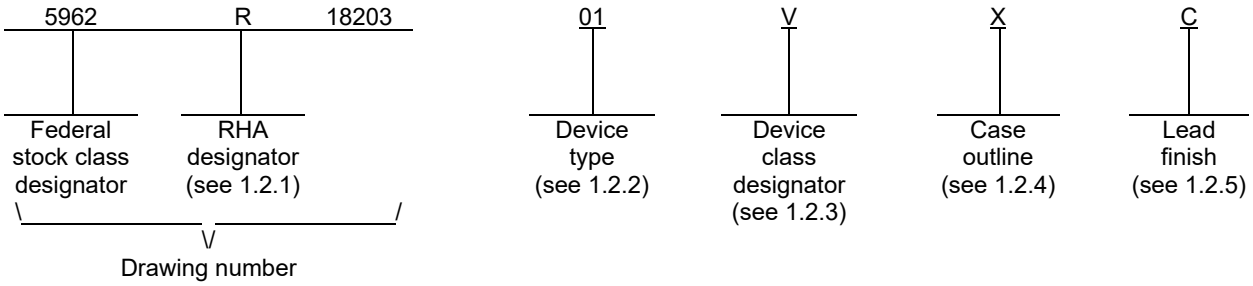
SIZE	CAGE CODE	
A	**67268**	**5962-18203**

SHEET 1 OF 26

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LM98640	Radiation hardened, dual channel, 14 bit, 40 mega samples per second (MSPS) analog front end with low voltage differential signaling (LVDS) output

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Ceramic quad flat pack (CQFP) with exposed pad

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage (VDD33)	4.2 V maximum
Supply voltage (VDD18)	2.35 V maximum
Voltage on any VDD33 input pin (not to exceed 4.2 V)	-0.3 V to VDD33 + 0.3 V
Voltage on any VDD33 output pin (not to exceed 4.2 V)	-0.3 V to VDD33 + 0.3 V
Voltage on any VDD18 input or output pin (33 to 52) (not to exceed 2.35 V)	-0.3 V to VDD18 + 0.3 V
Input current at any pin other than supply pins	±25 mA maximum 3/
Package input current (except supply pins)	±50 mA maximum 3/
Maximum junction temperature (T_J)	150°C
Storage temperature range	-65°C to +150°C
Electrostatic discharge (ESD) rating: 4/	
Human body model (HDM) per JEDEC JS-001	2500 V 5/
Charge device model (CDM) per JEDEC JESD22-C101	250 V 6/
Thermal resistance, junction-to-case, top ($\theta_{JC,top}$)	3.8°C/W
Thermal resistance, junction-to-case, bottom ($\theta_{JC,bottom}$)	0.3°C/W
Thermal resistance, junction-to-bottom (θ_{JB})	7.6°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	16.4°C/W
Characterization parameter, junction-to-top (ψ_{JT})	1.7°C/W
Characterization parameter, junction-to-top (ψ_{JB})	7.2°C/W

1.4 Recommended operating conditions.

Supply voltage (VDD33)	+3.15 V to +3.45 V 2/ 3/
Supply voltage (VDD18)	+1.7 V to +1.9 V 2/ 3/
Absolute supply return voltage |VSS33 – VSS18 |	100 mV maximum
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are measured with respect to VSS = 0 V.
3/ When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < VSS$ or $V_{IN} > VDD33$), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.
4/ Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0 Ω.
5/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2500 V may actually have higher performance.
6/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rad(Si)/s) ..... 100 krad(Si) 7/

Single event phenomenon (SEP):
No Single event latchup (SEL) occurs at effective LET (see 4.4.4.2) ..... ≤ 120 MeV/(mg/cm^2) 8/
No Single event functional interrupt occurs at an effective LET (see 4.4.4.2) ..... ≤ 120 MeV/(mg/cm^2) 8/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

7/ Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.

8/ Heavy ion testing facility was 88” Cyclotron Facility at Lawrence Berkeley National Laboratory (LBNL) located in Berkeley, California and ion beam energy was 4.5 MeV/nucleon exposed inside a vacuum chamber. No single event latch-up (SEL) or single-event functional interrupt (SEFI) was observed when irradiated with Bismuth(Bi) ions at fluence 1x10^7 ions/cm^2 at an angle 35° with bias voltage 1.8 V and 3.3 V corresponding to an effective LET of 120 MeV/(mg/cm^2). For more information on SEP test results, customers are requested to contact the manufacturer.

2.2 Non-Government publications. The following document form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIOINAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) induced by Heavy Ion Irradiation of Semiconductor Devices

(Copies of this document is available online at https://www.astm.org/).

JEDEC Solid State Technology Association

JEDEC JS-001	–	Human Body Model Testing of Integrated Circuits
JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	–	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	–	Recommended ESD-CDM Target Levels

(Copies of this document is available online at https://www.jedec.org).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing diagrams. The timing diagrams shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.6 Passive elements requirements. Discrete capacitors, that are included as an integral part of the microcircuit design shall be used to improve the microcircuit performance in areas of decoupling, signal conditioning, noise conditioning or radiation hardened assurance performance. Discrete capacitors that are internally or externally utilized as part of QML microcircuits shall be evaluated/qualified in accordance to the paragraph 3.15 of MIL-PRF-38535. Microcircuit manufacturer shall document capacitors evaluation/qualification test methodology to their QM plan and the processes used concerning the capacitors.

3.2.6.1 Capacitors use: These devices are being assembled with five internal C1 through C5 precious metal electrode (PME) 0201 gold terminated bypass capacitors with capacitance value 10 nF and voltage 10 V, which meet approved criteria in accordance with MIL-PRF-123 or as approved by the qualifying activity.

The capacitors are placed in the following locations, between

1. VDD33 (pins 2, 3) and VSS33 (pins 4, 5)
2. VSS33 (pins 13, 14) and VDD33 (pins 15, 16)
3. VREFB2 (pin 18) and VREFT2 (pin 19)
4. VDD18 (pins 53, 54) and VSS18 (pin 55, 56)
5. VREFT1 (pin 67) and VREFB1 (pin 68)

See block diagram figure 3 for more details.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CMOS digital input dc specifications		(SCLK, $\overline{SEN}$, SDI, CLPIN)					
Logical 1 input voltage	V_{IH}		1,2,3	01	2.0		V
Logical 0 input voltage	V_{IL}		1,2,3	01		0.8	V
Logical 1 input current	I_{IH}	CLPIN	1,2,3	01		100	µA
V_{IH} = VDD33		SCLK, SDI				300	nA
		$\overline{SEN}$				6	µA
Logical 0 input current	I_{IL}	CLPIN	1,2,3	01	-300		nA
V_{IL} = VSS		SCLK, SDI			-300		nA
		$\overline{SEN}$			-100		µA
CMOS digital output dc specification (SDO)							
Logical 1 output voltage	V_{OH}	I_{OUT} = -0.5 mA	1,2,3	01	1.8		V
Logical 0 output voltage	V_{OL}	I_{OUT} = 1.6 mA	1,2,3	01		0.2	V
Output leakage current	I_{OH}	V_{OUT} = VDD	1,2,3	01		50	nA
Output leakage current	I_{OL}	V_{OUT} = VSS	1,2,3	01	-50		nA
LVDS clock receiver dc specifications		(INCLK+ and INCLK- pins)					
Differential LVDS clock high threshold voltage	V_{IHL}	V_{CM} (LVDS input common mode voltage) = 1.25 V, R_L = 100 Ω	1,2,3	01		250	mV
Differential LVDS clock low threshold voltage	V_{ILL}	V_{CM} (LVDS input common mode voltage) = 1.25 V, R_L = 100 Ω	1,2,3	01	-250		mV
Differential LVDS clock input current	I_{IHL}	V_{IH} = VDD33	1,2,3	01		100	µA
Differential LVDS clock input current	I_{ILL}	V_{IL} = VSS	1,2,3	01	-49		µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LVDS output dc specifications							
Differential output voltage	V_{OD}	LVDS output modes =	1,2,3	01	210	410	mV
LVDS output offset voltage	V_{OS}	0000 x 100, R_L = 100 Ω	1,2,3	01	1.05	1.3	V
Differential output voltage	V_{OD}	LVDS output modes =	1,2,3	01	250	460	mV
LVDS output offset voltage	V_{OS}	0000 x 101, R_L = 100 Ω	1,2,3	01	1.05	1.3	V
Differential output voltage	V_{OD}	LVDS output modes =	1,2,3	01	300	535	mV
LVDS output offset voltage	V_{OS}	0000 x 110, R_L = 100 Ω	1,2,3	01	.95	1.2	V
Differential output voltage	V_{OD}	LVDS output modes =	1,2,3	01	350	590	mV
LVDS output offset voltage	V_{OS}	0000 x 111, R_L = 100 Ω	1,2,3	01	.95	1.2	V
LVDS output leakage current	I_{OH}		1,2,3	01		5	µA
LVDS output leakage current	I_{OL}		1,2,3	01	-5		µA
Output short circuit current	I_{OS}	V_{OUT} = 0 V, R_L = 100 Ω	1,2,3	01		50	mA
Power supply specifications							
VDD33 analog supply current,	IA	Powerdown control reg = 0x00					
dual channel, power optimized		5 MHz	1,2,3	01		58	mA
for PGA gain = 1 – 4x		40 MHz				98	
VDD33 analog supply current,	IA	Powerdown control reg = 0x00					
dual channel, power optimized		5 MHz	1,2,3	01		58	mA
for PGA gain = 1 – 8x		40 MHz				103	
VDD33 analog supply current, single channel, power optimized for PGA gain = 1 – 4x	IA	Powerdown control reg = = 0 x 15 (CH1 PD) or = 0 x 2A (CH2 PD)	1,2,3	01			
		5 MHz				35	mA
		40 MHz				60	
VDD33 analog supply current, single channel, power optimized for PGA gain = 1 – 8x	IA	Powerdown control reg = = 0 x 15 (CH1 PD) or = 0 x 2A (CH2 PD)	1,2,3	01			
		5 MHz				35	mA
		40 MHz				64	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply specifications – continued.							
VDD33 analog supply current powerdown	IA	Powerdown control register = 0 x 80	1,2,3	01		3.85	mA
VDD18 digital supply current		5 MHz	1,2,3	01		29	mA
		40 MHz				37	
VDD18 digital supply current powerdown	ID	Powerdown control register = 0 x 80	1,2,3	01		3.0	mA
Average power dissipation Power optimized for PGA gain = 1-4x, dual channel, LVDS dual lane mode	PWR	5 MHz	1,2,3	01		244	mW
		40 MHz				390	
Average power dissipation Power optimized for PGA gain = 1-8x, dual channel, LVDS dual lane mode	PWR	5 MHz	1,2,3	01		244	mW
		40 MHz				407	
Input sampling circuit specifications							
Input voltage level	V_{IN}	CDS gain = 1x, PGA gain = 1x	1,2,3	01		2	Vp-p
		CDS gain = 2x, PGA gain = 1x				1	
VCLP reference circuit specification							
VCLP DAC resolution			1,2,3	01	5		Bits
VCLP DAC step size			1,2,3	01	96	102	mV
VCLP DAC voltage minimum output	V_{VCLP}	VCLP control register = 0110 0000	1,2,3	01	194	298	mV
VCLP DAC voltage maximum output	V_{VCLP}	VCLP control register = 0111 1101	1,2,3	01	2.99	3.11	mV

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Coarse analog offset DAC specifications							
Offset adjustment range referred to AFE input CDS gain = 1x		Minimum DAC code = 0 x 000	1,2,3	01	-264	-251	mV
		Maximum DAC code = 0 x 1FF			251	266	
Offset adjustment range referred to AFE input CDS gain = 2x		Minimum DAC code = 0 x 000	1,2,3	01	-132	-126	mV
		Maximum DAC code = 0 x 1FF			126	133	
Offset adjustment range referred to AFE output		Minimum DAC Code = 0 x 000	1,2,3	01	-2162	-2058	LSB
		Maximum DAC Code = 0 x 1FF			2058	2176	
Differential non-linearity	DNL	CDS = gain = 1x or 2x 40 MHz	1,2,3	01	-1.1	1.1	LSB
Integral non-linearity	INL	CDS = gain = 1x or 2x 40 MHz	1,2,3	01	-2.8	2.80	LSB
Fine analog offset DAC specifications							
Offset adjustment range referred to AFE input CDS gain = 1x		Minimum DAC code = 0x000	1,2,3	01	-5.9	-3.1	mV
		Maximum DAC code = 0x1FF			4.3	6.8	
Offset adjustment range referred to AFE input CDS gain = 2x		Minimum DAC code = 0x000	1,2,3	01	-2.9	-1.5	mV
		Maximum DAC code = 0x1FF			2.1	3.4	
Offset adjustment range referred to AFE output		Minimum DAC Code = 0x000	1,2,3	01	-48	-25	LSB
		Maximum DAC Code = 0x1FF			35	56	
PGA specifications							
Gain resolution			1,2,3	01		8	Bits
Maximum gain		CDS gain = 1x	1,2,3	01	7.92	8.78	V/V
					17.99	18.88	dB
Minimum gain		CDS gain = 1x	1,2,3	01	0.62	0.66	V/V
					-4.15	-3.54	dB
PGA function	Gain (V/V) = (180/(277-PGA code)) Gain (dB) = 20LOG10 (180/(277-PGA code))						
Channel matching		Minimum PGA gain	1,2	01	95.2%		
			3		94.0%		
		Maximum PGA gain	1,2		95.2%		
			3		94.0%		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ADC specifications							
Over range output code			1,2,3	01	16383		Code
Under range output code			1,2,3	01		0	Code
Full channel performance specifications							
Differential non linearity	DNL	5 MHz	1,2,3	01	-1.03	1.53	LSB
		5 MHz CDS			-1.20	2.24	
		40 MHz			-1.03	1.45	
Integral non linearity	DNL	5 MHz	1,2,3	01	-5.38	4.38	LSB
		5 MHz CDS			-3.41	5.15	
		40 MHz			-9.9	7.34	
Noise floor CDS gain = 1x PGA gain = FE	Noise	5 MHz	1,2	01		-64.6	dB
			3			-62.5	
		40 MHz	1,2			-64.6	
			3			-65.7	
Noise floor CDS gain = 1x PGA gain = FE	Noise	5 MHz	1,2	01		9.6	LSB
			3			11.9	
		40 MHz	1,2			9.45	
			3			8.5	
Noise floor CDS gain = 1x PGA gain = 61	Noise	5 MHz	1,2,3	01		-78	dB
		40 MHz				-78	
Noise floor CDS gain = 1x PGA gain = 61	Noise	5 MHz	1,2,3	01		2.05	LSB
		40 MHz				2.05	
Channel to channel crosstalk		5 MHz	4,5,6	01		-77	dB
		40 MHz				-74	
CDS mode bimodal offset CDS gain = 1x PGA gain = 8x	BMD	5 MHz	1,2,3	01		6.0	mV
		40 MHz				6.0	
CDS mode bimodal offset CDS gain = 1x PGA gain = 1x	BMD	5 MHz	1,2,3	01		1	mV
		40 MHz				1.05	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Full channel performance specifications – continued.							
Signal to noise ratio	SNR	5 MHz	4,5	01	66.0		dB
			6		63.0		
		40 MHz	4,5		66.5		
			6		62.0		
Total harmonic distortion	THD	5 MHz	4,5	01		-69.0	dB
			6			-67.8	
		40 MHz	4,5			--60.0	
			6			-60.0	
Spurious free dynamic range	SFDR	5 MHz	4,5	01	69.4		dB
			6		68.4		
		40 MHz	4,5		60.0		
			6		60.0		
Signal to noise plus distortion ratio	SINAD	5 MHz	4,5	01	65.0		dB
			6		62.0		
		40 MHz	4,5		59.0		
			6		59.0		
Effective number of bits	ENOB	5 MHz	4,5	01	10.5		Bits
			6		10.0		
		40 MHz	4,5		9.5		
			6		9.5		
Input clock timing specification							
Input clock frequency	f_{INCLK}	INCLK = ADCCLK , (ADC rale clock)	9,10,11	01	5	40	MHz
Input clock duty cycle	T_{dc}	f_{INCLK} = 15 MHz	9,10,11	01	40/60	60/40	%

See footnotes at end of table.

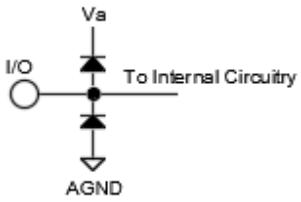
TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial interface timing specifications		See figure 4					
Input clock frequency	f_{SCLK}	$f_{SCLK} \le f_{INCLK}$, INCLK = ADCCLK, (ADC rate clock)	9,10,11	01	1	20	MHz
SCLK duty cycle		f_{INCLK} = 15 MHz	9,10,11	01	40/60	60/40	ns
Input hold time	t_{IH}	f_{INCLK} = 15 MHz	9,10,11	01	2.5		ns
Input setup time	t_{IS}	f_{INCLK} = 15 MHz	9,10,11	01	2.5		ns
SCLK start time after $\overline{SEN}$ low	t_{SENSC}	f_{INCLK} = 15 MHz	9,10,11	01	1.5		ns
$\overline{SEN}$ high after last SCLK rising edge	t_{SCSEN}	f_{INCLK} = 15 MHz	9,10,11	01	2.5		ns
$\overline{SEN}$ pulse width	t_{SENW}	f_{INCLK} = 15 MHz	9,10,11	01	8		ns
Output delay time	t_{OD}	f_{INCLK} = 15 MHz	9,10,11	01		11.6	ns
Data output to high Z	t_{HZ}	f_{INCLK} = 15 MHz	9,10,11	01		1.23	T_{SCLK}

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

2/ Unless otherwise specified, VDD33 = 3.3 V, VDD18 = 1.8 V, C_L = 10 pF, and f_{INCLK} = 40 MHz.

3/ The analog inputs are protected as shown below. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per footnote 4/ of Table IA. However, input errors will be generated If the input goes above VDD33 and below VSS.



4/ When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < VSS or V_{IN} > VDD33), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP	Temperature	Effective Linear energy transfer (LET)
01	No SEL	125°C	LET ≤ 120 MeV/(mg/cm^2)
	No SEFI	125°C	LET ≤ 120 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Heavy ion testing facility was 88" Cyclotron Facility at Lawrence Berkeley National Laboratory (LBNL) located in Berkeley, California and ion beam energy was 4.5 MeV/nucleon exposed inside a vacuum chamber. No single event latch-up (SEL) or single-event functional interrupt (SEFI) was observed when irradiated with Bismuth(Bi) ions at fluence 1x10^7 ions/cm^2 at an angle 35° with bias voltage 1.8 V and 3.3 V corresponding to an effective LET of 120 MeV(mg/cm^2). For more information on SEP test results, customers are requested to contact the manufacturer.

Case outline X

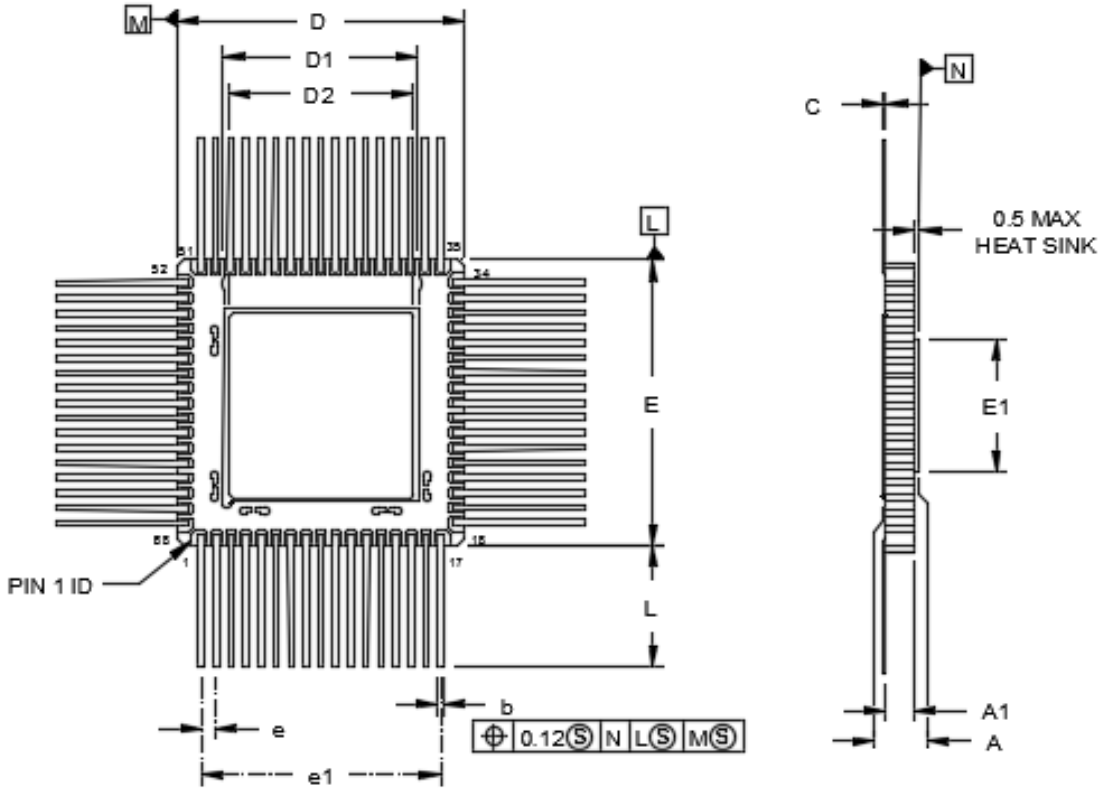


FIGURE 1. Case outline.

Case outline X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.1120	.1316	2.845	3.345
A1	.0811	.0992	2.06	2.52
b	.0161	.0200	0.41	0.51
c	.0078	.0118	0.20	0.30
D	.9401	.9598	23.88	24.38
D1	.6271	.6429	15.93	16.33
D2	.6020	.6079	15.291	15.443
E	.9401	.9598	23.88	24.38
E1	.4279	.4381	10.87	11.13
e	.0499 BSC		1.27 BSC	
e1	.7999 BSC		20.32 BSC	
L	.3838	.4035	9.75	10.25

NOTE:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.

FIGURE 1. Case outline – continued..

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VCOM1	18	VREFB2	35	VDD18	52	ATB1
2	VDD33	19	VREFT2	36	VSS18	53	VDD18
3	VDD33	20	VSS33	37	TXFRM+	54	VDD18
4	VSS33	21	VSS33	38	TXFRM-	55	VSS18
5	VSS33	22	VDD33	39	TXOUT3+	56	VSS18
6	OS1-	23	VDD33	40	TXOUT3-	57	INCLK-
7	OS1+	24	VSS33	41	TXOUT2+	58	INCLK+
8	VSS33	25	SDO	42	TXOUT2-	59	VSS33
9	VCLP	26	SDI	43	TXOUT1+	60	VDD33
10	VSS33	27	SCLK	44	TXOUT1-	61	VDD33
11	OS2+	28	$\overline{\text{SEN}}$	45	TXOUT0+	62	VSS33
12	OS2-	29	NC	46	TXOUT0-	63	IBIAS0
13	VSS33	30	CLPIN	47	TXCLK+	64	IBIAS1
14	VSS33	31	VSS18	48	TXCLK-	65	VREFBG
15	VDD33	32	VDD18	49	VSS18	66	VSS33
16	VDD33	33	DTM1	50	VDD18	67	VREFT1
17	VCOM2	34	DTM0	51	ATB0	68	VREFB1

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol	I/O 1/	Type	Resistor	Description
1	VCOM1	O	A		Common mode of ADC reference. Bypass with 0.1 µF capacitor to VSS33.
2	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
3	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
4	VSS33		P		Analog supply return.
5	VSS33		P		Analog supply return.
6	OS1-	I	A		Analog input signal.
7	OS1+	I	A		Sample/hold mode reference level. Bypassed with a 0.1 µF to ground in CDS mode.
8	VSS33		P		Analog supply return.
9	VCLP	O	A		Programmable clamp voltage output. Normally bypassed with a 0.1 µF capacitor to VSS33.
10	VSS33		P		Analog supply return.
11	OS2+	I	A		Sample/hold mode reference level. Bypassed with a 0.1 µF to ground in CDS mode.
12	OS2-	I	A		Analog input signal.
13	VSS33		P		Analog supply return.
14	VSS33		P		Analog supply return.
15	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
16	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
17	VCOM2	O	A		Common mode of ADC reference. Bypass with 0.1 µF capacitor to ground.
18	VREFB2	O	A		Bottom of ADC reference. Bypass with a 0.1 µF capacitor to ground.
19	VREFT2	O	A		Top of ADC reference. Bypass with a 0.1 µF capacitor to ground.
20	VSS33		P		Analog supply return.
21	VSS33		P		Analog supply return.
22	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
23	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
24	VSS33		P		Analog supply return.
25	SDO	O	D		Serial interface data output. (Tri-state when $\overline{SEN}$ is high)
26	SDI	I	D		Serial interface data input. (Tri-state when $\overline{SEN}$ is high)
27	SCLK	I	D	PD	Serial interface shift register clock. (Tri-state when $\overline{SEN}$ is high)
28	SEN	I	D	PU	Active-low chip enable for the serial interface.
29	NC				No connection. Can be connected to VSS18.
30	CLPIN	I	D		Input clamp signal.
31	VSS18		P		Digital supply return.
32	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
33	DTM1	O	D		Digital timing monitor. If not used, can be connected to VDD18 through a 10 kΩ resistor.
34	DTM0	O	D		Digital Timing Monitor. If not used, can be connected to VDD18 through a 10 kΩ resistor.
35	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.

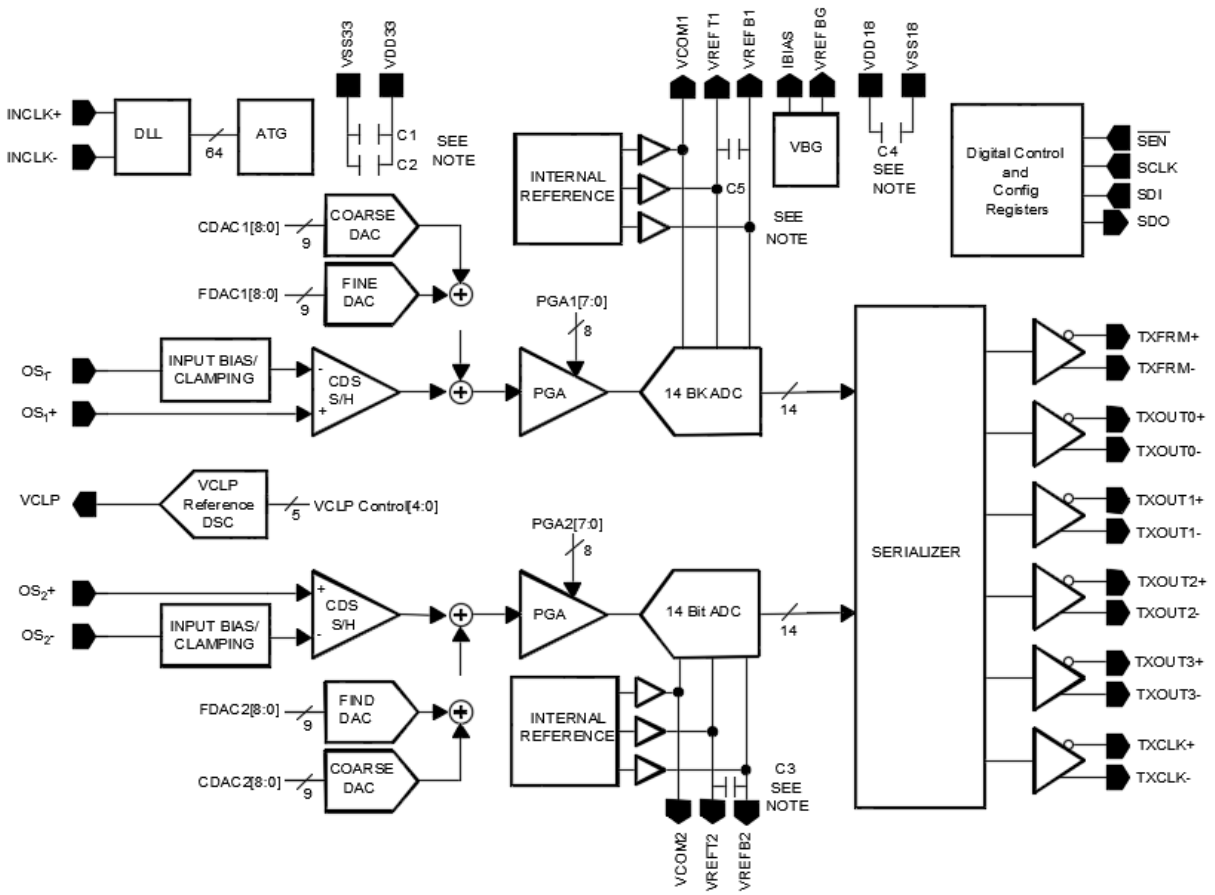
See footnote at end of table.

FIGURE 2. Terminal connection – continued.

Terminal number	Terminal symbol	I/O 1/	Type	Resistor	Description
36	VSS18		P		Digital supply return.
37	TXFRM+	O	D		LVDS Frame+
38	TXFRM-	O	D		LVDS Frame-
39	TXOUT3+	O	D		LVDS Data Out3+
40	TXOUT3-	O	D		LVDS Data Out3-
41	TXOUT2+	O	D		LVDS Data Out2+
42	TXOUT2-	O	D		LVDS Data Out2-
43	TXOUT1+	O	D		LVDS Data Out1+
44	TXOUT1-	O	D		LVDS Data Out1-
45	TXOUT0+	O	D		LVDS Data Out0+
46	TXOUT0-	O	D		LVDS Data Out0-
47	TXCLK+	O	D		LVDS Clock+
48	TXCLK-	O	D		LVDS Clock-
49	VSS18		P		Digital supply return.
50	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
51	ATB0	O	A		Analog test bus. If not used, can be connected to VSS18 through a 10 kΩ resistor.
52	ATB1	O	A		Analog test bus. If not used, can be connected to VSS18 through a 10 kΩ resistor.
53	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
54	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
55	VSS18		P		Digital supply return.
56	VSS18		P		Digital supply return.
57	INCLK-	I	D		Clock Input. Inverting input for LVDS clocks.
58	INCLK+	I	D		Clock Input. Non-Inverting input for LVDS clocks.
59	VSS33		P		Analog supply return.
60	VDD33		P		Analog power supply. Decouple with minimum 0.1µF capacitor to VSS33 plane.
61	VDD33		P		Analog power supply. Decouple with minimum 0.1µF capacitor to VSS33 plane.
62	VSS33		P		Analog supply return.
63	IBIAS0	I	A		Connect with external 10 kΩ 1% resistor to IBIAS1 pin.
64	IBIAS1	I	A		Connect with external 10 kΩ 1% resistor to IBIAS0 pin.
65	VREFBG	O	A		Band gap reference output. Bypass with a 0.1 µF capacitor to VSS33. Can be overdriven with external voltage source.
66	VSS33		P		Analog supply return.
67	VREFT1	O	A		Top of ADC reference. Bypass with a 0.1 µF capacitor to VSS33.
68	VREFB1	O	A		Bottom of ADC reference. Bypass with a 0.1 µF capacitor to VSS33.
	Exposed Pad		P		Exposed pad must be soldered to ground plane to ensure rated performance.

1/ I = input, O = output, IO = bi-directional, P = power, D = digital, A = analog, PU = pull up with an internal resistor, and PD = pull down with internal resistor

FIGURE 2. Terminal connections - continued.



Note: These devices are being assembled with five internal C1 through C5 precious metal electrode (PME) 0201 gold terminated bypass capacitors with capacitance value 10 nF and voltage 10 V, which meet approved criteria in accordance with MIL-PRF-123 or as approved by the qualifying activity. The capacitors are placed in the following locations, between

1. VDD33 (pins 2, 3) and VSS33 (pins 4, 5)
2. VSS33 (pins 13, 14) and VDD33 (pins 15, 16)
3. VREFB2 (pin 18) and VREFT2 (pin 19)
4. VDD18 (pins 53, 54) and VSS18 (pin 55, 56)
5. VREFT1 (pin 67) and VREFB1 (pin 68)

FIGURE 3. Block diagram.

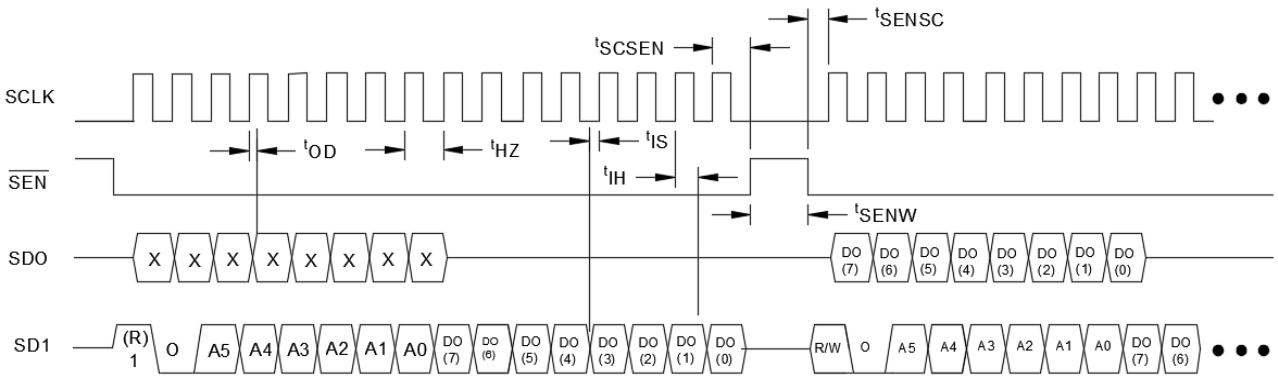


FIGURE 4. Serial interface specification diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4, 7, 9	1, 4, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 4, 1/ 5, 6, 7, 8, 9, 10,11	1, 2, 3, 1/ 2/ 4, 5, 6, 7, 8, 9, 10,11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9	1, 2, 3, 4, 5, 6, 7, 8, 9
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 2/ 5, 6, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9

1/ PDA applies to subgroups 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

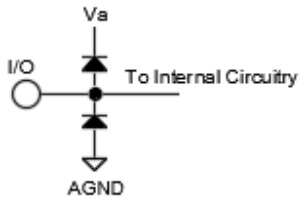
4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameter	Symbol	Conditions	Device type	Drift limit		Specification limit		Drift % of specification	Units
				Min	Max	Min	Max		
VDD33 Analog supply current dual channel power optimized for PGA gain = 1 - 4x	IA	Powerdown control reg = 0 x 00 (see manufacturer's datasheet section for PGA and ADC power trimming register settings)							
		5 MHz	01		±5.5		±58	9.48	mA
		40 MHz	01				±98	5.61	
VDD33 Analog supply current dual channel power optimized for PGA gain = 1 - 8x	IA	Powerdown control reg = 0 x 00 (see manufacturer's datasheet section for PGA and ADC Power trimming register settings)							
		5 MHz	01		±5.5		±58	9.48	mA
		40 MHz	01				±103	5.34	
VDD33 Analog supply current single channel power optimized for PGA gain = 1 - 4x	IA	Powerdown control reg = 0 x 15 (CH1 PD) or = 0 x 2A (CH2 PD) (see manufacturer's datasheet section for PGA and ADC Power Trimming register settings)							
		5 MHz	01		±3		±35	8.57	mA
		40 MHz	01				±60	5.00	
VDD33 Analog supply current single channel power optimized for PGA gain = 1 - 8x	IA	Powerdown control reg = 0 x 15 (CH1 PD) or = 0 x 2A (CH2 PD) (see manufacturer's datasheet section for PGA and ADC Power Trimming register settings)							
		5 MHz	01		±2.5		±35	7.14	mA
		40 MHz	01				±64	3.91	
VDD18 Digital supply current	ID	5 MHz	01		±2.5		29	8.62	mA
		40 MHz					37	6.76	

1/ The analog inputs are protected as shown below. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per footnote 4/ as specified under Table I. However, input errors will be generated, if the input goes above VDD33 and below VSS.



2/ These parameters are worse case drift. Deltas are performed at room temperature post operational life. All other parameters no Deltas are required

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ±10%.

f. For SEL test limits, see table IB herein.

g. For SEFI test limits, see table IB herein

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of latchup (SEL).

c. Number of transients/functional interrupts (SEFI).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-01-22

Approved sources of supply for SMD 5962-18203 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1820301VXC	01295	LM98640-RHA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243