REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct case outline X package. Add radiation hardened requirements. Add Appendix A for microcircuit die. Make corrections to pin assignments under Figure 2. Make limit changes to I_{SD} V_{IN}, V_{IHEN}, V_{ILEN}, t_{LOW}, V_{OVPR}, and V_{OVPF} tests as specified under Table I. Make additions to V_{OUT} and Thermal pad descriptions as specified under Figure 2. - ro	19-06-11	C. SAFFLE
B	Add device type 02, case outline Y, and device class P requirements. Glass transition temperature information to paragraph 1.4. Make change to Figure 4. - ro	23-12-19	J. ESCHMEYER

Revision Status of Sheets

REV	B	B	B	B	B	B	B	B	B	B	B											
SHEET	23	24	25	26	27	28	29	30	31	32	33											
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
RICK OFFICER

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
19-02-04

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR, 7 V, 6 A LOAD SWITCH MONOLITHIC SILICON

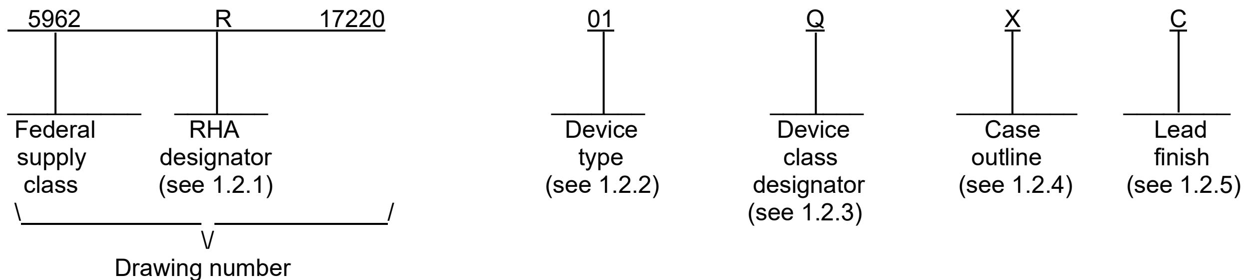
AMSC N/A	REVISION LEVEL B	SIZE A	CAGE CODE **67268**	**5962-17220**
		SHEET 1 OF 33		

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V or Y) and plastic encapsulated microcircuits (PEM) (device class N) for military, terrestrial and avionics application and device class P for space application. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device classes N and P, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. RHA marked devices classes are N, P, Q, Y, and V and meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H2201-SP	Radiation hardened 7 volt, 6 amp load switch
02	TPS7H2201-SP(QMLP)	Radiation hardened 7 volt, 6 amp load switch

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N or P	Certification and qualification to MIL-PRF-38535 for PEM performance environments.
Y	Certification and qualification to MIL-PRF-38535. Non hermetic flip chip technology on a ceramic or organic substrate.
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	16	Ceramic flat pack (CFP) with integrated thermal pads
Y	See figure 1	32	Plastic thin shrink small outline package (TSSOP)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, P, Q, Y, and V.

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Input voltage (V_{IN}) .... -0.3 V to 7.5 V
Output voltage (V_{OUT}) .... -0.3 V to 7.5 V
Enable and over voltage protection pins (EN, OVP) .... -0.3 V to 7.5 V
Current sense, current limit timer, retry timer, current limit and
soft start pins (CS, ILTIMER, RTIMER, IL, SS) .... -0.3 V to V_{IN} + 0.3 V
Maximum continuous switch current (I_{MAX}) .... 9 A maximum
Maximum pulsed switch current ($t \leq 5$ μs) (I_{PLS}) .... 45 A maximum
Maximum junction temperature (T_J) .... -55°C to +150°C
Storage temperature range .... -65°C to +150°C
Case outline X:
Thermal resistance, junction-to-ambient (θ_{JA}) .... 72.3°C/W
Thermal resistance, junction-to-case (top) (θ_{JCtop}) .... 96.1°C/W
Thermal resistance, junction-to-board (θ_{JB}) .... 42.1°C/W
Characterization parameter, junction-to-top (ψ_{JT}) .... 3.3°C/W
Characterization parameter, junction-to-board (ψ_{JB}) .... 42.5°C/W
Thermal resistance, junction-to-case (bottom) (θ_{JCbot}) .... 0.6°C/W
Case outline Y:
Thermal resistance, junction-to-ambient (θ_{JA}) .... 23.5°C/W
Thermal resistance, junction-to-case (top) (θ_{JCtop}) .... 11.2°C/W
Thermal resistance, junction-to-board (θ_{JB}) .... 5.4°C/W
Characterization parameter, junction-to-top (ψ_{JT}) .... 0.1°C/W
Characterization parameter, junction-to-board (ψ_{JB}) .... 5.4°C/W
Thermal resistance, junction-to-case (bottom) (θ_{JCbot}) .... 0.5°C/W
Electrostatic discharge (ESD) rating:
Human body model (HDM) per JEDEC JS-001 .... ±4000 V 3/
Charge device model (CDM) per JEDEC JESD22-C101 .... ±750 V 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values are with respect to network ground pin.

3/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions.

4/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions.

1.4 Recommended operating conditions.

Input voltage (V_{IN}) .... 1.5 V to 7 V
Input voltage slew rate (SR_{VIN}) .... 0.01 V/µs
Output voltage (V_{OUT}) .... 0 V to 7 V 5/
Maximum continuous switch current (I_{MAX}) .... 6 A
Ambient operating temperature range (T_A) .... -55°C to +125°C 6/
Glass transition temperature:
Mold compound (Tg) .... 115°C 7/

1.5 Radiation features.

Device type 01 :
Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s) .... 100 krads(Si) 8/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s) .... 100 krads(Si) 8/
Device type 02:
Maximum total dose available (dose rate = 50 - 300 rad(Si)/s) .... 100 krads(Si) 9/

Heavy ion single event phenomenon (SEP):
No Single event latch-up (SEL) occurs at effective LET_{eff} (see 4.4.4.2) .... ≤ 75 MeV/(mg/cm^2) 10/
No Single event burnout (SEB) occurs at effective LET_{eff} (see 4.4.4.2) .... ≤ 75 MeV/(mg/cm^2) 10/
No Single event gate rupture (SEGR) occurs at effective LET_{eff} (see 4.4.4.2) .... ≤ 75 MeV/(mg/cm^2) 10/
No Single event functional interrupt (SEFI) occurs at LET_{eff} (see 4.4.4.2) .... ≤ 75 MeV/(mg/cm^2) 10/

5/ This maximum V_{OUT} voltage is only applicable when the device is disabled (EN = low). When the device is enabled (EN = high), the maximum V_{OUT} voltage is the input voltage, V_{IN}.

6/ In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature $T_{A(max)}$ is dependent on the maximum operating junction temperature $T_{J(max)}$, the maximum power dissipation of the device in the application $P_{D(max)}$, and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation:
$T_A(max) = T_J(max) – (\theta_{JA} \times P_D(max))$.

7/ Glass transition temperature (Tg) of mold compound measured specification value 115°C but, tested Tg is 135°C.

8/ The manufacturer supplying device type 01 (LBC7 process technology) has performed characterization testing in accordance with MIL-STD-883 method 1019, and the parts exhibited no low dose rate sensitivity at a dose level of 100 krad(Si). The radiation end points limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krad(Si).

9/ Device type 02 (LBC7 process technology) supplied to this drawing has been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 100 krads(Si) as specified herein.

10/ For more information on SEP test results, customers are requested to contact the manufacturer (see SEP table IB).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) INTERNATIONAL

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) from Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JESD22-C101 – Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD 57 – Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation
JEDEC JEP 155 – Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 – Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, P, Q, Y, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing waveform. The timing waveform shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

\T/ YMLLLLSG4
1722002PYE-
O Q MLA NNNN

O – PIN 1

\T/	= TI LOGO
YM	= MONTHLY DATE CODE
LLLL	= LOT TRACE CODE
S	= ASSEMBLY SITE CODE
	(PER QSS 005-120)
Q	= QML
MLA	= COUNTRY
NNNN	= SERIAL NUMBER, 4 DIGIT

MAXIMUM	CHARACTERISTICS:
8 CHARACTERS	- 1 ST LINE
10 CHARACTERS	- 2 ND LINE

G4 MUST BE SYMBOLIZED WITH A SOLDI LINE UNDERSCORE

3.5.1 Certification/compliance mark. The certification mark for device classes N, P, Q, Y, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supplies and currents							
Quiescent current	I_Q	I_{OUT} = 0 mA, V_{IN} = EN = 5 V, CS resistor of 20 kΩ to GND	1,2,3	01, 02		6.5	mA
V_{IN} to V_{OUT} forward leakage current	I_F		1,2,3	01		250	µA
		EN = V_{OUT} = GND, measured V_{OUT} current, $1.5 V \le V_{IN} \le 7 V$		02		250	
V_{IN} off state supply current	I_{SD} V_{IN}	V_{IN} = 5 V, EN = GND, V_{OUT} = 0 V, measured V_{IN} current	1,2,3	01		3.1	mA
				02		3	
		M, D, P, L, R	1	01, 02		3.1	
		V_{IN} = 3.3 V, EN = GND, V_{OUT} = 0 V, measured V_{IN} current	1,2,3	01, 02		3.1	
		M, D, P, L, R	1	01, 02		3.1	
		V_{IN} = 1.8 V, EN = GND, V_{OUT} = 0 V, measured V_{IN} current	1,2,3	01, 02		3.1	
		M, D, P, L, R	1	01, 02		3.1	
Reverse current protection leakage current	I_{RCP}	EN = 0 V, V_{IN} = 0 to 7 V, V_{OUT} = 0 to 7 V for $V_{OUT} > V_{IN}$	1,2,3	01, 02		2.5	mA
		M, D, P, L, R	1	02		20	
		EN = 7 V, V_{IN} = 0 V, V_{OUT} = 0 to 7 V	1,2,3	01, 02		2.5	
		M, D, P, L, R	1	02		20	
Soft start							
Soft start charge current	I_{SS}		1,2,3	01, 02		83	µA

See footnote at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Enable and undervoltage lockout (EN/UVLO) input.							
EN/UVLO threshold voltage, rising	V_{IHEN}		1,2,3	01, 02	0.56	0.65	V
EN/UVLO threshold voltage, falling	V_{ILEN}		1,2,3	01, 02	0.47	0.55	V
EN/UVLO hysteresis voltage	$HYST_{EN}$		1,2,3	01, 02		124	mV
EN signal low time during cycling	t_{LOW}	R_{TIMER} = GND, I_L = 1 A. I_{VOUT} = 2 A, see figure 3	9,10,11	01, 02	20		µs
V_{IN} percentage for enable	VIN_{EN}		1,2,3	01, 02	75		%
EN pin input leakage current	I_{EN}	EN = V_{IN} = 5 V	1,2,3	01, 02		12	nA
Overvoltage protection (OVP)							
OVPR threshold voltage, rising	V_{OVPR}		1,2,3	01, 02	0.52	0.63	V
OVPF threshold voltage, falling	V_{OVPF}		1,2,3	01, 02	0.5	0.59	V
OVP hysteresis voltage	$HYST_{OVP}$	1.6 V < V_{IN} < 7 V	1,2,3	01, 02		55	mV
OVP pin input leakage current	I_{OVP}		1,2,3	01, 02		15	nA
Current limit and current sense							
Time for valid CS output after enable	t_{CSEN}	C_{SS} = 120 nF, see figure 4	9,10,11	01, 02		5	ms
Minimum V_{OUT} current for valid CS output			1,2,3	01, 02	750		mA
V_{OUT} current change to CS delay time		0.5 A rising step, 100 mA/µs, 1.5 V ≤ V_{IN} ≤ 7 V, see figure 5	9,10,11	01, 02		74	µs
		0.5 A falling step, 100 mA/µs, 1.5 V ≤ V_{IN} ≤ 7 V, see figure 5				73	
CS pin accuracy		0.75 A ≤ I_{VOUT} ≤ 7.5 A	1,2,3	01, 02	-10	10	%
CS pin voltage		0.75 A ≤ I_{VOUT} ≤ 7.5 A, no OCP	1,2,3	01, 02		V_{IN} – 0.4	V
Current limit setting	I_{IL}	I_{VOUT} ≤ 1 A	1,2,3	01, 02	I_{VOUT} + 0.5		A
		1 A < I_{VOUT} ≤ 3 A			I_{VOUT} + 1		
		I_{VOUT} > 3 A			I_{VOUT} + 1.5		

See footnote at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Current limit and current sense – continued.							
Programmable current limit accuracy		1.5 V ≤ V_{IN} ≤ 7 V	1,2,3	01, 02	-20%	20%	
Fast trip off time		V_{IN} = 5 V, C_{SS} = 2.7 nF	9,10,11	01		158	µs
Internal current limit timer (fast trip off current limit)		V_{IN} = 5 V, I_{VOUT} = 3 A, I_L = 6 A, ILTIMER = V_{IN}, 10 mΩ short in 10 µs	9,10,11	01		35	µs
Timers		See figure 6.					
ILTIMER charge current	$I_{ILTIMER}$		1,2,3	01, 02	0.7	1.38	µA
ILTIMER internal pull down resistance	$PD_{ILTIMER}$	40 mV on ILTIMER pin	4,5,6	01, 02		153	Ω
RTIMER charge current	I_{RTIMER}		1,2,3	01, 02	0.7	1.38	µA
RTIMER internal pull down resistance	PD_{RTIMER}	40 mV on RLTIMER pin	4,5,6	01, 02		153	Ω
Resistance characteristics							
ON – state resistance	R_{ON}	V_{IN} = 7 V, I_L = 7.5 A , lead length = 2.5 mm	4	01		34	mΩ
			5			45	
			6			24	
		V_{IN} = 7 V, I_L = 7.5 A	4	02		21	
			5			27	
			6			17	
		V_{IN} = 5 V, I_L = 7.5 A, lead length = 2.5 mm	4	01		35	
			5			47	
			6			26	
		V_{IN} = 5 V, I_L = 7.5 A	4	02		23	
			5			29	
			6			18	

See footnote at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resistance characteristics – continued.							
ON – state resistance	R_{ON}	V_{IN} = 3.3 V, I_L = 7.5 A, lead length = 2.5 mm	4	01		38	mΩ
			5			52	
			6			28	
		V_{IN} = 3.3 V, I_L = 7.5 A	4	02		26	
			5			33	
			6			21	
		V_{IN} = 1.8 V, I_L = 7.5 A, lead length = 2.5 mm	4	01		51	
			5			70	
			6			36	
		V_{IN} = 1.8 V, I_L = 7.5 A	4	02		37	
			5			48	
			6			29	
		V_{IN} = 1.5 V, I_L = 7.5 A, lead length = 2.5 mm	4	01		63	
			5			87	
			6			44	
		V_{IN} = 1.5 V, I_L = 7.5 A	4	02		46	
			5			59	
			6			36	

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L and R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ The manufacturer supplying device type 01 (LBC7 process technology) has performed characterization testing in accordance with MIL-STD-883 method 1019, and the parts exhibited no low dose rate sensitivity at a dose level of 100 krad(Si). The radiation end points limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krad(Si).

3/ Device type 02 (LBC7 process technology) supplied to this drawing has been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019. The TID test is performed as radiation lot acceptance testing of these devices to TID level 100 krads(Si) as specified herein.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP/SEE	Temperature (T_C)	Conditions	Linear energy transfer (LET_{eff})
01, 02	No SEL	125°C	V_{IN} = 7 V, I_{OUT} = 6 A	$LET_{eff} \leq 75$ MeV/(mg/cm^2)
	No SEB	33°C	V_{IN} = 7 V, 1.5 V, I_{OUT} = 6 A, 0 A	$LET_{eff} \leq 75$ MeV/(mg/cm^2)
	No SEGR	33°C	V_{IN} = 7 V, 1.5 V, I_{OUT} = 6 A, 0 A	$LET_{eff} \leq 75$ MeV/(mg/cm^2)
	No SEFI	33°C	V_{IN} = 7 V, 1.5 V, I_{OUT} = 6 A, 0 A	$LET_{eff} \leq 75$ MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board.

3/ SEE test shall be performed in accordance with ASTM F1192 or JESD57. For more information on SEP test results, customers are requested to contact the manufacturer.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

Case X

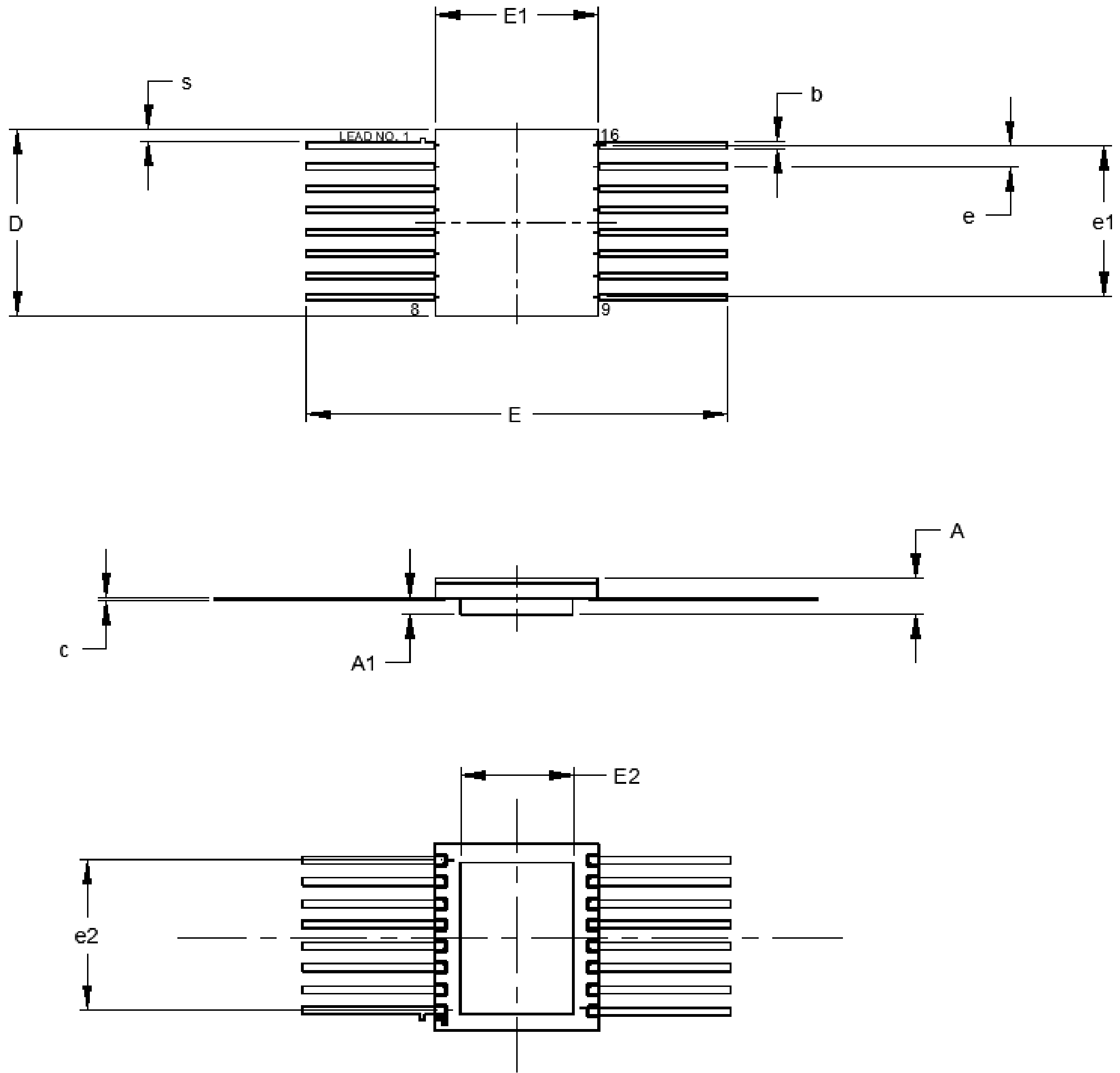


FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	.072	.0920	1.833	2.333
A1	.027	.047	0.690	1.190
b	.015	.019	0.382	0.482
c	.004	.007	0.097	0.177
D	.424	.443	10.760	11.260
e	.047	.053	1.190	1.350
e1	.350 NOM		8.890 NOM	
e2	.337	.356	8.550	9.050
E	.970	.990	24.642	25.142
E1	.369	.389	9.380	9.880
E2	.250	.269	6.340	6.840
s	.033 REF		0.844 REF	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid. The lid and heat slug are connected to GND pin.
3. The terminals will be gold plated.

FIGURE 1. Case outlines – continued.

Case Y

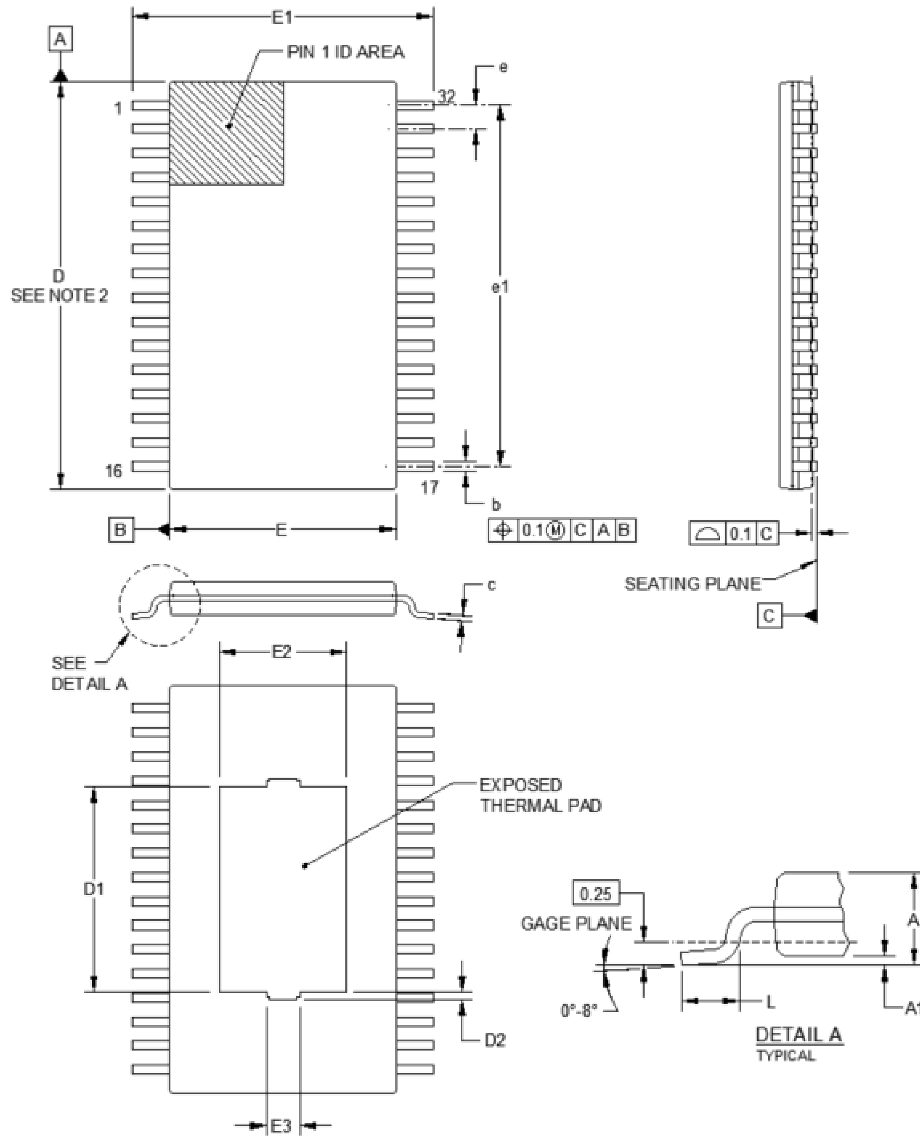


FIGURE 1. Case outlines - continued.

Case Y - continued

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.047	---	1.2
A1	.002	.006	0.05	0.15
b	.007	.012	0.19	0.30
c	.006 NOM		0.15 NOM	
D	.429	.437	10.9	11.1
D1	.201	.236	5.1	6.0
D2	.008 REF		0.2 REF	
E	.236	.244	6.0	6.2
E1	.311 NOM	.326 NOM	7.9 NOM	8.3 NOM
E2	.118	.153	3.0	3.9
E3	.035 REF		0.9 REF	
e	.026 BSC		0.65 BSC	
e1	.384 BSC		9.75 BSC	
L	.020	.029	0.50	0.75

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension D body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
3. For dimensions D2 and E3, features may differ and may not be present.
4. Falls within reference to JEDEC MO-153.

FIGURE 1. Case outlines - continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	VIN
2	VIN
3	VIN
4	VIN
5	CS
6	EN
7	OVP
8	GND
9	RTIMER
10	IL
11	ILTIMER
12	SS
13	VOUT
14	VOUT
15	VOUT
16	VOUT

FIGURE 2. Terminal connections.

Device type	01	
Case outline	X	
Terminal symbol	I/O	Description
VIN	I	Switch input. Input bypass capacitor recommended for minimizing VIN dip.
EN	I	Active high switch control input. Do not leave floating.
OVP	I	Overvoltage protection. Programmable using an external resistor divider. If no OVP is desired, this pin should be connected to GND.
SS	I/O	Switch slew rate control. Can be left floating.
GND	---	Device ground.
RTIMER	I/O	Fault timer control during disabled and retry mode. Connecting this pin to GND holds the switch disabled until the EN pin is cycled.
IL	I/O	Current limiter control.
ILTIMER	I	Fault timer control during limiting mode. Connecting this pin to VIN uses the internal current limit timer.
CS	O	Current sense pin proportional to output current.
VOUT	O	Switch output. A minimum 10 μF output capacitor is recommended.
NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
Thermal pad	---	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND.

FIGURE 2. Terminal connections - continued.

Device type	01		
Case outline	Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VIN	17	NC
2	VIN	18	RTIMER
3	VIN	19	NC
4	VIN	20	IL
5	VIN	21	ILTIMER
6	VIN	22	SS
7	VIN	23	VOUT
8	VIN	24	VOUT
9	VIN	25	VOUT
10	VIN	26	VOUT
11	CS	27	VOUT
12	EN	28	VOUT
13	OVP	29	VOUT
14	NC	30	VOUT
15	GND	31	VOUT
16	NC	32	VOUT

FIGURE 2. Terminal connections - continued.

Device type	02	
Case outline	Y	
Terminal symbol	I/O	Description
VIN	I	Switch input. Input bypass capacitor recommended for minimizing VIN dip.
EN	I	Active high switch control input. Do not leave floating.
OVP	I	Overvoltage protection. Programmable using an external resistor divider. If no OVP is desired, this pin should be connected to GND.
SS	I/O	Switch slew rate control. Can be left floating.
GND	---	Device ground.
RTIMER	I/O	Capacitor programmed fault timer control during disabled and retry mode. Connecting this pin to GND holds the switch disabled until the EN pin is cycled. Do not float this pin or connect it to VIN.
IL	I/O	Programmable using an external resistor to GND. Do not float this pin.
ILTIMER	I	Capacitor programmed fault timer control during current limiting mode. Connecting this pin to VIN uses the internal current limit timer and connecting this pin to GND disables the internal timer functionality for the ILTIMER as well as retry mode. In this case, the device will remain at programmed current limit indefinitely in the event of a short without going intro retry mode. Do not float this pin.
CS	O	Current sense pin proportional to output current. Connect a resistor to GND.
VOUT	O	Switch output. A minimum 10 μF output capacitor is recommended.
NC	---	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.
Thermal pad	---	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND.

FIGURE 2. Terminal connections - continued.

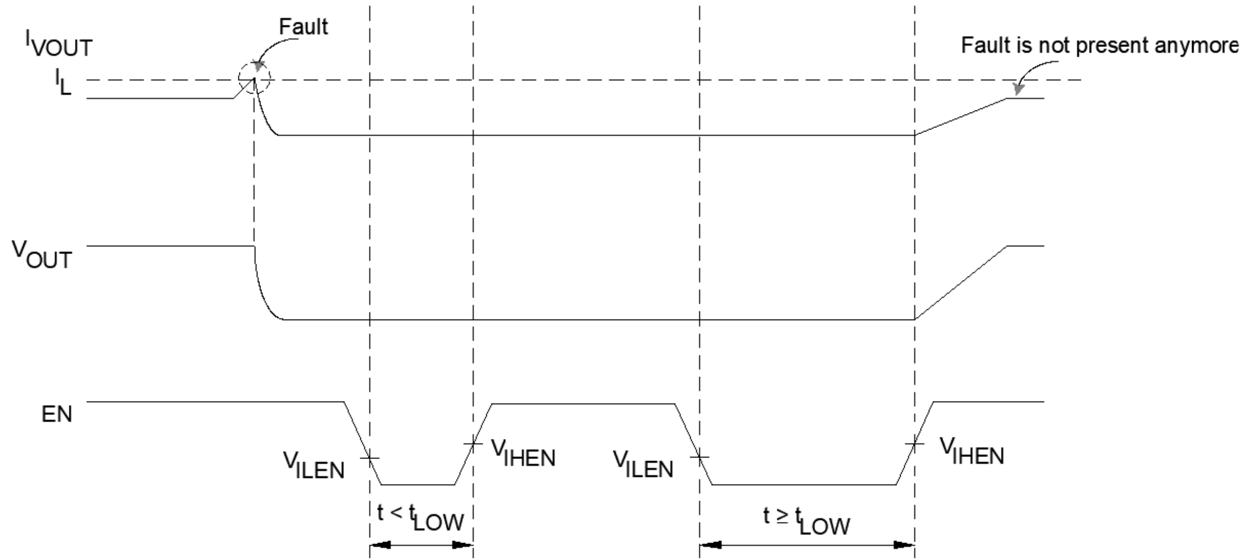


FIGURE 3. EN signal low time to restart device waveform. (t_{LOW})

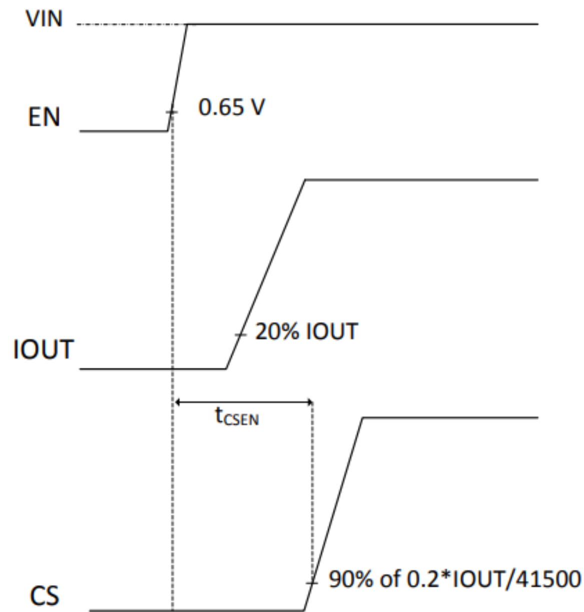


FIGURE 4. tCSEN waveforms.

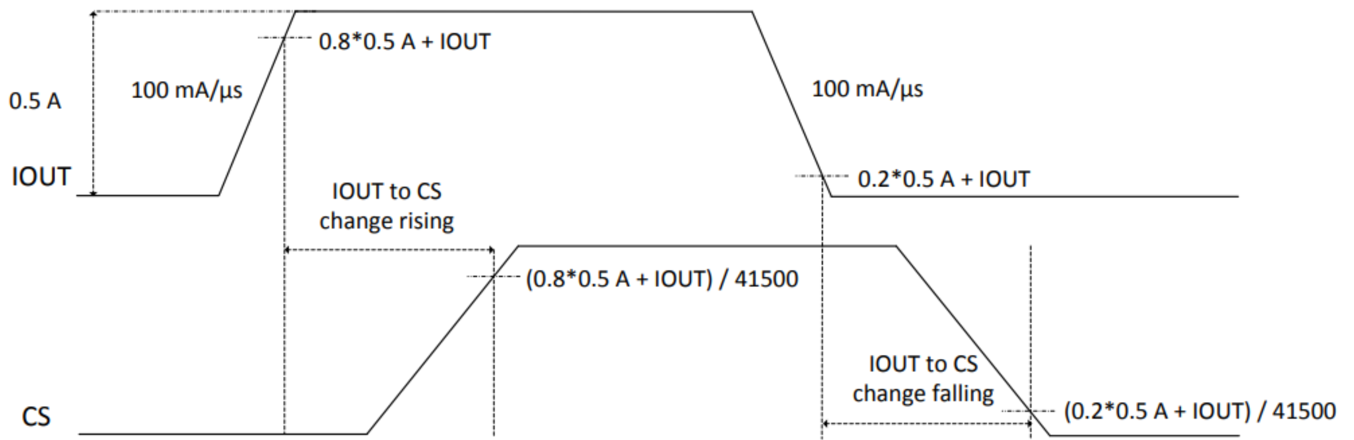


FIGURE 5. VOUT current to CS change delay time.

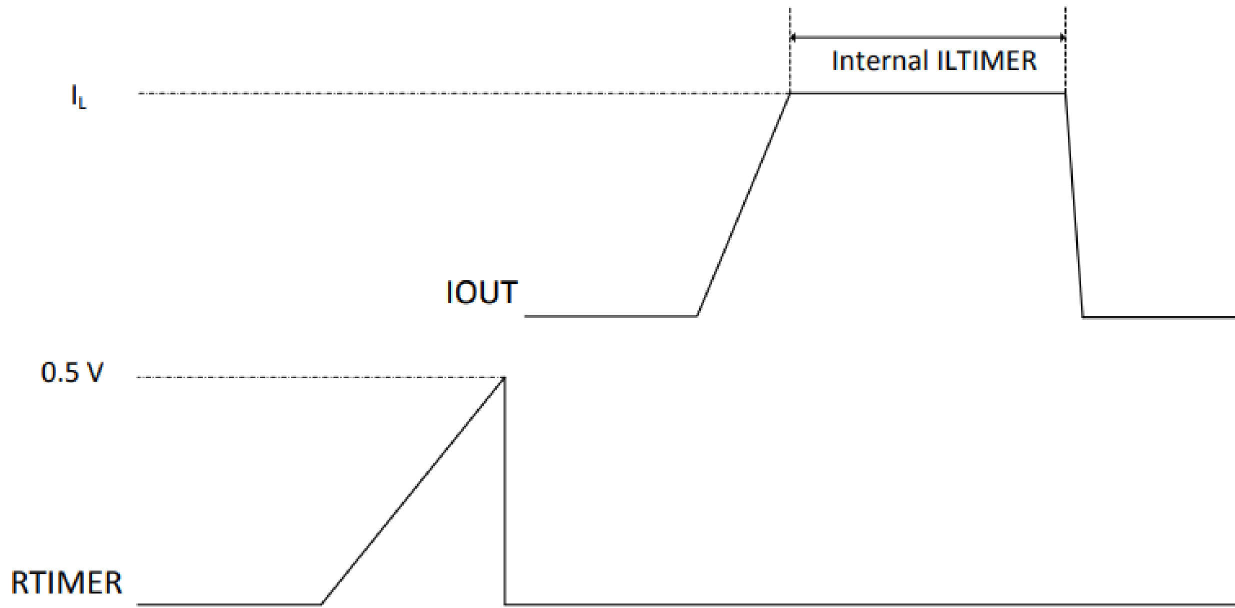


FIGURE 6. Internal ILTIMER waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, P, Q, Y, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, P, Q, Y, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, P, Q, Y and V.

a. Test condition A, B, C and D. Burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Unless otherwise specified in the QM plan, for devices class N, P, Q, Y, and V, dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

c. For devices class P, Y, and V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

4.3 Qualification inspection. Qualification inspection for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. Preconditioning shall be performed on non hermetic device classes N, P, and Y surface mount devices as specified in the manufacturer’s QM plan. Thermal shock is not applicable to class N, P, and organic class Y.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)				
	Device class N	Device class P	Device class Q	Device class V	Device class Y
Interim (pre burn-in) electrical parameters, (see 4.2)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Post burn-in electrical parameters (see 4.2.1)	1, 2, 3, 4, 1/ 5, 6, 9, 10, 11	1, 2, 3, 1/ 2/ 4, 5, 6, 9, 10, 11	1, 2, 3, 1/ 4, 5, 6, 9, 10, 11	1, 2, 3, 1/ 2/ 4, 5, 6, 9, 10, 11	1, 2, 3, 1/ 4, 5, 6, 9, 10, 11
Group A (Final electrical) test requirements (see 4.4.1)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4.2)	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 2/ 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11	1, 2, 3, 2/ 4, 5, 6, 9, 10, 11	1, 2, 3, 4, 5, 6, 9, 10, 11
Group D end-point electrical parameters (see 4.4.3)	1, 4, 9	1, 4, 9	1, 4, 9	1, 4, 9	1, 4, 9
Group E end-point electrical parameters (see 4.4.4)	1, 4, 9	1, 4, 9	1, 4, 9	1, 4, 9	1, 4, 9

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Device type	Limit
Quiescent current	I_Q	I_{OUT} = 0 mA, V_{IN} = EN = 5 V, CS resistor of 20 kΩ to GND	01, 02	±275 μA
V_{IN} to V_{OUT} forward leakage current	I_F		01, 02	±5 μA
V_{IN} off-state supply current	ISD VIN	EN = GND, V_{OUT} = 0 V	01, 02	±125 μA
Reverse current protection leakage current	IRCP	EN = 0 V, V_{IN} = 0 to 7 V V_{OUT} = 0 to 7 V for $V_{OUT} > V_{IN}$	01, 02	±190 μA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. RHA levels for device classes N, P, Q, Y, and V, shall be as specified in MIL-PRF-38535 and the end-point electrical parameters subgroups shall be as specified in table IIA herein.

b. For device classes N, P, Q, Y, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and D for device type 01 and condition A for device type 02 and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V and P devices (see 1.5 herein). SEP testing shall be performed on actual devices or technology process on the Standard Evaluation Circuit (SEC) as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 or JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ±10% for SEL.

f. For SEP test limits, see table IB herein.

g. For SEL test limits, see table IB herein.

h. For SEFI test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply. Sources of supply for device classes N, P, Q, Y, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of latch-up (SEL).

c. Occurrence of burnout (SEB).

d. Occurrence of gate rupture (SEGR).

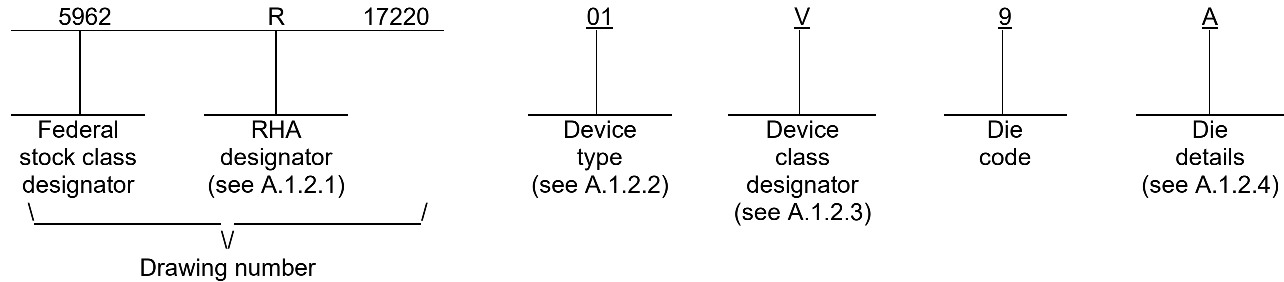
e. Occurrence of functional interrupt (SEFI).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-17220

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H2201-SP	7 volt, 6 amp load switch

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figures A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0591.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

Bond pad coordinates in microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VIN	1	679.75	5529	835.25	5684.5
VIN	2	286.85	5529	442.35	5684.5
VIN	3	286.85	5343.5	442.35	5499
VIN	4	679.75	5343.5	835.25	5499
VIN	5	286.85	5157.1	442.35	5312.6
VIN	6	679.75	5157.1	835.25	5312.6
VIN	7	286.85	4970.65	442.35	5126.15
VIN	8	679.75	4970.65	835.25	5126.15
VIN	9	286.85	4053	442.35	4208.5
VIN	10	679.75	4053	835.25	4208.5
VIN	11	286.85	3867.5	442.35	4023
VIN	12	679.75	3867.5	835.25	4023
VIN	13	286.85	3681.1	442.35	3836.6
VIN	14	679.75	3681.1	835.25	3836.6
VIN	15	286.85	3494.65	442.35	3650.15
VIN	16	679.75	3494.65	835.25	3650.15
VIN	17	286.85	2572.85	442.35	2728.35
VIN	18	679.75	2572.85	835.25	2728.35
VIN	19	286.85	2384.85	442.35	2540.35
VIN	20	679.75	2384.85	835.25	2540.35
AVDD	21	61.1	2046.7	216.6	2202.2
AVDD	22	61.1	1857.2	216.6	2012.7
CS	23	61.1	1645.3	216.6	1800.8
EN	24	61.1	1080.75	216.6	1236.25
OVP	25	61.1	451.4	216.6	606.9
GND	26	452.45	61.1	607.95	216.6
GND	27	641.95	61.1	797.45	216.6
RTIMER	28	3103.2	61.1	3258.7	216.6
IL	29	3683.4	652.7	3838.9	808.2
ILTIMER	30	3683.4	1221.4	3838.9	1376.9
SS	31	3683.4	1715.65	3838.9	1871.15
VOUT	32	3457.4	2384.85	3612.9	2540.35
VOUT	33	3064.5	2384.85	3220	2540.35
VOUT	34	3457.4	2572.85	3612.9	2728.35
VOUT	35	3064.5	2572.85	3220	2728.35

FIGURE A-1. Die bonding pad locations and electrical functions.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-17220

Bond pad coordinates in microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VOUT	36	3457.4	3494.65	3612.9	3650.15
VOUT	37	3064.5	3494.65	3220	3650.15
VOUT	38	3457.4	3681.1	3612.9	3836.6
VOUT	39	3064.5	3681.1	3220	3836.6
VOUT	40	3457.4	3867.5	3612.9	4023
VOUT	41	3064.5	3867.5	3220	4023
VOUT	42	3457.4	4053	3612.9	4208.5
VOUT	43	3064.5	4053	3220	4208.5
VOUT	44	3457.4	4970.65	3612.9	5126.15
VOUT	45	3064.5	4970.65	3220	5126.15
VOUT	46	3457.4	5157.1	3612.9	5312.6
VOUT	47	3064.5	5157.1	3220	5312.6
VOUT	48	3457.4	5343.5	3612.9	5499
VOUT	49	3064.5	5343.5	3220	5499
VOUT	50	3457.4	5529	3612.9	5684.5
VOUT	51	3064.5	5529	3220	5684.5

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

DSCC FORM 2234
APR 97

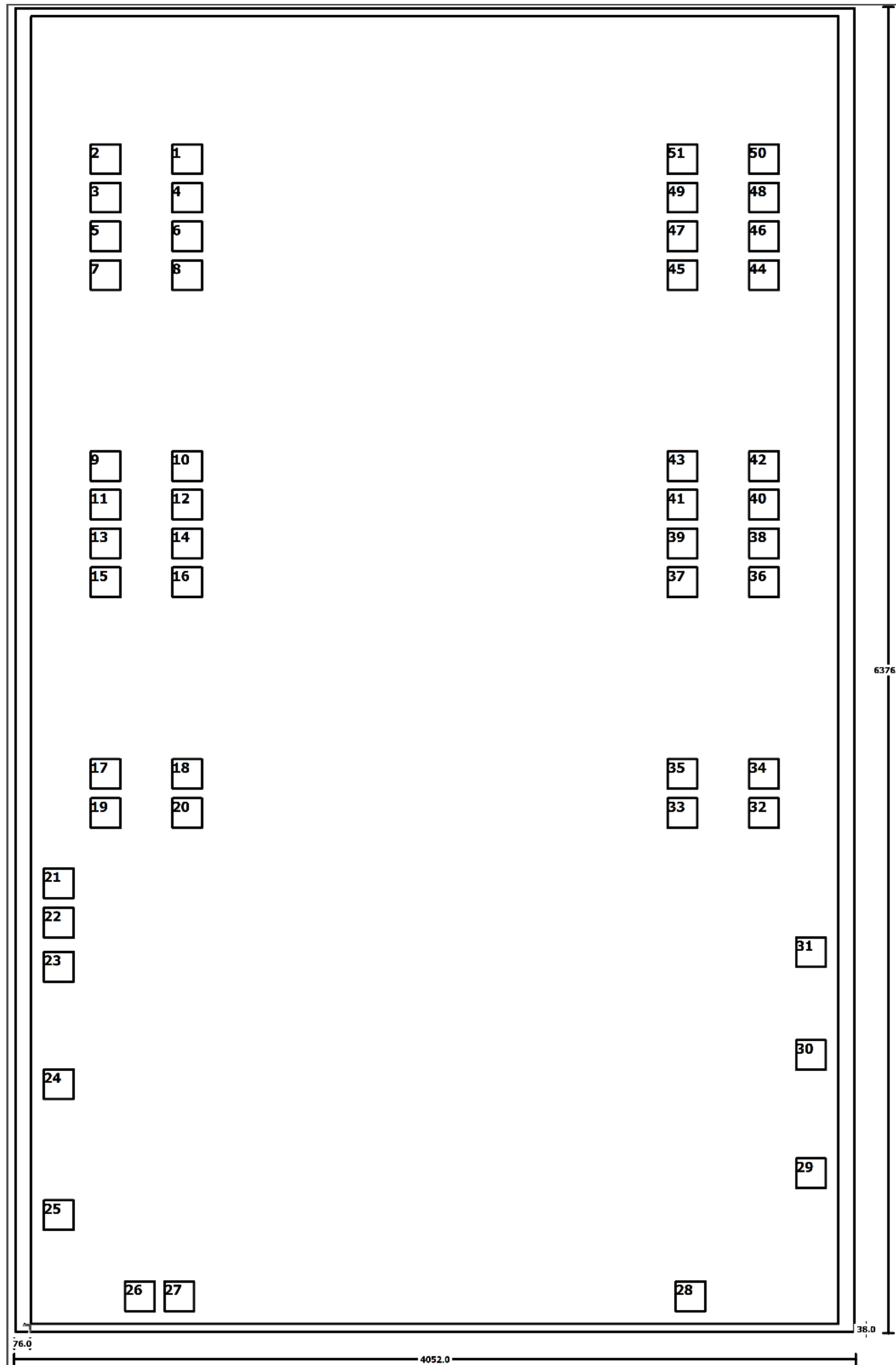


FIGURE A-1. Die bonding pad locations and electrical functions - continued.

Die physical dimensions :

Die size: 3510 μm x 5670 μm

Die thickness: 15 mils ±1 mils

Interface materials.

Top metallization: Al

Backside metallization: Bare back

Glassivation.

Type: Nitride

Thickness: 11 kÅ

Substrate: Single crystal silicon

Assembly related information.

Substrate potential: Ground

Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-12-19

Approved sources of supply for SMD 5962-17220 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1722001VXC	01295	TPS7H2201-SP
5962R1722001VXC	01295	TPS7H2201-RHA
5962R1722001V9A	01295	TPS7H2201-KGD
5962R1722002PYE	01295	TPS7H2201-QMLP

1/ The lead finish shown for each PIN is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.