REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Remove V_H and I_{IH}, update limits of INL_{ADC}, DNL_{ADC}, E_{OFF}, and GE_{ADC} to Table IA. Update SEP Test Limits, and relevant notes to Table IB. Correction to pin M2, pin C4 on Figure 3. Correction MOSI to MISO for tDS and MISO to MOSI for tVD, remove tDIS and tACC on Figure 5. Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - TTM	21-04-23	Muhammad A. Akbar

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
18-11-29

REVISION LEVEL
A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, CMOS, 32-BIT MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-17212**

SHEET 1 OF 26

DSCC FORM 2233
APR 97

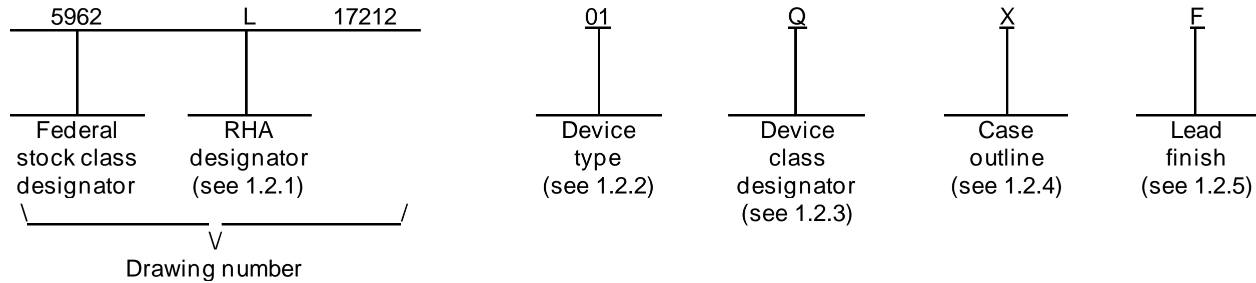
5962-E061-21

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT32M0R500	32-Bit Microcontroller
02	UT32M0R500	32-Bit Microcontroller with additional screening 1/

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	143	Ceramic Land Grid Array (CLGA)
Y	See figure 1	143	Ceramic Column Grid Array (CCGA) 2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Device type 02 provides a QML-Q product with additional testing as specified in section 4.2.1.d.
2/ Package Y (Ceramic Column Grid Array) lead finish is "F" and is a composition of tin (Sn) 63% and lead (Pb) 37%.

1.3 Absolute maximum ratings. 3/ 4/

Positive Digital Supply Voltage (V_{DD}) .... -0.3 V to +4.2 V
Positive Analog Supply Voltage (V_{DDA}) .... -0.3 V to +4.2 V
Digital Pin Input Voltage (V_{ID}) .... V_{SS} – 0.3 V to V_{DD} + 0.3 V
Analog Pin Input Voltage (V_{IA}) .... V_{SSA} – 0.3 V to V_{DDA} +0.3 V
Maximum Power Dissipation (P_D) 5/ .... 4.5 W
Junction Temperature (T_J) .... -55°C to +150°C
Maximum Thermal resistance, junction-to-case (θ_{JC}) .... 10°C/W
Storage temperature (T_{STG}) .... -65°C to +150°C
Maximum ESD Protection (ESD_{HBM}) 6/ .... 2000 V

1.4 Recommended operating conditions. 7/

Positive Digital Supply Voltage (V_{DD}) .... +3.0 V to +3.6 V
Positive Analog Supply Voltage (V_{DDA}) .... +3.0 V to +3.6 V
Digital Ground (V_{SS}) .... +0.0 V
Analog Ground (V_{SSA}) .... +0.0 V
Temperature Range (T_{OP}) .... -55°C to +105°C
Case Operating Temperature Range (T_C) .... -55°C to +105°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rad(Si)/s)....... 50 krads(Si) 8/ 10/
Single Event Phenomenon (SEP):
No SEL occurs at effective LET (see 4.4.4.2) .... ≤ 80 MeV-cm^2/mg 9/ 11/ 12/
Heavy Ion Soft Error Rate (SER) (see 4.4.4.2) .... $8.30x10^{-8}$ errors/device-day 9/ 11/ 12/ 13/ 14/ 15/

3/ Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

4/ All V_{DD} voltages referenced to V_{SS} and all V_{DDA} voltages referenced to V_{SSA}.

5/ Per MIL-STD-883, method 1012.1, section 3.4.1, P_D = [TJ(max)-TC(max))/θ_{JC}]. Using T_C = 105°C.

6/ Per MIL-STD-883, method 3015.9, Table 3.

7/ V_{DD} referenced to V_{SS} and V_{DDA} referenced to V_{SSA}.

8/ The manufacturer supplying device types 01-02 has performed total ionizing dose (TID) testing in accordance with MIL-STD-883 Method 1019, Condition A. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 50 krad(Si).

9/ The manufacturer supplying device types 01-02 also performed single event effects (SEE) test at the Texas A&M University (TAMU) heavy ion radiation effects K500 super-conducting cyclotron with gold(Au) ion beam and observed no single event latch-up(SEL) occurs at an effective LET = 80 MeV-cm^2/mg. The Soft-reset Error Rate (SER) test detected the frequency of microcontroller soft-resets across a spectrum of heavy ion beams at supply voltage VDD = 3.0 V, temperature 25°C and onset LET= 45 MeV-cm^2/mg (saturated cross section $1.05x10^{-6}$ cm^2) and the calculated SER error rate of this device is $8.3x10^{-8}$ errors/device-day for Adams 90% worst case environment, Geosynchronous Orbit, 100 mils Aluminum shield in Space Radiation 6.0. For more information about SEE test, contact manufacturer.

10/ For internal NOR Flash Memory Only. Irradiated per MIL-STD-883 Method 1019.9 Condition C at 50-300 rad(Si)/s using an in-situ 900 rad(Si) device unpowered and 100 rad(Si) device statistically biased duty cycle repeated 50 times to achieve a TID level of 50 krad(Si). This irradiation in-situ biasing method is predicated on an application which may allow the device to be unpowered during 90% of the mission life.

11/ SEL characterization is performed at worst case voltage and temperature. V_{DD} = V_{DDA} = 3.6 V at ≥ 105°C.

12/ Contact Manufcaturer for additional information regarding the radiation related upsets and error rates.

13/ SEU characterization is performed at V_{DD} = V_{DDA} = 3.0 V at 25°C.

14/ The error rate calculation was performed using Adams 90% worst case environment, Geosynchronous Orbit, 100 mils Aluminum.

15/ Heavy Ion Soft-reset Error Rate (SER) is defined as an erroneous output signal from the microcontroller device that can be corrected by preforming one or more normal functions of the device. Soft errors can be generated from SEU, SEFI, MBU, MCU, and/or SET.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices
JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board
JESD78 – Standardized Test Procedure for Characterization of Latch-up in CMOS Integrated Circuits.

(Copies of these documents are available online at https://www.jedec.org/.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 2.

3.2.3 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.4 Timing definition for F/S mode of operation for I^2C bus. The timing definition for F/S mode of operation for I^2C bus shall be as specified on figure 4.

3.2.5 SPI Timing Diagram (Master Mode). The SPI Timing Diagram (Master Mode) shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +105°C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ $+3.0\ V \le V_{DDA} \le +3.6\ V$ unless otherwise specified	Group A Subgroups	Limits		Units
				Min	Max	
System clock frequency	f_{SYSCLK}		1, 2, 3	50 TYP		MHz
V_{DD} quiescent supply current	Q_{IDD}	All analog functions and peripherals in shutdown mode			6	mA
V_{DDA} supply current	Q_{IDDA}				5	mA
Active Digital Supply Current	A_{IDD}				80	mA
Active Analog Supply Current	A_{IDDA}				20	mA
I/O DC Characteristics 2/						
High level Input Voltage	V_{IH}	Vout ≥ $V_{OH(min)}$	1, 2, 3	2		V
Low Level Input Voltage	V_{IL}	Vout ≤ $V_{OL(max)}$			0.8	V
High Level Input Leakage Current	I_{IH}	$V_{IN} = V_{DD}$			1	µA
Low Level Input Leakage Current	I_{IL}	$V_{IN} = 0$ V		-1		µA
Input Capacitance 3/	C_{IO}		4		15	pF
High Level Output Voltage	V_{OH}	V_{DD} = min, I_{OL} = -100 µA	1, 2, 3	V_{DD} – 0.2		V
		V_{DD} = min, I_{OH} = -8 mA		2.4		V
Low Level Output Voltage	V_{OL}	V_{DD} = min, I_{OL} = 100 µA			0.2	V
		V_{DD} = min, I_{OL} = 8 mA			0.4	V
Output short circuit current 5/	I_{OS}	V_{OUT} = 0 V or $V_{OUT} = V_{DD}$		-70	+70	mA
Input leakage; pull-up state	I_{INPU}	$V_{IN} = 0$ V		10	65	µA
Input leakage; pull-down state	I_{INPD}	$V_{IN} = V_{DD}$		-65	-10	µA
Analog High Level Input Leakage Current 6/	I_{IHA}	V_{IN} = 2.9 V			60	µA
High Level Input Leakage Current for DACx 7/	I_{IH_DAC}	$V_{IN} = V_{DD}$			35	µA
Analog Low Level Input Leakage Current for DACx 7/	I_{IL_DAC}	$V_{IN} = 0$ V		-10		µA
AC Characteristics 5/						
Rise time	t_r		9,10,11		5	ns
Fall time	t_f				5	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +105°C$ $+3.0\ V \leq V_{DD} \leq +3.6\ V$ $+3.0\ V \leq V_{DDA} \leq +3.6\ V$ unless otherwise specified	Group A Subgroups	Limits						Units
				Standard Mode		Fast Mode 18/		Fast Mode Plus 18/		
				Min	Max	Min	Max	Min	Max	
I^2C PIN Characteristics 2/ 8/ 9/ See FIGURE 3										
High Level Input Voltage	V_{IH}		1, 2, 3	0.7* V_{DD}		0.7* V_{DD}		0.7* V_{DD}		V
Low Level Input Voltage	V_{IL}			-0.5	0.3* V_{DD}	-0.5	0.3* V_{DD}	-0.5	0.3* V_{DD}	V
Input Leakage Current	I_{IH}	$0.1{*}V_{DD}$ < VIN < $0.9{*}V_{DD(max)}$		-10	+10	-10	+10	-10	+10	µA
Input Capacitance 3/	C_{IO}				10		10		10	pF
Low Level Output Voltage 5/	V_{OL}	V_{DD} > 2 V, I_{OL} = 3 mA (open-drain)		0	0.4	0	0.4	0	0.4	V
Low Level Output Current 5/	I_{OL}	V_{OL} = 0.4 V		3		3		20		mA
		V_{OL} = 0.6 V				6				mA
Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ 5/	t_{of}		9, 10, 11		250					ns
SCL clock frequency 5/	f_{SCL}			0	100	0	400	0	1000	kHz
Rise time 5/	t_r	For both SDA and SCL signals			1000		300		120	ns
Fall time 5/ 10/ 11/ 12/ 13/	t_f				300		300		120	ns
Low period of the SCL clock 5/	t_{LOW}			4.7		1.3		0.5		µs
High period of SCL clock 5/	t_{HIGH}			4.0		0.6		0.26		
Setup time for a repeated START condition 5/	$t_{SU;STA}$			4.7		0.6		0.26		
Data hold time 5/ 14/	$t_{HD;DAT}$			0		0		0		
Data setup time 5/	$t_{SU;DAT}$			250		100		50		
Setup time for STOP condition 5/	$t_{SU:STO}$			4.0		0.6		0.26		
Bus free time between a STOP and START condition 5/	t_{BUF}			4.7		1.3		0.5		
Data valid time 5/ 15/ 16/	$t_{VD;DAT}$				3.45		0.9		0.45	
Data valid time 5/ 16/ 17/	$t_{VD;ACK}$				3.45		0.9		0.45	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +105°C +3.0 V ≤ V_{DD} ≤ +3.6 V +3.0 V ≤ V_{DDA} ≤ +3.6 V unless otherwise specified	Group A Subgroups	Limits			Units
				Min	TYP	Max	
SPI I/O Characteristics See FIGURE 4							
SPI Clock frequency 5/	f_{SCK}		9, 10, 11			10	MHz
SPI clock period 5/	t_{SCK}			100			ns
SCK High Time 5/	t_H			50			
SCK Low Time 5/	t_L			50			
SCK Rise time 19/	t_r					25	
SCK Fall Time 19/	t_f					25	
Data input setup time wrt SCK edge 5/	t_{DS}			30			
Data input hold time wrt SCK edge 5/	t_{DH}			30			
Data out valid after SCK edge 5/	t_{VD}					30	
Data out rise time 5/	t_{DR}					30	
Data out fall time 19/	t_{DF}					30	
Data out hold time after SCK edge 5/	t_{HD}			5			
SSN low to first SCK edge 5/	$t_{SU(SSN)}$			1 SCLK Period			
Oscillator Characteristics - Internal Clock Source Characteristics							
Frequency 20/	f_{SYSCLK}		4,5,6		50	52	MHz
Duty Cycle 4/				40		60	%
Accuracy		Factory Trimmed		-4		+4	%
Internal Oscillator Startup 19/						6	µs
Oscillator Characteristics - External Clock Source Characteristics 2/							
Frequency 5/	f_{SYSCLK}		4,5,6		50	52	MHz
Duty Cycle 5/		Typical = 50%		40		60	%
External Clock input high level voltage		XTAL2 only		2			V
External Clock input low level voltage		XTAL2 only				0.8	V
Oscillator Characteristics – External Crystal Oscillator Characteristics							
Crystal Frequency 3/ 22/	f_{XOSC}		4			50	MHz
Maximum crystal transconductance 5/	G_m		4,5,6			80	mA/V
Supported crystal external load range 21/	C_{XOSCL}		4,5,6	8		16	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +105°C +3.0 V ≤ V_{DD} ≤ +3.6 V +3.0 V ≤ V_{DDA} ≤ +3.6 V unless otherwise specified		Group A Subgroups	Limits			Units
					Min	TYP	Max	
12-bit ADC Characteristics (Includes Analog Mux, PGA and AAF)								
Number of Channels 4/ 23/		Single-ended Input		7,8A,8B		16		bits
		Differential Input				8		
Resolution 4/ 23/	Nbits					12		
Modulator Conversion Clock Frequency 4/ 23/	f_{ADCK}						12.5	MHz
Integral Nonlinearity 4/ 23/	INL_{ADC}	PGA Gain = 1	Differential Input		-4		+4	LSB
			Single-Ended Input		-4		+22	
Differential Nonlinearity 4/ 23/	DNL_{ADC}	PGA Gain = 1	Differential Input		-1.5		+1.5	
			Single-Ended Input		-1.2		+2	
Offset Error 4/ 23	E_{OFF}	PGA Gain = 1	Differential Input		-50		50	
			Single-Ended Input		-50		50	
Gain Error 4/ 23/	GE_{ADC}	PGA Gain = 1			-4		+1	%
Offset Temperature Coefficient 5/	T_{COFF}			1,2,3			15	ppm/°C
Signal-to-Noise Ratio 4/	SNR	PGA Gain = 1, -3 dBFS, FIN = 1 kHz sine wave	Differential Input	4,5,6	68	70		dB
			Single-Ended Input		58	60		
Total Harmonic Distortion 5/	THD	PGA Gain = 1, -3 dBFS, FIN = 1 kHz sine wave				-70	-65	
Conversion Time 5/ 24/	t_{CONV}	Single-Shot Mode or Auto-Sequence (from start of convert command)		9,10,11		125		ADCK Cycles
Initiation Time 5/ 24/ 25/		After enable, PGA Gain = 1				1250		ADCK Cycles
Effective Number of Bits 4/	ENOB	10kHz sine wave, PGA Gain = 1, V_{CM} = 1.0 V	Differential Input	4,5,6	10	11		bit
			Single-Ended Input		9	9.5		
Input Signal Range 4/ 23/ 26/		PGA Gain = 1, Vcm = 1.0 V	Differential Input	7,8A,8B		±1.5		Vp-p
			Single-Ended Input		0		1.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +105°C +3.0 V ≤ V_{DD} ≤ +3.6 V +3.0 V ≤ V_{DDA} ≤ +3.6 V unless otherwise specified	Group A Subgroups	Limits			Units
				Min	TYP	Max	
12-bit ADC Characteristics (Includes Analog Mux, PGA and AAF) - Continued							
Supply Current 5/ 27/		Full signal path	1,2,3			14	mA
Power Supply Rejection 4/		DC		46		48	dB
Common Mode Rejection 5/		DC; Only applies to differential input signals		60			dB
Input Common Mode Range 4/		Differential Input		0.4		1.4	V
MUX							
Switch On Resistance 5/	RSW	Gain = ½	1,2,3		267	300	kΩ
		1			200		
		2			133		
		4			80		
		8			44		
		16			24		
Input Capacitance 4/ 28/			4			16	pF
Channel-to-Channel Crosstalk 4/		Differential input, Input Frequency=10 kHz	4,5,6	-70			dB
Input Settling Time 5/ 29/		From input of mux to ADC to settle within 1/2 – LSB accuracy	9,10,11	12	20	28	μs
PGA and AAF							
Programmable Gain Range 4/ 23/ 30/			7,8A,8B	0.5		16	V/v
Filter Flatness 5/		Through 50 kHz baseband	4,5,6		±0.5	±1	dB
Attenuation, Filter Stopband 5/		Input Frequency = 150 kHz			-3		
		600 kHZ			-36		
		1.5 MHz			-60		
		6 MHz			-90		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +105°C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ $+3.0\ V \le V_{DDA} \le +3.6\ V$ unless otherwise specified	Group A Subgroups	Limits			Units
				Min	TYP	Max	
12-bit DAC Characteristics - Static Performance							
Resolution 4/ 23/	Nbits		7,8A,8B	12			bits
Reference Voltage 5/	V_{REF_DAC}		1,2,3		2.4		V
Update rate 5/ 23/			7,8A,8B			100	kHz
Integral Nonlinearity 4/ 23/ 32/	INL_{DAC}			-4	±0.7	4	LSB
Differential Nonlinearity 4/ 23/ 32/	DNL_{DAC}			-3	±0.4	3	LSB
Gain Error 4/	G_{E_DAC}		1,2,3	-2.5	±0.2	2.5	%FSR
Gain Error Drift 5/	ΔG_{E_DAC}/°C				-3		ppm/°C
Offset Error 4/	V_{OS}	Code = 0x014		-50		50	LSB
Offset Error Drift 5/	ΔV_{OS}/°C				8	20	ppm/°C
Output Impedance in Shutdown Mode 5/	$ROUT_{sh}$				100	200	kΩ
Supply rejection ratio 5/	PSRR+	static DC measurement		37		43	dB
Output Noise 5/	ONoise	No External Output Filter	4,5,6		250		µVrms
		With external 10 kHz Output Filter			128		
		With external 100 kHz Output Filter			41		
Dynamic Performance							
Voltage Output Slew Rate 4/		Load = 5 kΩ//40 pF	9,10,11			1	V/µs
Output settling time to ½ LSB 5/ 33/		Load = 5 kΩ//40 pF			10		µs
Output voltage swing 4/ 23/		Load = 5 kΩ//40 pF		0		VREF - 1LSB	
Startup time 5/		From EN pin transitions low-to-high to valid VOUT value			10		µs
Max capacitance load for stability 5/		With or without R_L = 5 kΩ				40	pF
Power Dissipation (each DAC)							
Analog Supply Current 5/	I_{ADAC}	Code = 0xFFF, Load = 5 kΩ//40 pF	1,2,3	1.4	1.45	1.5	mA
Digital Supply Current 5/	I_{DDAC}	Frequency=100 kHz with updates to DAC0 and DAC1 data registers				1.5	mA
Analog + Digital Supply Current during Shutdown 5/	I_{SHDN}				35	300	nA
Output Short Circuit Current 5/	I_{SCDAC}	DACx pin shorted to either V_{DDA} or V_{SSA}			15	22	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +105°C$ $+3.0\ V \leq V_{DD} \leq +3.6\ V$ $+3.0\ V \leq V_{DDA} \leq +3.6\ V$ unless otherwise specified	Group A Subgroups	Limits			Units
				Min	TYP	Max	
Comparator Characteristics - 31/							
Input Common-Mode Voltage Range 3/	V_{CMR}		1,2,3	0.0		V_{DDA}	V
Input-Referred Hysteresis 3/ 34/	V_{HYS}	$V_{CM} = V_{DDA}$	4,5,6	15	35	110	mV
		$V_{CM} = V_{DDA}/2$		5	20	35	mV
		$V_{CM} = 0\ V$		8	14	25	mV
Input-Referred Positive Trip Point 3/ 34/ 35/	V_{TRIP+}	$V_{CM} = V_{DDA}$		2		52	mV
		$V_{CM} = V_{DDA}/2$		1		20	
		$V_{CM} = 0\ V$		4		11	
Input-Referred Negative Trip Point 3/ 34/ 35/	V_{TRIP-}	$V_{CM} = V_{DDA}$		-2		-52	mV
		$V_{CM} = V_{DDA}/2$		-1		-20	
		$V_{CM} = 0\ V$		-4		-11	
Input Offset Voltage 3/ 36/	V_{OS}	$V_{CM} = 0\ V$, or $V_{CM} = V_{DDA}/2$, or $V_{CM} = V_{DDA}$	1,2,3	0		10	mV
Common-Mode Rejection Ratio 3/ 37/	CMRR	$V_{DDA} = 3.3V$, $V_{CM} = -0.1V$ and 3.4V			1.5	4	mV/V
Power-Supply Rejection Ratio 3/ 38/	PSRR	$V_{CM} = V_{DDA}/2$			1	2	mV/V
Propagation Delay 5/ 23/	t_{PD}	Overdrive = 10 mV	9,10,11	55	80	110	ns
Propagation-Delay Skew 5/ 39/	t_{SKEW}	Overdrive = 100mV		-100		100	ns
Pulse Width Modulator Characteristics 4/							
Maximum period count		16-bit	9,10,11	2		65535	Counts
Dead band Range				20		81920	
Clock Prescalar Range				1		256	
Timer/Counter Characteristics 5/ 23/							
Maximum possible count		32-bit register	7,8A,8B			4.3E9	Count
UART Characteristics 5/ 23/ 40/							
Baud rate			9,10,11	600		115200	Bd/s

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +105°C$ $+3.0\ V \leq V_{DD} \leq +3.6\ V$ $+3.0\ V \leq V_{DDA} \leq +3.6\ V$ unless otherwise specified	Group A Subgroups	Limits			Units
				Min	TYP	Max	
Power-on-Reset Characteristics 2/ 5/							
Reset Delay Time	t_{RD}		9,10,11	16		128	ms
V_{DD} Threshold Range	V_{DD_RTH}			1.30		2.60	V
V_{DDA} Threshold Range	V_{DDA_RTH}			1.30		2.60	V
Temperature Monitor 3/ 23/ 42/							
Nonlinearity			1,2,3	-4		5	°C
Absolute Accuracy						12	°C
Gain				-3.2			mV/°C
Offset		Temp = 0 °C		-1.2			V
Power				68		103	µA
Precision Current Source							
Source Current 5/	Iout		1,2,3		1		mA
Current Precision		Typ = 1.0 mA, +25°C		-1.5		1.5	%FS
Enable delay to Iout 5/	$t_{EDILH(1)}$					100	ns
Current Drift Over Temperature				-5.0		+5.0	%FS

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

1/ RHA parts supplied to this drawing have been characterized through all levels M, D, P and L of irradiation. However, this device is only tested at the 'L' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ All voltages referenced to V_{SS}.
3/ Characterized only for initial qualification and after any design or process changes which may affect this parameter.
4/ Guaranteed by characterization (for DAC INL and DNL using code 21 – 4095).
5/ Guaranteed by design, not production tested.
6/ Refers to AIN14 and AIN15 pins only.
7/ Refer to DACx pins only.
8/ See the I2C-Bus specification in manufacturer UM10204 for details.
9/ All related AC (timing) related parameters tested with a load capacitance of 50 pF.
10/ A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
11/ Cb = total capacitance of one buse line in pF. Max of 400 pF in Standard- and Fast-Modes, and 550 pF in Fast-Plus Mode.
12/ The maximum tf for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage tf is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
13/ In Fast-Mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
14/ $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
15/ $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
16/ $t_{HD;DAT}$ could be 3.45 us and 0.9 us for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or tVD;ACK by a transistion time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
17/ $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
18/ Compatible with Fast Mode and Fast Mode Plus specifications.
19/ Provided as a design limit only, neither production tested or guaranteed.
20/ Min value based on divider setting. See User manual for details
21/ Provided as a design limit only, neither production tested or guaranteed.
22/ Guaranteed by characterization using Statek CX1HGSM crystal.
23/ Functionally tested during production.
24/ Assumes clock for ADC (ADCK) = 12.5 MHz. See UT32M0R500 User Manual for details.
25/ Initiation time is a time necessary for the ADC to achieve full accuracy. It is time after the ADC and PGA are enabled6(power-up) and a PGA gain is selected. This includes the multiplexer settling time.
26/ Single-ended input is referenced to VSSA.
27/ Highest power supply current dissipation is at highest temperature, highest voltage.
28/ Includes capacitance from I/O.
29/ Settling time is the time required from when an analog input is selected at the AMUX, which will settle to 12-bit accuracy, until the CONVERT command should be received by the ADC to begin a conversion operation.
30/ Gain range has discrete levels of 0.5, 1, 2, 4, 8, and 16.
31/ All voltages referenced to V_{SSA}.
32/ ±1LSB = ±0.0244% of Full Scale = ±244 ppm. Full Scale = 2.4 V.
33/ Settling time with change from code 0xFFF to 0x014. Time measured from rising edge of data word to within ±0.5LSB of final value with a load = 40 pF.
34/ The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis.
35/ The input-referred trip points are the limits of the differential input voltage (for Vcm = 0.0) required to make the comparator output change state.
36/ The Input Offset Voltage is defined as the mean of the trip points. Vos = (VTRIP+ - VTRIP-)/2.
37/ CMRR = (V_{OSL}-V_{OSH}) / 3.5V, where V_{OSL} is the offset at VCM = -0.1V and V_{OSH} is the offset at VCM = 3.4V.
38/ PSRR = (V_{OS3} - $V_{OS3.6}$) / 0.6V where V_{OS3} is the offset voltage with V_{DDA} =3V, and $V_{OS3.6}$ is the offset voltage with V_{DDA} = 3.6V.
39/ Propagation Delay Skew is the difference between t_{PDLH} and t_{PDHL}.
40/ Provided as a design guideline, not production tested or guaranteed.
41/ If V_{DDC} (internally generated core voltage) is below V_{DDC_BO} for longer than t_{VDDC_BO}, the POR may re-enter the reset state.
42/ PGA gain at 16x.

Table IB. SEP test limits. 1/ 2/ 3/

Device type	$V_{DD} = V_{DDA}$ = 3.0 V 3/		Bias V_{DD} = 3.6 V For SEL test and observed No SEL occurs at effective LET
	Soft Reset Event Rate (events/device-day)	Saturated Cross-Section (cm^2/device)	
All	8.30×10^{-8} errors/device-day	1.05×10^{-6} cm^2	LET ≤ 80 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ The manufacturer supplying device types 01-02 also performed single event effects (SEE) test at the Texas A&M University (TAMU) heavy ion radiation effects K500 super-conducting cyclotron with gold (Au) ion beam and observed no single event latch-up (SEL) occurs at an effective LET = 80 MeV-cm^2/mg. The Soft-reset Error Rate (SER) test detected the frequency of microcontroller soft-resets across a spectrum of heavy ion beams at supply voltage V_{DD} = 3.0 V, temperature 25°C and onset LET= 45 MeV-cm^2/mg (saturated cross section 1.05×10^{-6} cm^2) and the calculated SER error rate of this device is 8.3×10^{-8} errors/device-day for Adams 90% worst case environment, Geosynchronous Orbit, 100 mils Aluminum shield in Space Radiation 6.0. For more information about SEE test, contact manufacturer.

Case outline X

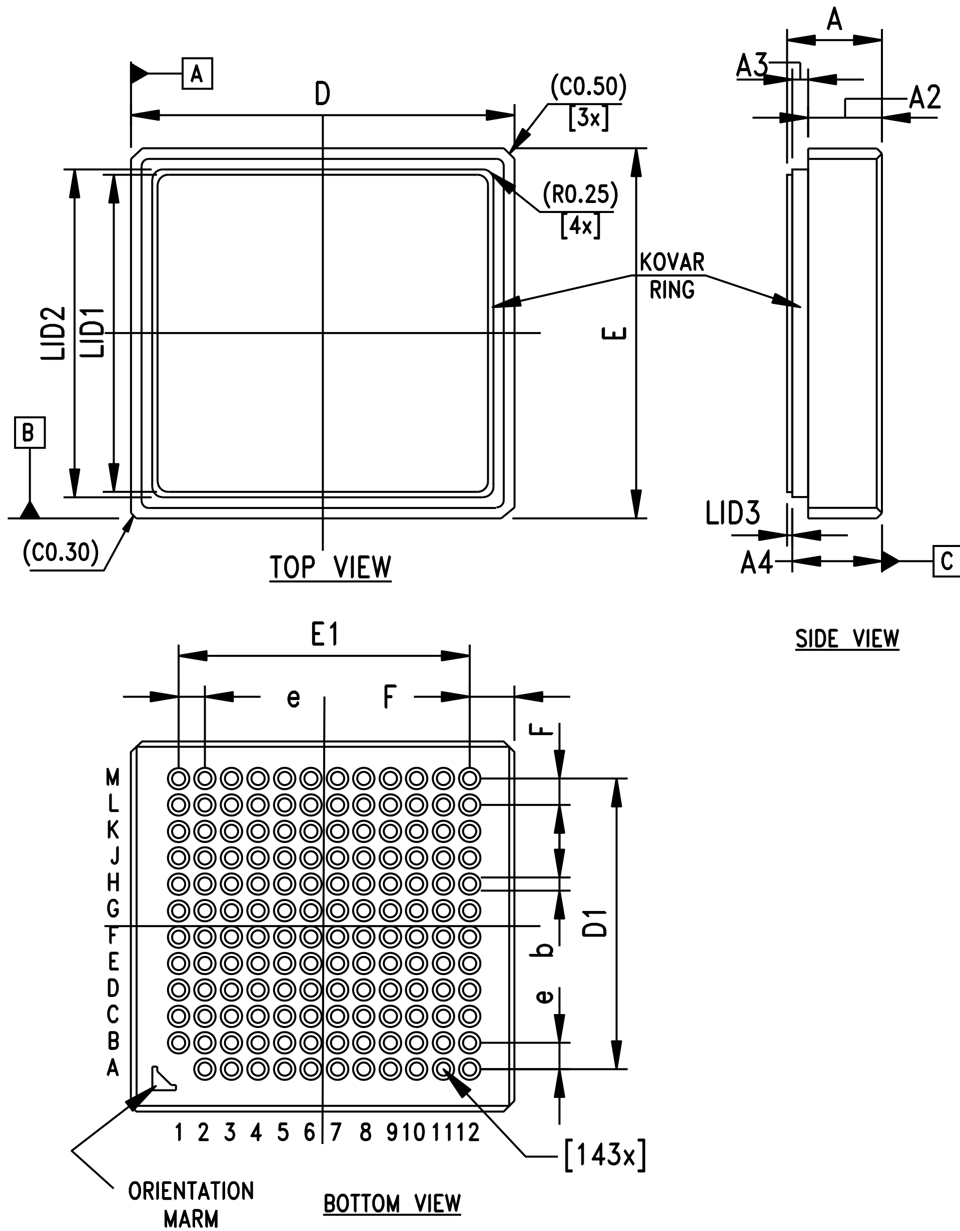


FIGURE 1. Case outline X. - Ceramic Land Grid Array (CLGA)

Case outline X – Continued.

Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		5.28	D1/E1	10.87	11.13
A2	3.60	4.40	e	0.95	1.05
A3	0.60	0.70	F	1.75 TYP	
A4	4.20	5.10	LID1	12.38	12.47
b	0.75	0.85	LID2	12.81	13.07
D/E	14.35	14.65	LID3	0.124	0.130

Notes:
1. Material is 90% Minimum Alumina.
2. Units are Millimetres.
3. LID is connected to VSS
4. Exposed-Metal Platting PER MIL-PRF-38535.
    a. NICKEL BASE: Electro-Plated 2.54 – 8.89 µm.
    b. GOLD: Electro-Plated 2.54 – 5.72 µm

FIGURE 1. <u>Case outline</u> X - Continued.

Case outline Y.

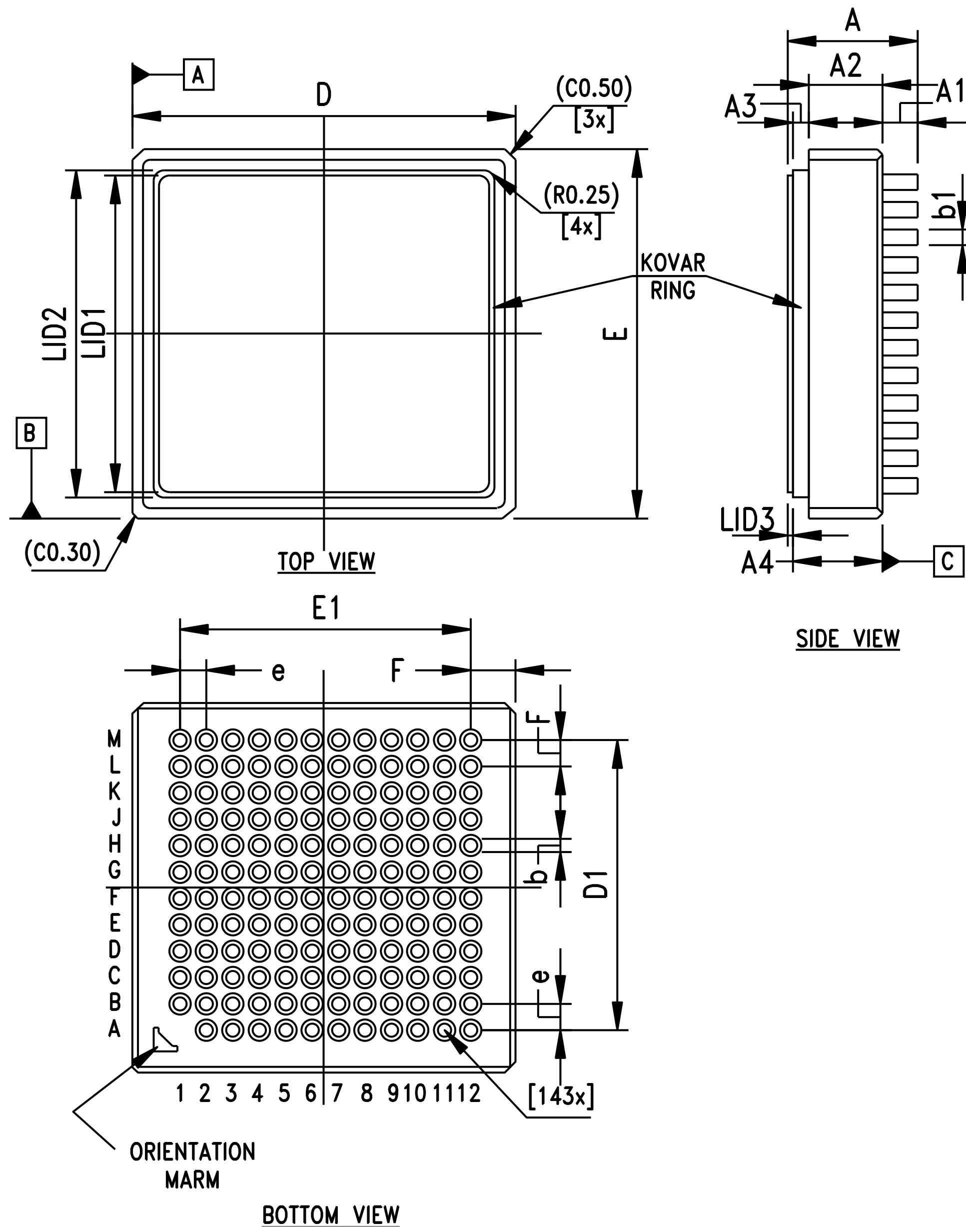


FIGURE 1. Case outline Y. - Ceramic Column Grid Array (CCGA)

Case outline Y - Continued.

Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		7.69	D/E	14.35	14.65
A1	2.01	2.41	D1/E1	10.87	11.13
A2	3.60	4.40	e	0.95	1.05
A3	0.60	0.70	F	1.75 TYP	
A4	4.20	5.10	LID1	12.38	12.47
b	0.75	0.85	LID2	12.81	13.07
b1	0.51	0.61	LID3	0.124	0.130

Notes:

1. Material is 90% Minimum Alumina.
2. Units are Millimetres.
3. LID is connected to VSS
4. Exposed-Metal Platting PER MIL-PRF-38535.
   a. NICKEL BASE: Electro-Plated 2.54 – 8.89 µm.
   b. GOLD: Electro-Plated 2.54 – 5.72 µm

FIGURE 1. Case outline Y - Continued.

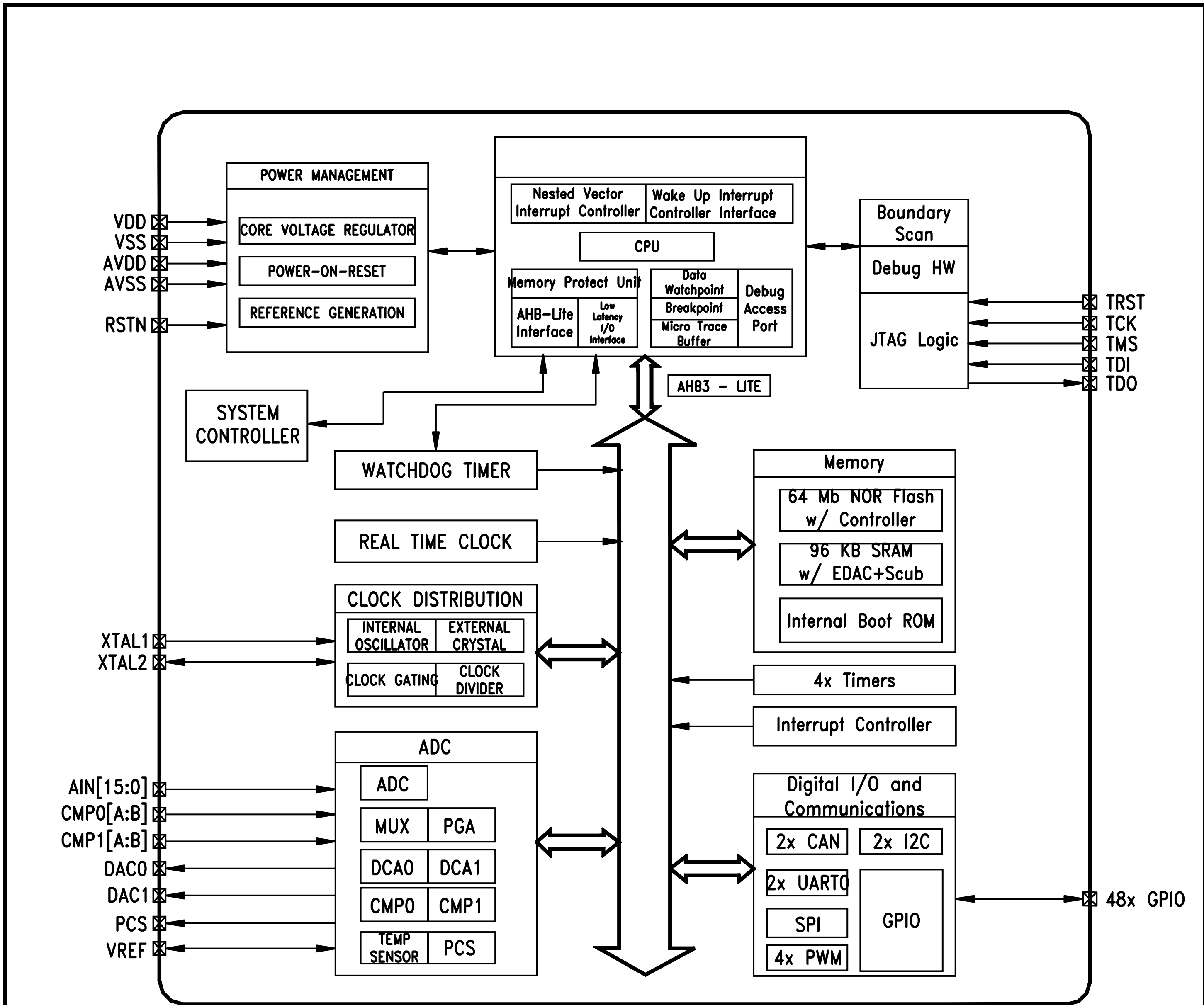


FIGURE 2. Block diagram.

	12	11	10	9	8	7	6	5	4	3	2	1	
M	AIN11	AIN14	AIN15	PCS	BOOTCFG[0]	UART0_RXD	UART0_TXD	CAN0_TXD	CAN0_RXD	SSN/GPIO43	MISO/GPIO42	MOSI/GPIO41	M
L	AIN10	AIN13	CLKSEL	VSSA	VDDA	TMS	TCK	Reserved	TDO	GPIO15	GPIO14	SCLK/GPIO40	L
K	AIN9	AIN12	RSTN	VSSA	VDDA	BOOTCFG[1]	Reserved	TDI	TRST	GPIO13	GPIO12	SDA1/GPIO39	K
J	AIN8	AIN7	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO11	GPIO10	SCL1/GPIO38	J
H	AIN3	AIN6	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO9	GPIO8	XTAL1	H
G	AIN2	AIN5	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO7	GPIO6	XTAL2	G
F	AIN1	AIN4	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO5	GPIO4	SDA0/GPIO37	F
E	AIN0	Reserved	Reserved	VSSA	VDDA	VDD	VSS	VDD	VSS	GPIO3	GPIO2	SCL0/GPIO36	E
D	DAC0	CMP1+	LDO15_BYP	VSSA	VDDA	VSSA	VDDA	VDD	VSS	GPIO1	GPIO0	UART1_RXD/GPIO35	D
C	DAC1	CMP1–	LDO28_BYP	VSSA	VDDA	VSSA	VDDA	VSS	Reserved	PWM3/GPIO47	PWM2/GPIO46	UART1_TXD/GPIO34	C
B	CMP0+	Reserved	GPIO16/INTR17	GPIO17/INTR18	GPIO18/INTR19	GPIO19 INTR20	GPIO20/INTR21	GPIO21/INTR22	GPIO22/INTR23	PWM1/GPIO45	PWM0/GPIO44	CAN1_TXD/GPIO33	B
A	CMP0–	GPIO24/CMP0OU	GPIO25/CMP1OUT	GPIO26/RTCK	GPIO27/SSN1	GPIO28/SSN2	GPIO29	GPIO30	GPIO31	GPIO23/INTR24	CAN1_RXD / GPIO32		A
	12	11	10	9	8	7	6	5	4	3	2	1	

FIGURE 3. Terminal Connection.

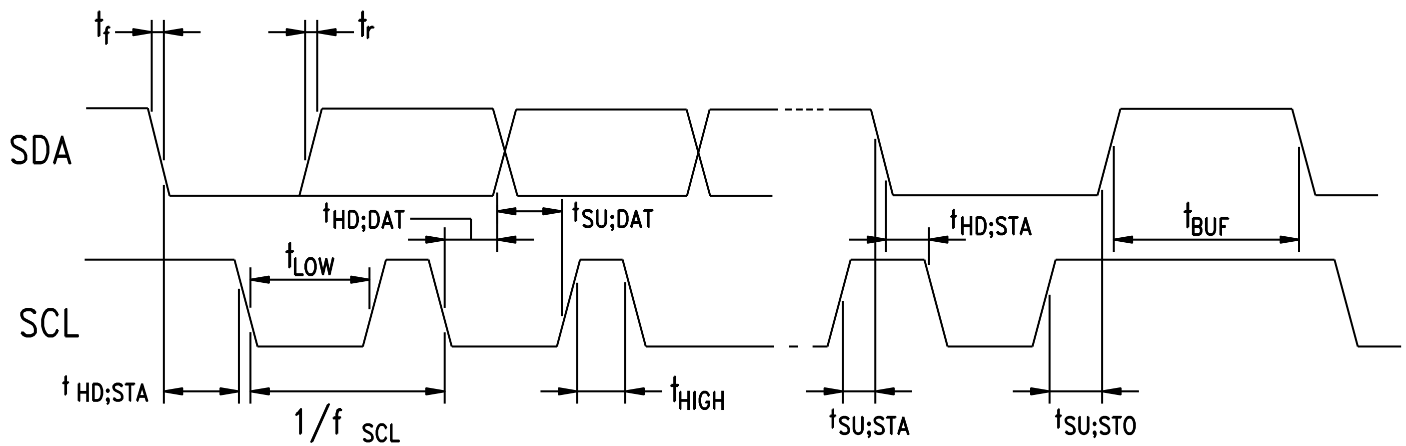


FIGURE 4. Timing definition for F/S mode of operation for I²C bus.

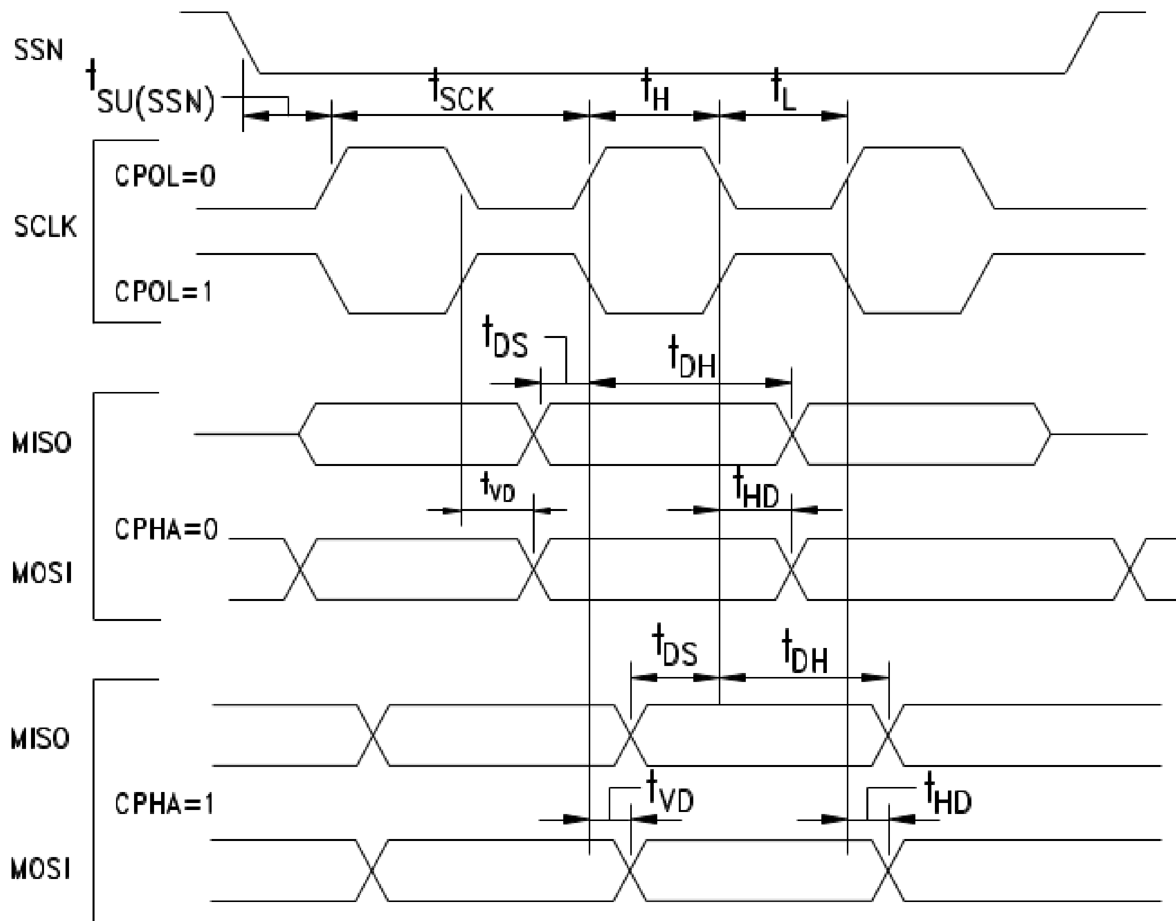


FIGURE 5. SPI Timing Diagram (Master Mode).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device type 02.

(1) 100% internal visual, method 2010 condition A of MIL-STD-883.
(2) 100% PIND (Single pass).
(3) Serialization.
(4) Group A end-points electrical.
(5) Dynamic burn-in at +125°C for 240 hours or equivalent, deltas, PDA (3%) for Functional Test only, and PDA (5%) for DC and Functional Test combined.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1, 7, 9
Static burn-in I and II (method 1015)	Not Required	Required
Dynamic burn-in (method 1015)	Required	Required
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4) 4/	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Post-column attach electrical parameters test (see 4.2) 5/	1	1

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters.
4/ For CGA package, Group D test shall be performed all applicable LGA level test and in addition column destructive pull test and salt atmosphere test method (TM 1009) is required.
5/ For CGA package solderability test shall be performed in accordance with test method 2003.

TABLE IIB. Delta limits at +25°C.

Parameter	Delta Limit 1/	Unit
Supply current Q_{IDD}	±1.1 mA of previous measured value	mA

1/ The above parameter shall be recorded before and after the required burn-in and life-test.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C. The latchup test temperature shall be at the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = V_{DDA} = 3.0 V dc for the upset measurements and V_{DD} = V_{DDA} = 3.6 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-04-23

Approved sources of supply for SMD 5962-17212 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L1721201QXC	65342	UT32M0R500-ZQC
5962L1721202QXC	65342	UT32M0R500-ZQC
5962L1721201QYF 3/	65342	UT32M0R500-SQF
5962L1721202QYF 3/	65342	UT32M0R500-SQF

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Devices listed on this drawing are supplied to lead finish “F”. The solder column material copper wound and solder coated and is of compositions of tin (Sn) 63% and lead (Pb) 37%.

Vendor CAGE number	Vendor name and address
65342	Cobham Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.