| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Make correction to note 3 in Figure 1 for case outline X. -rrp | 19-01-15 | C. SAFFLE |

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | A | A | A | A | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | | | | | | | | | | | | | | | |

| REV STATUS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
RICK OFFICER

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**http://www.dla.mil/landandmaritime**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
17-02-02

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, LOW VOLTAGE 1:10 LVPECL WITH SELECTABLE INPUT CLOCK DRIVER, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-16207** |

SHEET 1 OF 18

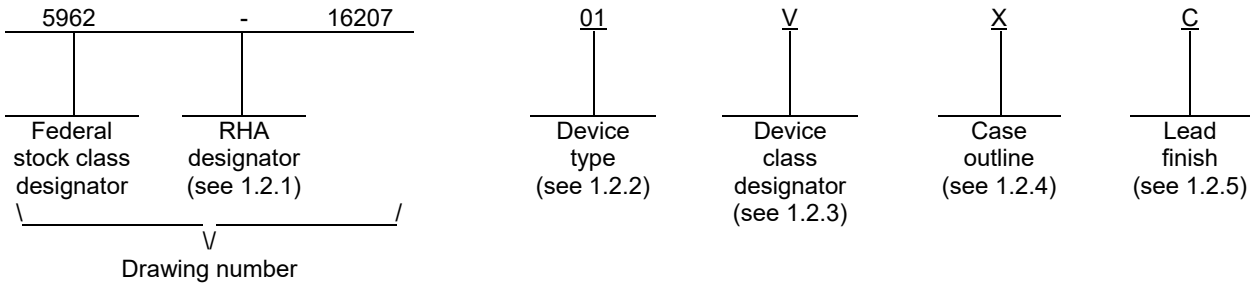
DSCC FORM 2233
APR 97

5962-E149-19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | CDCLVP111 | Low voltage 1:10 low voltage positive emitter coupled logic (LVPECL) with selectable input clock driver |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | See figure 1 | 36 | Quad leaded chip carrier style with non-conductive tie bar |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply voltage ($V_{CC}$) (relative to $V_{EE}$) | -0.3 V to 4.6 V |
| Input voltage ($V_{IN}$) | -0.3 V to $V_{CC}$ + 0.5 V |
| Output voltage ($V_{OUT}$) | -0.3 V to $V_{CC}$ + 0.5 V |
| Input current ($I_{IN}$) | ±20 mA |
| Negative supply voltage ($V_{EE}$) (relative to $V_{CC}$) | -4.6 V to 0.3 V |
| Sink/source current ($I_{BB}$) | -1 mA to 1 mA |
| DC output current ($I_O$) | -50 mA |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Maximum operating junction temperature ($T_J$) | +125°C |
| Thermal resistance, junction-to-case (top) ($R\theta_{JC}$) (top) | 33.2°C/W |
| Thermal resistance, junction-to-ambient ($R\theta_{JA}$) | 107.2°C/W 2/ |
| Thermal resistance, junction-to-board ($R\theta_{JB}$) | 98.9°C/W |
| Characterization parameter, junction-to-top ($\psi_{JT}$) | 29.2°C/W |
| Characterization parameter, junction-to-board ($\psi_{JB}$) | 91.36°C/W |
| Thermal resistance, junction-to-case (bottom) ($R\theta_{JC}$) (bot) | 13.4°C/W |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{CC}$) (relative to $V_{EE}$) | 2.375 V to 3.8 V |
| Ambient operating temperature range ($T_A$) | -55°C to +125°C |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ According to JESD 51-7 standard.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC Solid State Technology Association

EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions<br>$-55°C \le T_A \le +125°C$<br>$V_{SUPPLY}$: $V_{CC}$ = 0 V,<br>$V_{EE}$ = -2.375 V to -3.8 V,<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DC electrical characteristics. | | | | | | | |
| Supply internal current | $I_{EE}$ | Absolute value of current | 1,2,3 | 01 | 30 | 85 | mA |
| Output and internal supply current | $I_{CC}$ | All outputs terminated 50 Ω to $V_{CC}$ – 2 V | 1,3 | 01 | | 385 | mA |
| | | | 2 | | | 405 | |
| Input current | $I_{IN}$ | Includes pull up/pull down resistors, $V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ – 2 V | 1,2,3 | 01 | -150 | 150 | µA |
| Internally generated bias voltage | $V_{BB}$ | $V_{EE}$ = -3 V to -3.8 V, $I_{BB}$ = -0.2 mA | 1,2,3 | 01 | -1.45 | -1.125 | V |
| | | $V_{EE}$ = -2.375 V to -2.75 V, $I_{BB}$ = -0.2 mA | | | -1.3 | -1.1 | |
| High level input voltage (CLK_SEL) | $V_{IH}$ | | 1,2,3 | 01 | -1.165 | -0.88 | V |
| Low level input voltage (CLK_SEL) | $V_{IL}$ | | 1,2,3 | 01 | -1.81 | -1.475 | V |
| Input amplitude voltage (CLKn, $\overline{\text{CLKn}}$ ) | $V_{ID}$ | Difference of input, $\lvert V_{IH} - V_{IL} \rvert$ 2/ | 1,2,3 | 01 | 0.5 | 1.3 | V |
| Common mode voltage (CLKn, $\overline{\text{CLKn}}$ ) | $V_{CM}$ | DC offset relative to $V_{EE}$ | 1,2,3 | 01 | $V_{EE}$ + 1 | -0.3 | V |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = -21 mA | 1 | 01 | -1.2 | -0.85 | V |
| | | | 2 | | -1.15 | -0.8 | |
| | | | 3 | | -1.26 | -0.85 | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = -5 mA | 1 | 01 | -1.85 | -1.425 | V |
| | | | 2,3 | | -1.85 | -1.25 | |
| Differential output voltage swing | $V_{OD}$ | Terminated with 50 Ω to $V_{CC}$ – 2 V, see figure 4 | 1,2,3 | 01 | 350 | | mV |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions<br>$-55°C \le T_A \le +125°C$<br>$V_{SUPPLY}$: $V_{CC}$ = 2.375 V to 3.8 V,<br>$V_{EE}$ = 0 V,<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DC electrical characteristics - continued. | | | | | | | |
| Supply internal current | $I_{EE}$ | Absolute value of current | 1,2,3 | 01 | 30 | 85 | mA |
| Output and internal supply current | $I_{CC}$ | All outputs terminated 50 Ω to $V_{CC}$ – 2 V | 1,3 | 01 | | 385 | mA |
| | | | 2 | | | 405 | |
| Input current | $I_{IN}$ | Includes pull up/pull down resistors,<br>$V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ – 2 V | 1,2,3 | 01 | -150 | 150 | µA |
| Internally generated bias voltage | $V_{BB}$ | $V_{CC}$ = -3 V to -3.8 V,<br>$I_{BB}$ = -0.2 mA | 1,2,3 | 01 | $V_{CC}$ -1.45 | $V_{CC}$ -1.125 | V |
| | | $V_{CC}$ = 2.375 V to 2.75 V,<br>$I_{BB}$ = -0.2 mA | | | $V_{CC}$ -1.3 | $V_{CC}$ -1.1 | |
| High level input voltage (CLK_SEL) | $V_{IH}$ | | 1,2,3 | 01 | $V_{CC}$ -1.165 | $V_{CC}$ -0.88 | V |
| Low level input voltage (CLK_SEL) | $V_{IL}$ | | 1,2,3 | 01 | $V_{CC}$ -1.81 | $V_{CC}$ -1.475 | V |
| Input amplitude voltage (CLKn, $\overline{CLKn}$ ) | $V_{ID}$ | Difference of input, $\lvert V_{IH} - V_{IL} \rvert$ 2/ | 1,2,3 | 01 | 0.5 | 1.3 | V |
| Common mode voltage (CLKn, $\overline{CLKn}$ ) | $V_{CM}$ | DC offset relative to $V_{EE}$ | 1,2,3 | 01 | 1 | $V_{CC}$ -0.3 | V |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = -21 mA | 1 | 01 | $V_{CC}$ -1.2 | $V_{CC}$ -0.85 | V |
| | | | 2 | | $V_{CC}$ -1.15 | $V_{CC}$ -0.80 | |
| | | | 3 | | $V_{CC}$ -1.26 | $V_{CC}$ -0.85 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions<br>$-55°C \le T_A \le +125°C$<br>$V_{SUPPLY}$: $V_{CC}$ = 2.375 V to 3.8 V,<br>$V_{EE}$ = 0 V,<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DC electrical characteristics - continued. | | | | | | | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = -5 mA | 1 | 01 | $V_{CC}$ -1.85 | $V_{CC}$ -1.425 | V |
| | | | 2,3 | | $V_{CC}$ -1.85 | $V_{CC}$ -1.25 | |
| Differential output voltage swing | $V_{OD}$ | Terminated with 50 Ω to $V_{CC}$ – 2 V, see figure 4 | 1,2,3 | 01 | 350 | | mV |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions<br>$-55°C \le T_A \le +125°C$<br>$V_{SUPPLY}$: $V_{CC}$ = 0 V,<br>$V_{EE}$ = -2.375 V to -3.8 V,<br>unless otherwise specified<br>or<br>$V_{SUPPLY}$: $V_{CC}$ = 2.375 V to 3.8 V,<br>$V_{EE}$ = 0 V,<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| AC electrical characteristics. | | | | | | | |
| Differential propagation delay CLKn, $\overline{CLKn}$ to all Q0, $\overline{Q0}$ ..Q9, $\overline{Q9}$ | $t_{pd}$ | | 9,10,11 | 01 | 100 | 355 | ps |
| Output to output skew | $t_{sk(o)}$ | See figure 5 | 9,10,11 | 01 | | 50 | ps |
| Additive phase jitter | $t_{aj}$ | Integration bandwidth of 20 kHz to 20 MHz, fout = 200 MHz at 25°C | 9,10,11 | 01 | | < 0.8 | ps |
| Maximum frequency | $f_{(max)}$ | Functional up to 3.5 GHz, see figure 4 | 9,10,11 | 01 | | 3500 | MHz |
| Output rise and fall time (20%, 80%) | $t_r$ / $t_f$ | See note 4 in figure 5 | 9,10,11 | 01 | | 240 | ps |

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $V_{ID}$ minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum $V_{ID}$ of 100 mV.

Case outline X

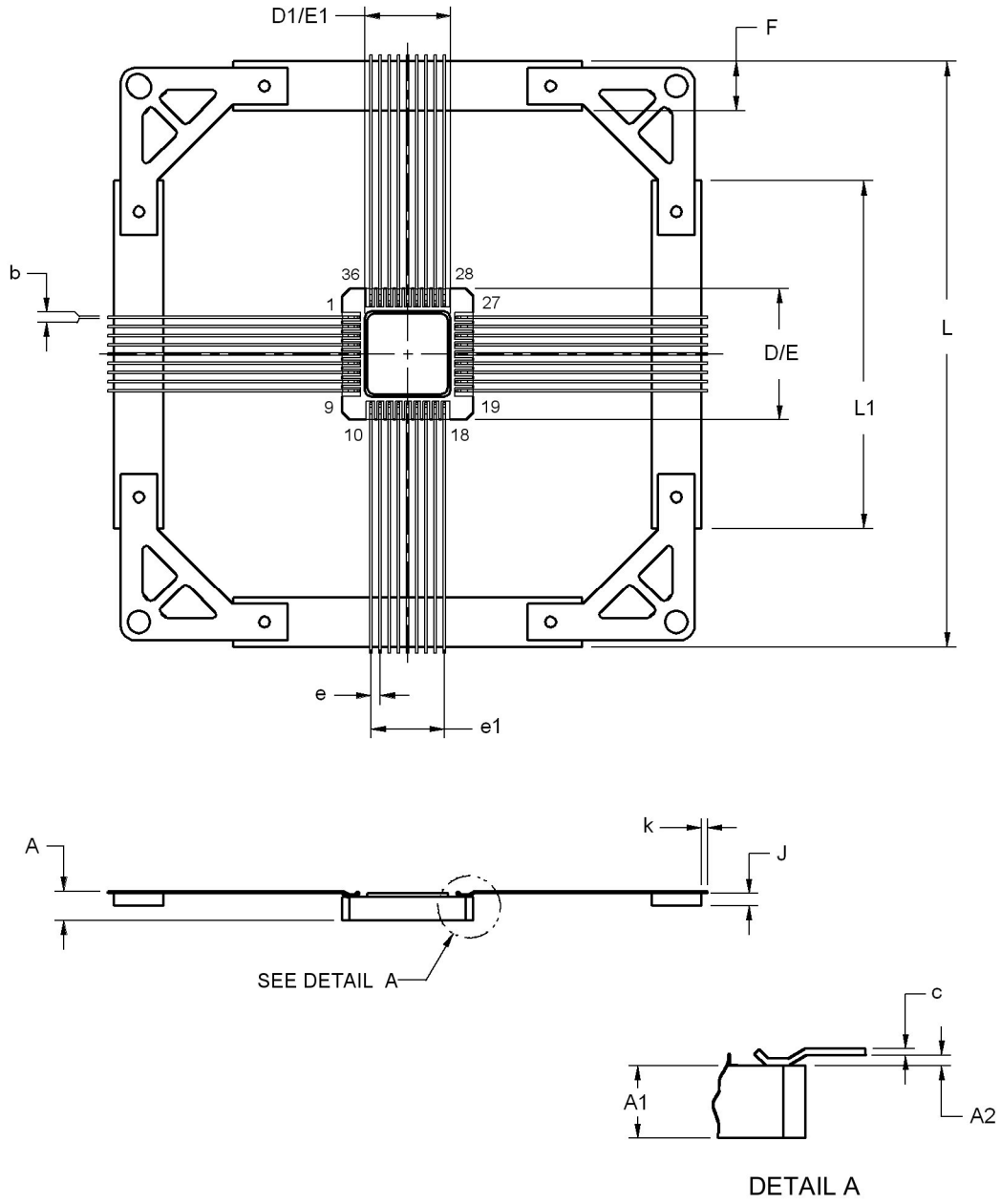



FIGURE 1. Case outline.

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | --- | .0875 | --- | 2.224 |
| A1 | --- | .0659 | --- | 1.674 |
| A2 | .0019 | .0141 | 0.05 | 0.36 |
| b | .0058 | .0097 | 0.148 | 0.248 |
| c | .0039 | .0078 | 0.1 | 0.2 |
| D/E | .3495 | .3652 | 8.878 | 9.278 |
| D1/E1 | .2337 | --- | 5.938 | --- |
| e | .0249 BSC | | 0.635 BSC | |
| e1 | .1999 BSC | | 5.08 BSC | |
| F | .1349 | --- | 3.429 | --- |
| J | .0354 | --- | 0.9 | --- |
| k | --- | .0196 | --- | 0.5 |
| L | 1.5838 | 1.6161 | 40.231 | 41.051 |
| L1 | .9401 | .9598 | 23.88 | 24.38 |

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid.
3. The gold die attach pad (inside the package), seal ring, and metal lid are electrically connected to the package ground leads.
4. The leads are gold plated and can be solder dipped.

FIGURE 1. Case outline - Continued.

| Device type | 01 | | |
|---|---|---|---|
| Case outline | X | | |
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | $V_{CC}$ | 19 | $\overline{Q6}$ |
| 2 | CLK_SEL | 20 | Q6 |
| 3 | CLK0 | 21 | $\overline{Q5}$ |
| 4 | $\overline{CLK\ 0}$ | 22 | Q5 |
| 5 | $V_{BB}$ | 23 | $\overline{Q4}$ |
| 6 | CLK1 | 24 | Q4 |
| 7 | $\overline{CLK\ 1}$ | 25 | $\overline{Q3}$ |
| 8 | $V_{EE}$ | 26 | Q3 |
| 9 | $V_{CC}$ | 27 | $V_{CC}$ |
| 10 | $V_{CC}$ | 28 | $V_{CC}$ |
| 11 | $\overline{Q9}$ | 29 | $\overline{Q2}$ |
| 12 | Q9 | 30 | Q2 |
| 13 | $\overline{Q8}$ | 31 | $\overline{Q1}$ |
| 14 | Q8 | 32 | Q1 |
| 15 | $\overline{Q7}$ | 33 | $\overline{Q0}$ |
| 16 | Q7 | 34 | Q0 |
| 17 | $V_{CC}$ | 35 | $V_{CC}$ |
| 18 | $V_{CC}$ | 36 | $V_{CC}$ |

FIGURE 2. Terminal connections.

| Terminal symbol | Description |
|---|---|
| CLK_SEL | Clock select. Used to select between CLK0 and CLK1 input pairs. Low voltage transistor-transistor logic (LVTTL) / low voltage complementary metal oxide semiconductor (LVCMOS) functionality compatible. |
| CLK0, $\overline{CLK}$ 0 | Differential low voltage emitter coupled logic (LVECL) / LVPECL input pair |
| CLK1, $\overline{CLK}$ 1 | Differential LVECL/LVPECL input pair |
| Q(9:0) | LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn. |
| $\overline{Q}$ (9:0) | LVECL/LVPECL complementary clock inputs, these outputs provide copies of $\overline{CLKn}$ . |
| $V_{BB}$ | Reference voltage output for single ended input operation. |
| $V_{CC}$ | Supply voltage. |
| $V_{EE}$ | Device ground or negative supply voltage in emitter coupled logic (ECL) mode. |

FIGURE 2. Terminal connections - continued.

| CLK_SEL | Active clock input |
|---|---|
| 0 | CLK0, $\overline{CLK0}$ |
| 1 | CLK1, $\overline{CLK1}$ |

FIGURE 3. Truth table.

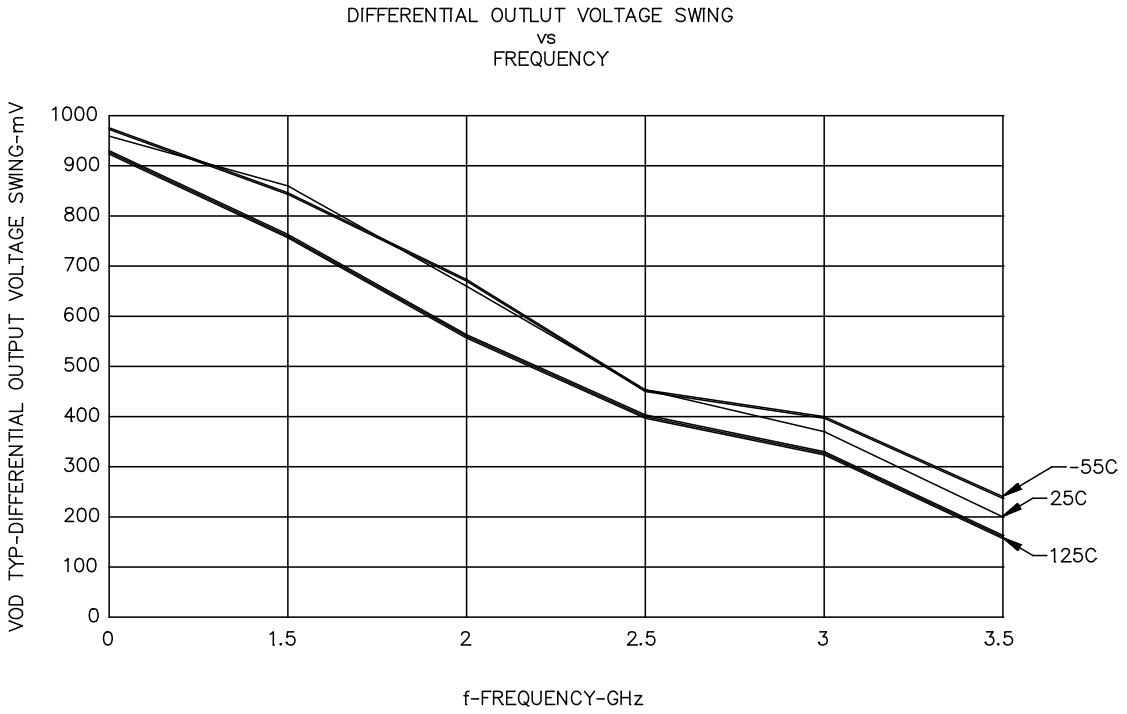
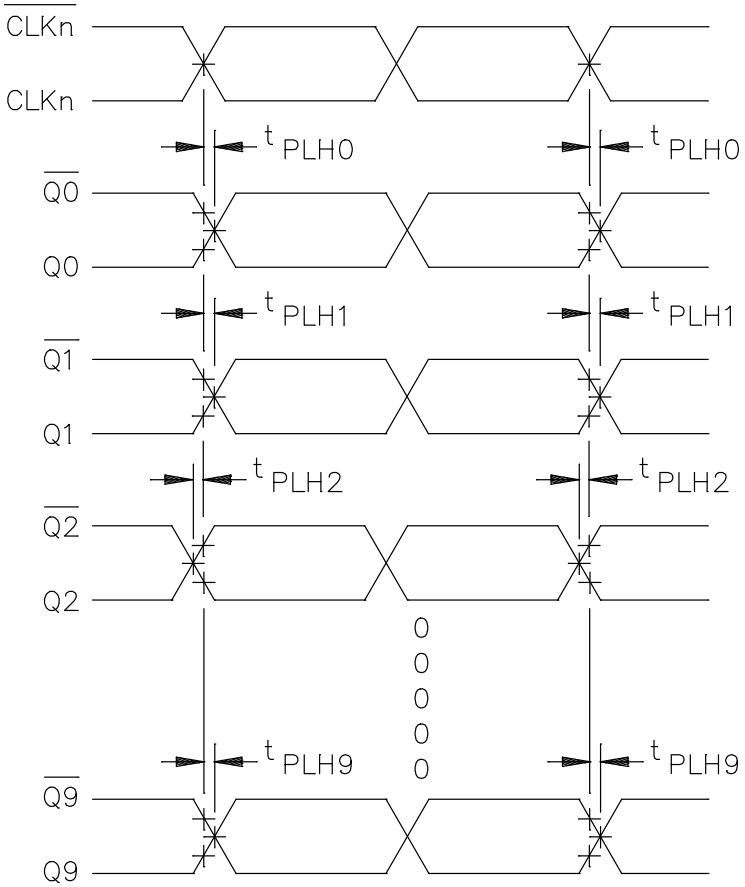



FIGURE 4. Differential output voltage swing graph.




NOTES:

1. Output skew $t_{sk(0)}$, is calculated as the greater of: the difference between the fastest and the slowest $t_{PLHn}$ (n = 0, 1, ..9) or the difference between the fastest and the slowest $t_{PHLn}$ (n = 0, 1,..9).
2. Part to part skew $t_{sk(pp)}$, is calculated as the greater of: the difference between the fastest and the slowest $t_{PLHn}$ (n = 0, 1,…9) across multiple devices or the difference between the fastest and the slowest $t_{PHLn}$ (n = 0, 1, …9) across multiple devices.
3. Nominal values measured at ambient when clock input is 155.52 MHz for an integration bandwidth of 20 kHz to 5 MHz.
4. Input conditions: $V_{CM}$ = 1 V, $V_{ID}$ = 0.5 V, and $f_{IN}$ = 1 GHz.

FIGURE 5. Waveform for calculating both output and part to part skew.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|
| | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | 1,2,3,9,10,11 | 1,2,3,9,10,11 |
| Final electrical parameters (see 4.2) | 1,2,3, 1/ 9,10,11 | 1,2,3, 2/ 9,10,11 |
| Group A test requirements (see 4.4) | 1,2,3,9,10,11 | 1,2,3,9,10,11 |
| Group C end-point electrical parameters (see 4.4) | 1,2,3,9,10,11 | 1,2,3, 2/ 9,10,11 |
| Group D end-point electrical parameters (see 4.4) | 1 | 1 |
| Group E end-point electrical parameters (see 4.4) | --- | --- |

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. $T_A$ = +25°C.

| Parameters | Symbol | Conditions | Delta limits | Units |
|---|---|---|---|---|
| Output and Internal supply current | $I_{CC}$ | All outputs terminated 50 Ω to $V_{CC}$ – 2 V | ±3.8 | mA |
| Supply internal current | $I_{EE}$ | Absolute value of current | ±0.77 | mA |
| Differential output voltage swing | $V_{OD}$ | Terminated with 50 Ω to $V_{CC}$ – 2 V | ±30 | mV |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = –21 mA | ±0.028 | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = –5 mA | ±0.028 | V |

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-01-15

Approved sources of supply for SMD 5962-16207 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-1620701VXC | 01295 | CDCLVP111HFG-V |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest lane<br>P.O. Box 660199<br>Dallas, TX 75243 |