

REVISIONS

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
|-----|-------------|-----------------|----------|
|     |             |                 |          |



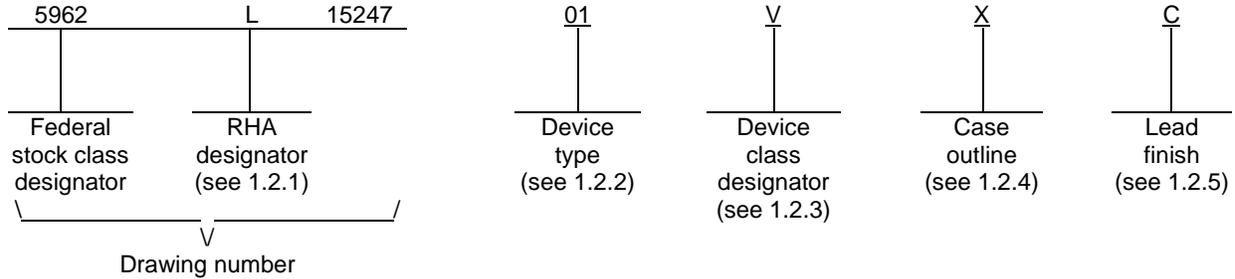
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|----------------------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|--|--|
| REV                  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |
| SHEET                |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |
| REV                  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |
| SHEET                | 15    | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |    |  |  |  |
| REV STATUS OF SHEETS | REV   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |
|                      | SHEET |    |    | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 |  |  |  |

|  |                                   |   |                           |                   |
|--|-----------------------------------|---|---------------------------|-------------------|
| PMIC N/A   | PREPARED BY<br>RODNEY D. CHAMBERS | <b>DLA LAND AND MARITIME</b><br><b>COLUMBUS, OHIO 43218-3990</b><br><a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a> |                           |                   |
| <b>STANDARD MICROCIRCUIT DRAWING</b><br><br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br><br>AMSC N/A | CHECKED BY<br>RAJESH PITHADIA     |   |                           |                   |
|  | APPROVED BY<br>CHARLES F. SAFFLE  | MICROCIRCUIT, DIGITAL-LINEAR, BiCMOS,<br>SINGLE 16-CHANNEL ANALOG MUX WITH<br>OVERVOLTAGE PROTECTION, MONOLITHIC SILICON                                |                           |                   |
|  | DRAWING APPROVAL DATE<br>16-03-14 |   |                           |                   |
|  | REVISION LEVEL                    | SIZE<br>A   | CAGE CODE<br><b>67268</b> | <b>5962-15247</b> |
|  |                                   | SHEET 1 OF 30   |                           |                   |

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. This device type identifies the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u> | <u>Circuit function</u>  |
|--------------------|-----------------------|--|
| 01                 | ISL71830SEH           | Radiation hardened, dielectrically isolated (DI), BICMOS, single 16-channel analog MUX with high impedance analog Input overvoltage protection |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| <u>Device class</u> | <u>Device requirements documentation</u>         |
|---------------------|--|
| Q, V                | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u>        |
|-----------------------|-------------------------------|------------------|-----------------------------|
| X                     | CDFP3-F28                     | 28               | Flat pack with grounded lid |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

|  |                 |
|--|-----------------|
| Supply voltage between V <sub>S</sub> and GND .....              | 7 V             |
| V <sub>REF</sub> to GND .....                                    | 7 V             |
| Digital input overvoltage range .....                            | VREF to GND     |
| Maximum current through a selected switch .....                  | 10mA            |
| Analog input overvoltage range (power on/off) .....              | -0.4 V to 7 V   |
| Storage temperature range .....                                  | -65°C to +150°C |
| Junction temperature (T <sub>J</sub> ) .....                     | +150°C          |
| Lead temperature (soldering, 10 seconds) .....                   | +275°C          |
| Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....    | 4°C/W           |
| Thermal resistance, junction-to-ambient (θ <sub>JA</sub> ) ..... | 48°C/W          |

1.4 Recommended operating conditions.

|   |                   |
|---|-------------------|
| Supply voltage (V <sub>S</sub> ) .....                      | 3.0 V to 5.5 V    |
| V <sub>REF</sub> .....                                      | 3.0 V to 5.5 V dc |
| Ambient operating temperature range (T <sub>A</sub> ) ..... | -55°C to +125°C   |

1.5 Radiation features.

|  |                                    |
|--|------------------------------------|
| Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s): .....                    | 50 krad(Si) 2/                     |
| Single event phenomena (SEP):  |                                    |
| No SEL occurs at effective linear energy threshold (LET): .....                        | ≤ 60 MeV·cm <sup>2</sup> /mg 3/ 4/ |
| No SEB occurs at effective linear energy threshold (LET): .....                        | ≤ 60 MeV·cm <sup>2</sup> /mg 4/    |
| Single event transients (SET) observed at an effective LET (see 4.4.4.3)               |                                    |
| (SET magnitude of ±20 mV at a cross section 2X10 <sup>-5</sup> cm <sup>2</sup> ) ..... | = 43 MeV cm <sup>2</sup> /mg 4/    |

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Device type 01 has been tested at low dose rate only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 75 krad(Si). Device type 01 is wafer acceptance tested to 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D, per customer request, and are marked at the standard 50 krad(Si) level.
- 3/ Device type 01 use silicon on insulator (SOI) technology. No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Pr ions at normal incidence, corresponding to a surface LET of 60 MeV·cm<sup>2</sup>/mg. The normal particle range into silicon for Pr ions after 30 mm of air is about 110 μm and the Bragg peak range is 37μm, resulting in ion penetration well beyond the sensitive volume of the devices.
- 4/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

|  |                  |                |                   |
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3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. Electrical performance characteristics.

| Test  | Symbol                   | Conditions 1/<br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br><br>V <sub>S</sub> = 5 V, V <sub>REF</sub> = 3.3V<br>unless otherwise specified             | Group A<br>subgroups | Device<br>type | Limits |     | Unit |
|---|--------------------------|---|----------------------|----------------|--------|-----|------|
|   |                          |   |                      |                | Min    | Max |      |
| Channel on<br>resistance  | R <sub>ON</sub>          | V <sub>S</sub> = 4.5 V, V <sub>IN</sub> = 0 V to V <sub>S</sub><br>I <sub>OUT</sub> = 1 mA  | 1,2,3                | 01             |        | 120 | Ω    |
|   |                          |   | M, D, P, L           |                | 1 3/   |     |      |
| R <sub>ON</sub> match between<br>channels   | ΔR <sub>ON</sub>         | V <sub>S</sub> = 4.5 V,<br>V <sub>IN</sub> = 0 V, 2.25V, 4.5V,<br>I <sub>OUT</sub> = 1 mA   | 1,2,3                | 01             |        | 5   | Ω    |
|   |                          |   | M, D, P, L           |                | 1 3/   |     |      |
| R <sub>ON</sub> flatness  | ΔR <sub>ON-FL</sub>      | V <sub>S</sub> = 4.5 V, V <sub>IN</sub> = 0 V to V <sub>S</sub><br>I <sub>OUT</sub> = 1 mA  | 1,2,3                | 01             |        | 40  | Ω    |
|   |                          |   | M, D, P, L           |                | 1 3/   |     |      |
| Switch Input Off<br>Leakage   | I <sub>IN(OFF)</sub>     | V <sub>S</sub> = 5.5 V, V <sub>IN</sub> = 5 V,<br>all unused inputs and output<br>equal = 0.5V, see figure 4 2/                                 | 1, 2, 3              | 01             | -30    | 30  | nA   |
|   |                          |   | M, D, P, L           |                | 1 3/   | -30 |      |
|   |                          | V <sub>S</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V,<br>all unused inputs and output<br>equal = 5V, see figure 4 2/                                 | 1, 2, 3              |                | -30    | 30  | nA   |
|   |                          |   | M, D, P, L           |                | 1 3/   | -30 |      |
| Switch Input Off<br>Over Voltage  | I <sub>IN(OFF-OV)</sub>  | V <sub>S</sub> = 5.5 V, V <sub>IN</sub> = +7 V,<br>V <sub>OUT</sub> = 0 V,<br>unused inputs = 0V,<br>see figure 4                               | 1, 3                 | 01             | -30    | 30  | nA   |
|   |                          |   | 2                    |                | -30    | 120 |      |
|   |                          |   | M, D, P, L           |                | 1 3/   | -30 |      |
| Switch off leakage<br>into the input of an<br>unselected<br>channel with<br>supplies grounded | I <sub>IN(PWR-OFF)</sub> | V <sub>IN</sub> = +7 V,<br>V <sub>REF</sub> = V <sub>EN</sub> = V <sub>A</sub> = ±V <sub>S</sub> = 0 V,<br>unused inputs = 0 V,<br>see figure 4 | 1,3                  | 01             | -20    | 20  | nA   |
|   |                          |   | 2                    |                | -20    | 50  |      |
|   |                          |   | M, D, P, L           |                | 1 3/   | -20 |      |
| Switch off leakage<br>into the input of an<br>unselected<br>channel with<br>supplies open     | I <sub>IN(PWR-OFF)</sub> | V <sub>IN</sub> = +7 V,<br>V <sub>REF</sub> = V <sub>EN</sub> = V <sub>A</sub> = ±V <sub>S</sub> = 0 V,<br>unused inputs = 0 V,<br>see figure 4 | 1,3                  | 01             | -20    | 20  | nA   |
|   |                          |   | 2                    |                | -20    | 50  |      |
|   |                          |   | M, D, P, L           |                | 1 3/   | -20 |      |

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

| Test   | Symbol                 | Conditions 1/<br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>V <sub>S</sub> = 5 V, V <sub>REF</sub> = 3.3V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |      | Unit |
|--|------------------------|---|----------------------|----------------|--------|------|------|
|  |                        |   |                      |                | Min    | Max  |      |
| Switch on leakage<br>into the input of a<br>selected channel<br>(over voltage) | I <sub>IN(ON-OV)</sub> | V <sub>S</sub> = 5.5V, V <sub>IN</sub> = +7V,<br>V <sub>OUT</sub> = OPEN,<br>unused inputs = 0 V,<br>see figure 4               | 1, 2, 3              | 01             | 2.75   | 5.5  | μA   |
|  |                        |   | M, D, P, L           |                | 1 3/   | 2.75 |      |
| Switch off leakage<br>into the output with<br>the part disabled                | I <sub>OUT(OFF)</sub>  | V <sub>S</sub> = 5.5V, V <sub>IN</sub> = 0.5 V,<br>V <sub>OUT</sub> = 5.0 V,<br>see figure 4 2/                                 | 1, 3                 | 01             | -30    | 30   | nA   |
|  |                        |   | 2                    |                | 0      | 150  |      |
|  |                        |   | M, D, P, L           |                | 1 3/   | -30  |      |
|  |                        | V <sub>S</sub> = 5.5V, V <sub>IN</sub> = 5.0 V,<br>V <sub>OUT</sub> = 0.5 V,<br>see figure 4 2/                                 | 1, 3                 |                | -30    | 30   |      |
|  |                        |   | 2                    |                | -60    | 0    |      |
|  |                        |   | M, D, P, L           |                | 1 3/   | -30  |      |
| Switch on leakage<br>into the<br>input/output for a<br>selected switch         | I <sub>OUT(ON)</sub>   | V <sub>S</sub> = 5.5V, V <sub>IN</sub> = V <sub>OUT</sub> = 5.0 V,<br>unused inputs = 0.5 V,<br>see figure 4 2/                 | 1, 3                 | 01             | -30    | 30   | nA   |
|  |                        |   | 2                    |                | 0      | 150  |      |
|  |                        |   | M, D, P, L           |                | 1 3/   | -30  |      |
|  |                        | V <sub>S</sub> = 5.5V, V <sub>IN</sub> = V <sub>OUT</sub> = 0.5 V,<br>unused inputs = 5.0 V,<br>see figure 4 2/                 | 1, 3                 |                | -30    | 30   |      |
|  |                        |   | 2                    |                | -60    | 0    |      |
|  |                        |   | M, D, P, L           |                | 1 3/   | -30  |      |

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

| Test  | Symbol                           | Conditions 1/<br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>V <sub>S</sub> = 5 V, V <sub>REF</sub> = 3.3V<br>unless otherwise specified                          | Group A<br>subgroups | Device<br>type | Limits |     | Unit |
|---|----------------------------------|--|----------------------|----------------|--------|-----|------|
|   |                                  |  |                      |                | Min    | Max |      |
| Logic input high/low<br>voltage<br>level                    | V <sub>IH</sub> /V <sub>IL</sub> | V <sub>S</sub> = 5.5V, V <sub>REF</sub> = 3.3V<br>M, D, P, L   | 1, 2, 3              | 01             | 1.3    | 1.6 | V    |
|   |                                  |  | 1 3/                 |                | 1.3    | 1.6 |      |
| Input Current Into V <sub>A</sub><br>and<br>V <sub>EN</sub> | I <sub>IH</sub> /I <sub>IL</sub> | V <sub>S</sub> = 5.5V,<br>V <sub>REF</sub> = V <sub>EN</sub> = V <sub>A</sub> = 3.3V<br>M, D, P, L   | 1, 2, 3              | 01             | -100   | 100 | nA   |
|   |                                  |  | 1 3/                 |                | -100   | 100 |      |
| Quiescent supply<br>current                                 | I <sub>SUPPLY</sub>              | V <sub>S</sub> = V <sub>REF</sub> = V <sub>EN</sub> = 5.5V,<br>V <sub>A</sub> = 0 V 2/<br>M, D, P, L   | 1,3                  | 01             |        | 100 | nA   |
|   |                                  |  | 2                    |                |        | 300 |      |
|   |                                  |  | 1 3/                 |                |        | 300 |      |
| Supply current in V <sub>REF</sub>                          | I <sub>REF</sub>                 | V <sub>S</sub> = V <sub>REF</sub> = V <sub>EN</sub> = 5.5V,<br>V <sub>A</sub> = 0 V 2/<br>M, D, P, L   | 1,2,3                | 01             |        | 200 | nA   |
|   |                                  |  | 1 3/                 |                |        | 200 |      |
| Capacitance:<br>channel input                               | C <sub>IN(OFF)</sub>             | +V <sub>S</sub> = -V <sub>S</sub> = 0 V,<br>f = 1 MHz, T <sub>A</sub> = +25°C,<br>see 4.4.1c   | 4                    | 01             |        | 5   | pF   |
| Capacitance:<br>channel output                              | C <sub>OUT(OFF)</sub>            | +V <sub>S</sub> = -V <sub>S</sub> = 0 V,<br>f = 1 MHz, T <sub>A</sub> = +25°C,<br>see 4.4.1c   | 4                    | 01             |        | 25  | pF   |
| Off isolation   | V <sub>ISO</sub>                 | V <sub>EN</sub> = V <sub>REF</sub> , f = 1 kHz,<br>R <sub>L</sub> = OPEN,<br>V <sub>S</sub> = 1 V <sub>RMS</sub> ,<br>T <sub>A</sub> = +25°C, see 4.4.1c | 4                    | 01             | 60     |     | dB   |
| Crosstalk rejection   | V <sub>CT</sub>                  | V <sub>EN</sub> = 0.8 V, f = 1 kHz,<br>R <sub>L</sub> = OPEN,<br>V <sub>S</sub> = 1 V <sub>RMS</sub> ,<br>T <sub>A</sub> = +25°C, see 4.4.1c             | 4                    | 01             | 73     |     | dB   |
| Charge injection  | V <sub>CTE</sub>                 | C <sub>L</sub> = 100 pF, V <sub>IN</sub> = 0 V,<br>see 4.4.1c  | 4                    | 01             |        | 5   | pC   |

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

| Test   | Symbol               | Conditions 1/<br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>V <sub>S</sub> = 5 V, V <sub>REF</sub> = 3.3V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits       |     | Unit |
|--|----------------------|---|----------------------|----------------|--------------|-----|------|
|  |                      |   |                      |                | Min          | Max |      |
| Functional test                                      |                      | See 4.4.1d  | 7,8A,8B              | 01             |              |     |      |
| Transition time from<br>address inputs to output     | t <sub>TRANS</sub>   | C <sub>L</sub> = 50 pF R <sub>L</sub> = 10 kΩ,<br>V <sub>S</sub> = 4.5 V  | 9, 10,11             | 01             | 10           | 70  | ns   |
|  |                      |   | M, D, P, L           |                | 9 <u>3</u> / | 10  |      |
| Break-before-make<br>time delay                      | t <sub>BBM</sub>     | C <sub>L</sub> = 50 pF R <sub>L</sub> = 100 Ω,<br>V <sub>S</sub> = 4.5 V<br>See figure 5  | 9, 10,11             | 01             | 5            | 40  | ns   |
|  |                      |   | M, D, P, L           |                | 9 <u>3</u> / | 5   |      |
| Propagation delay<br>time enable to I/O<br>channels  | t <sub>ON(EN)</sub>  | C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ,<br>V <sub>S</sub> = 4.5 V   | 9, 10,11             | 01             |              | 40  | ns   |
|  |                      |   | M, D, P, L           |                | 9 <u>3</u> / |     |      |
| Propagation delay<br>time disable to I/O<br>channels | t <sub>OFF(EN)</sub> | C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ,<br>V <sub>S</sub> = 4.5 V   | 9, 10,11             | 01             |              | 40  | ns   |
|  |                      |   | M, D, P, L           |                | 9 <u>3</u> / |     |      |

See footnotes at end of table.

|  |                  |                |                   |
|--|------------------|----------------|-------------------|
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TABLE IA. Electrical performance characteristics - Continued.

| Test                                      | Symbol                  | Conditions 4/<br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>V <sub>S</sub> = 3.3 V, VREF = 3.3V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits |     | Unit |
|---|-------------------------|---|----------------------|----------------|--------|-----|------|
|   |                         |   |                      |                | Min    | Max |      |
| Channel on<br>resistance                  | R <sub>ON</sub>         | V <sub>S</sub> = 3.0 V, V <sub>IN</sub> = 0 V to V <sub>S</sub><br>I <sub>OUT</sub> = 1 mA                            | 1,2,3                | 01             |        | 200 | Ω    |
|   |                         |   | M, D, P, L           |                | 1 3/   |     |      |
| R <sub>ON</sub> match between<br>channels | ΔR <sub>ON</sub>        | V <sub>S</sub> = 3.0 V,<br>V <sub>IN</sub> = 0.5 V, 2.5V<br>I <sub>OUT</sub> = 1 mA                                   | 1,2,3                | 01             |        | 5   | Ω    |
|   |                         |   | M, D, P, L           |                | 1 3/   |     |      |
| R <sub>ON</sub> flatness                  | ΔR <sub>ON-FL</sub>     | V <sub>S</sub> = 3.0 V, V <sub>IN</sub> = 0 V to V <sub>S</sub><br>I <sub>OUT</sub> = 1 mA                            | 1,2,3                | 01             |        | 50  | Ω    |
|   |                         |   | M, D, P, L           |                | 1 3/   |     |      |
| Switch Input Off<br>Leakage               | I <sub>IN(OFF)</sub>    | V <sub>S</sub> = 3.6 V, V <sub>IN</sub> = 3.1 V,<br>all unused inputs and output<br>equal = 0.5V, see figure 4 5/     | 1, 2, 3              | 01             | -30    | 30  | nA   |
|   |                         |   | M, D, P, L           |                | 1 3/   | -30 |      |
|   |                         | V <sub>S</sub> = 3.6 V, V <sub>IN</sub> = 0.5 V,<br>all unused inputs and output<br>equal = 3.1V, see figure 4 5/     | 1, 2, 3              |                | -30    | 30  | nA   |
|   |                         |   | M, D, P, L           |                | 1 3/   | -30 |      |
| Switch Input Off<br>Over Voltage          | I <sub>IN(OFF-OV)</sub> | V <sub>S</sub> = 3.6 V, V <sub>IN</sub> = +7 V,<br>V <sub>OUT</sub> = 0 V,<br>unused inputs = 0 V,<br>see figure 4    | 1, 3                 | 01             | -30    | 30  | nA   |
|   |                         |   | 2                    |                | -30    | 100 |      |
|   |                         |   | M, D, P, L           |                | 1 3/   | -30 |      |

See footnotes at end of table.

|  |                  |                |                   |
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TABLE IA. Electrical performance characteristics - Continued.

| Test   | Symbol                | Conditions <u>4/</u><br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>V <sub>S</sub> = 3.3 V, VREF = 3.3V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits      |     | Unit |
|--|-----------------------|--|----------------------|----------------|-------------|-----|------|
|  |                       |  |                      |                | Min         | Max |      |
| Switch on leakage<br>into the input of a<br>selected channel<br>(over voltage) | I <sub>IN(OV)</sub>   | V <sub>S</sub> = 3.6 V, V <sub>IN</sub> = +7 V,<br>V <sub>OUT</sub> = OPEN,<br>unused inputs = 0 V,<br>see figure 4          | 1, 2, 3              | 01             | 1.8         | 3.6 | μA   |
|  |                       |  | M, D, P, L           |                | 1 <u>3/</u> | 1.8 |      |
| Switch off leakage<br>into the output with<br>the part disabled                | I <sub>OUT(OFF)</sub> | V <sub>S</sub> = 3.6 V, V <sub>IN</sub> = 0.5 V,<br>V <sub>OUT</sub> = 3.1 V,<br>see figure 4 <u>5/</u>                      | 1, 3                 | 01             | -30         | 30  | nA   |
|  |                       |  | 2                    |                | 0           | 60  |      |
|  |                       |  | M, D, P, L           |                | 1 <u>3/</u> | -30 |      |
|  |                       | V <sub>S</sub> = 3.6 V, V <sub>IN</sub> = 3.1 V,<br>V <sub>OUT</sub> = 0.5 V,<br>see figure 4 <u>5/</u>                      | 1, 3                 |                | -30         | 30  |      |
|  |                       |  | 2                    |                | 0           | 30  |      |
|  |                       |  | M, D, P, L           |                | 1 <u>3/</u> | -30 |      |
| Switch on leakage<br>into the<br>input/output for a<br>selected switch         | I <sub>OUT(ON)</sub>  | V <sub>S</sub> = 3.6V, V <sub>IN</sub> = V <sub>OUT</sub> = 3.1 V,<br>unused inputs = 0.5 V,<br>see figure 4 <u>5/</u>       | 1, 3                 | 01             | -30         | 30  | nA   |
|  |                       |  | 2                    |                | 0           | 30  |      |
|  |                       |  | M, D, P, L           |                | 1 <u>3/</u> | -30 |      |
|  |                       | V <sub>S</sub> = 3.6V, V <sub>IN</sub> = V <sub>OUT</sub> = 0.5 V,<br>unused inputs = 3.1 V,<br>see figure 4 <u>5/</u>       | 1, 3                 |                | -30         | 30  |      |
|  |                       |  | 2                    |                | 0           | 30  |      |
|  |                       |  | M, D, P, L           |                | 1 <u>3/</u> | -30 |      |

See footnotes at end of table.

|  |                  |                |                   |
|--|------------------|----------------|-------------------|
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TABLE IA. Electrical performance characteristics - Continued.

| Test   | Symbol               | Conditions 4/<br>-55°C ≤ T <sub>A</sub> ≤ +125°C<br>V <sub>S</sub> = 3.3V, V <sub>REF</sub> = 3.3V<br>unless otherwise specified | Group A<br>subgroups | Device<br>type | Limits      |     | Unit |
|--|----------------------|--|----------------------|----------------|-------------|-----|------|
|  |                      |  |                      |                | Min         | Max |      |
| Quiescent supply<br>current                          | I <sub>SUPPLY</sub>  | V <sub>S</sub> = V <sub>REF</sub> = V <sub>EN</sub> = 3.6V, V <sub>A</sub><br>= 0 V <u>5/</u>                                    | 1,3                  | 01             |             | 100 | nA   |
|  |                      |  | 2                    |                |             | 300 |      |
|  |                      |  | M, D, P, L           |                | 1 <u>3/</u> | 300 |      |
| Supply current in V <sub>REF</sub>                   | I <sub>REF</sub>     | V <sub>S</sub> = V <sub>REF</sub> = V <sub>EN</sub> = 3.6V, V <sub>A</sub><br>= 0 V <u>5/</u>                                    | 1,2,3                | 01             |             | 200 | nA   |
|  |                      |  | M, D, P, L           |                | 1 <u>3/</u> | 200 |      |
| Functional test                                      |                      | See 4.4.1d   | 7,8A,8B              | 01             |             |     |      |
| Transition time from<br>address inputs to output     | t <sub>TRANS</sub>   | C <sub>L</sub> = 50 pF R <sub>L</sub> = 10 kΩ,<br>V <sub>S</sub> = 3.0V  | 9, 10,11             | 01             | 10          | 100 | ns   |
|  |                      |  | M, D, P, L           |                | 9 <u>3/</u> | 10  |      |
| Break-before-make<br>time delay                      | t <sub>BBM</sub>     | C <sub>L</sub> = 50 pF R <sub>L</sub> = 100 Ω,<br>V <sub>S</sub> = 3.0V<br>See figure 5  | 9, 10,11             | 01             | 5           | 50  | ns   |
|  |                      |  | M, D, P, L           |                | 9 <u>3/</u> | 5   |      |
| Propagation delay<br>time enable to I/O<br>channels  | t <sub>ON(EN)</sub>  | C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ,<br>V <sub>S</sub> = 3.0V   | 9, 10,11             | 01             |             | 50  | ns   |
|  |                      |  | M, D, P, L           |                | 9 <u>3/</u> | 50  |      |
| Propagation delay<br>time disable to I/O<br>channels | t <sub>OFF(EN)</sub> | C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ,<br>V <sub>S</sub> = 3.0V   | 9, 10,11             | 01             |             | 50  | ns   |
|  |                      |  | M, D, P, L           |                | 9 <u>3/</u> | 50  |      |

1/ Unless otherwise specified, V<sub>AH</sub> (logic level high) = 3.3 V dc, V<sub>AL</sub> (logic level low) = 0 V dc, V<sub>EN</sub> = 3.3 V, and V<sub>REF</sub> = 3.3 V dc. V<sub>S</sub> = 5.0 V dc.

2/ V<sub>S</sub> = 5.5V dc. V<sub>AH</sub> (logic level high) = 3.3 V dc, V<sub>AL</sub> (logic level low) = 0 V dc and V<sub>REF</sub> = 3.3 V dc.

3/ RHA device type 01 supplied to this drawing will meet all levels M, D, P and L of irradiation for condition D. However, device type 01 is only tested in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein) at a total ionizing dose of 75 krad(Si). Device type 01 is wafer acceptance tested 75 krad(Si) total ionizing dose per MIL-STD-883, method 1019, condition D, per customer request, and are marked at the standard 50 krad(Si) level.

Pre and Post irradiation values and parameters are as specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T<sub>A</sub> = +25°C.

4/ Unless otherwise specified, V<sub>AH</sub> (logic level high) = 3.3 V dc, V<sub>AL</sub> (logic level low) = 0 V dc, V<sub>EN</sub> = 3.3 V, and V<sub>REF</sub> = 3.3 V dc. V<sub>S</sub> = 3.3 V dc.

5/ V<sub>S</sub> = 3.6 V dc. V<sub>AH</sub> (logic level high) = 3.3 V dc, V<sub>AL</sub> (logic level low) = 0 V dc and V<sub>REF</sub> = 3.3 V dc.

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TABLE IB. SEP test limits. 1/ 2/

| Device type | SEP          | Temperature (T <sub>C</sub> ) | Linear energy transfer (LET)                              |
|-------------|--------------|-------------------------------|---|
| 01          | No SEL       | 125°C                         | Effective LET= 60 MeV·cm <sup>2</sup> /mg<br><u>3/ 4/</u> |
|             | No SEB       | 125°C                         | Effective LET=60 MeV·cm <sup>2</sup> /mg<br><u>4/</u>     |
|             | SET Observed | 25°C                          | LET= 43 MeV·cm <sup>2</sup> /mg <u>5/</u>                 |

1/ For SEP test conditions, see 4.4.4.5 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Device type 01 uses silicon on insulator (SOI) technology. No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with Pr ions at normal incidence, corresponding to a surface LET of 60 MeV·cm<sup>2</sup>/mg. The normal particle range into silicon for Pr ions after 30 mm of air is about 110 μm and the Bragg peak range is 37 μm, resulting in ion penetration well beyond the sensitive volume of the devices.

4/ SEL and SEB testing was performed at a supply voltage of V<sub>S</sub> = 6.3 V, V<sub>REF</sub> = 6.3 V

5/ SET testing was performed at supply voltages of V<sub>S</sub> = 3.0V and V<sub>S</sub> = 5.5 V. V<sub>REF</sub> = 3 V for both supplies tested. SET magnitude of ±20 mV at a cross section 2X10<sup>-5</sup> cm<sup>2</sup> was observed

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| Device type     | 01                                    |                 |                        |
|-----------------|---------------------------------------|-----------------|------------------------|
| Case outline    | X                                     |                 |                        |
| Terminal number | Terminal symbol                       | Terminal number | Terminal symbol        |
| 1               | Vs                                    | 15              | A2                     |
| 2               | NC                                    | 16              | A1                     |
| 3               | NC                                    | 17              | A0                     |
| 4               | IN 16                                 | 18              | $\overline{\text{EN}}$ |
| 5               | IN 15                                 | 19              | IN 1                   |
| 6               | IN 14                                 | 20              | IN 2                   |
| 7               | IN 13                                 | 21              | IN 3                   |
| 8               | IN 12                                 | 22              | IN 4                   |
| 9               | IN 11                                 | 23              | IN 5                   |
| 10              | IN 10                                 | 24              | IN 6                   |
| 11              | IN 9                                  | 25              | IN 7                   |
| 12              | GND                                   | 26              | IN 8                   |
| 13              | V <sub>REF</sub>                      | 27              | NC                     |
| 14              | A3                                    | 28              | OUT                    |
| Package lid     | Tied internally to terminal 12 (GND). |                 |                        |

NC = No connection

FIGURE 1. Terminal connections.

|  |                  |                |                   |
|--|------------------|----------------|-------------------|
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| Truth table    |                |                |                |                        |            |
|----------------|----------------|----------------|----------------|------------------------|------------|
| A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | $\overline{\text{EN}}$ | On channel |
| X              | X              | X              | X              | H                      | None       |
| L              | L              | L              | L              | L                      | 1          |
| L              | L              | L              | H              | L                      | 2          |
| L              | L              | H              | L              | L                      | 3          |
| L              | L              | H              | H              | L                      | 4          |
| L              | H              | L              | L              | L                      | 5          |
| L              | H              | L              | H              | L                      | 6          |
| L              | H              | H              | L              | L                      | 7          |
| L              | H              | H              | H              | L                      | 8          |
| H              | L              | L              | L              | L                      | 9          |
| H              | L              | L              | H              | L                      | 10         |
| H              | L              | H              | L              | L                      | 11         |
| H              | L              | H              | H              | L                      | 12         |
| H              | H              | L              | L              | L                      | 13         |
| H              | H              | L              | H              | L                      | 14         |
| H              | H              | H              | L              | L                      | 15         |
| H              | H              | H              | H              | L                      | 16         |

FIGURE 2. Truth table.

|  |                  |                |                   |
|--|------------------|----------------|-------------------|
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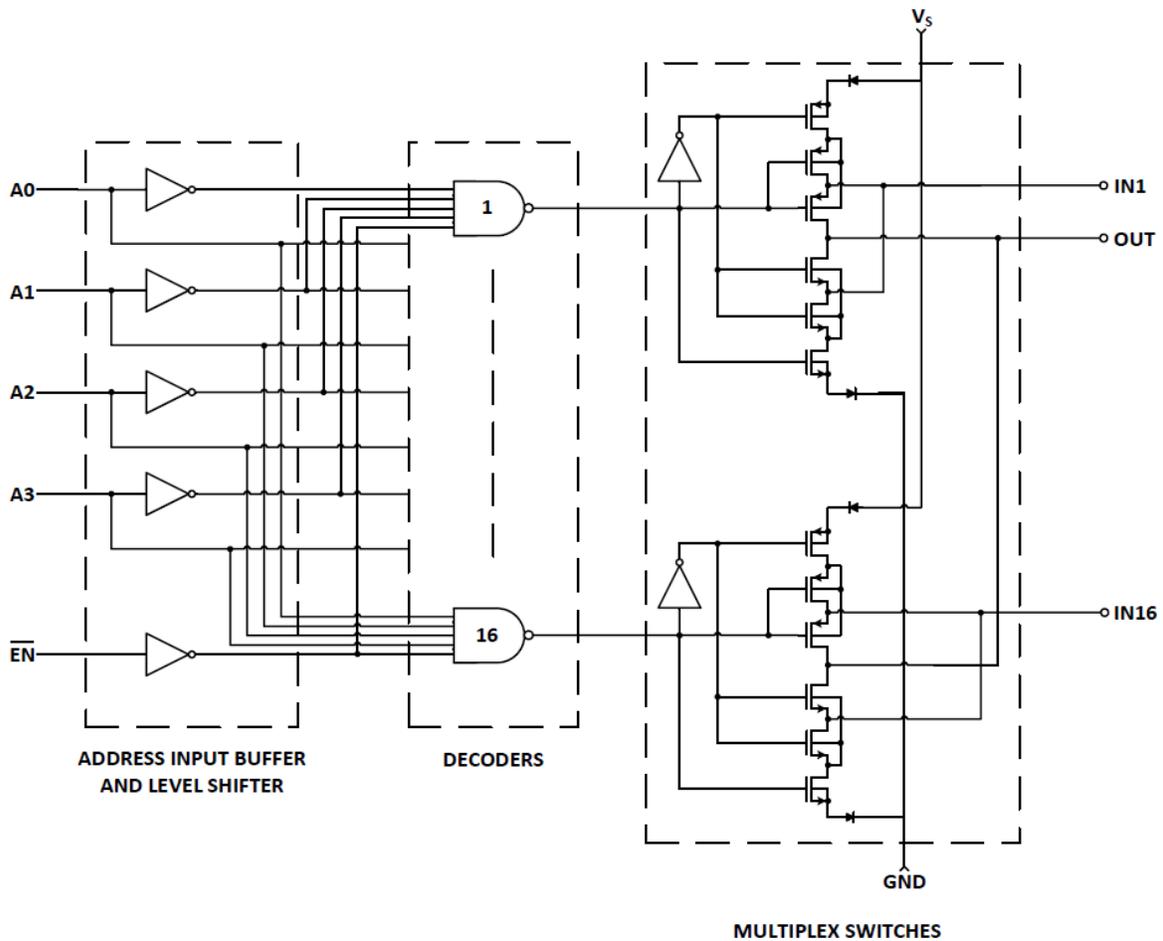


FIGURE 3. Logic diagram.

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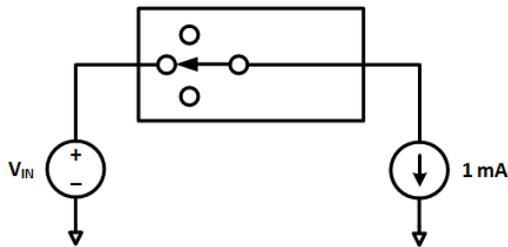
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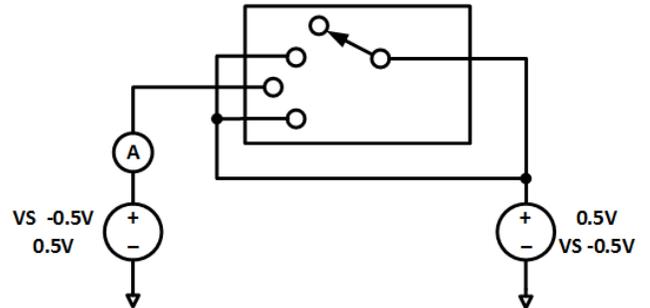
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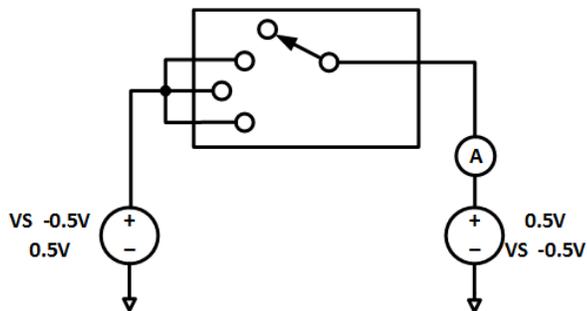
On Resistance vs. Input Signal Level



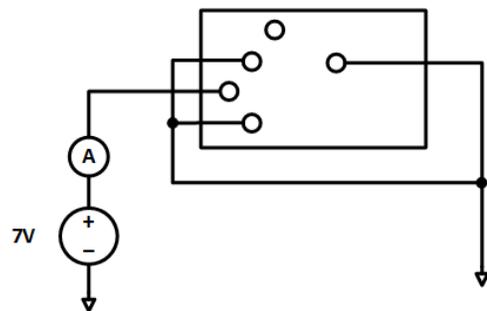
$I_{S(OFF)}$  Leakage Current



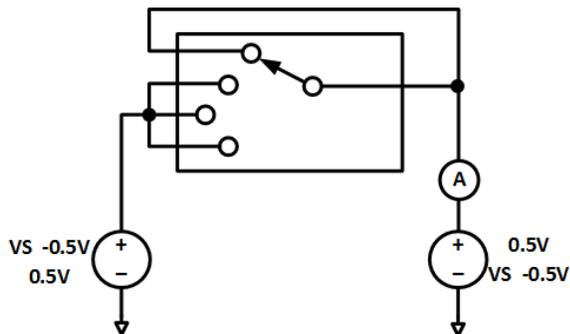
$I_{D(OFF)}$  Leakage Current



$I_{S(OFF)}$  Leakage Current Powered Off



$I_{D(ON)}$  Leakage Current



$I_{S(ON-OV)}$  Leakage Current

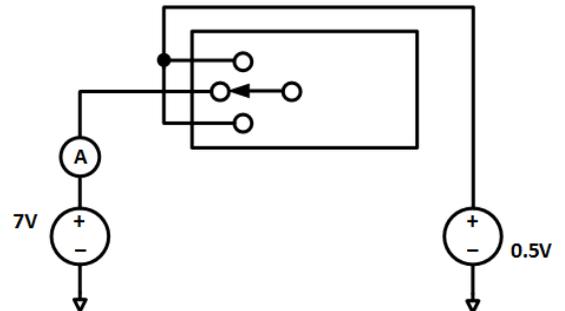


FIGURE 4. Test circuits for dc levels.

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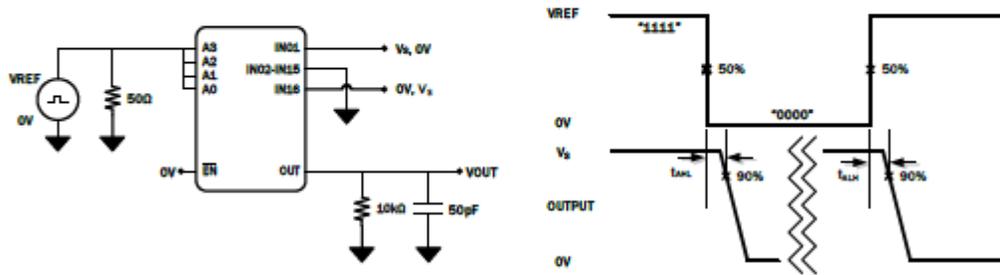
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### Address To Output Delay



### Break-Before-Make Delay

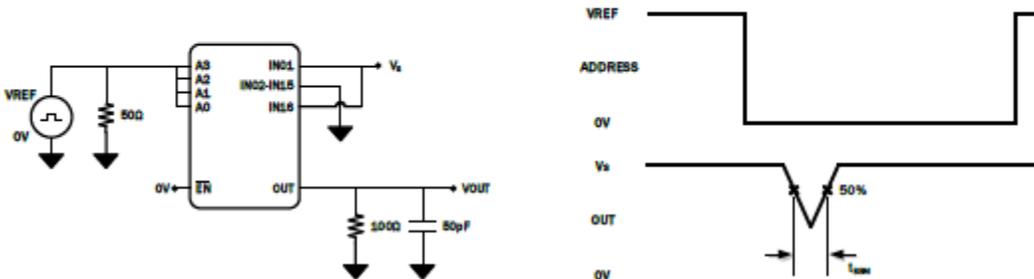


FIGURE 5. Test circuits and waveforms for ac levels.

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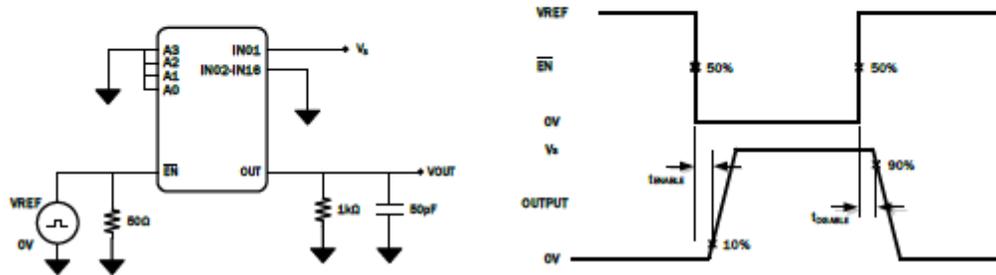
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### Enable To Output Delay



### Charge Injection

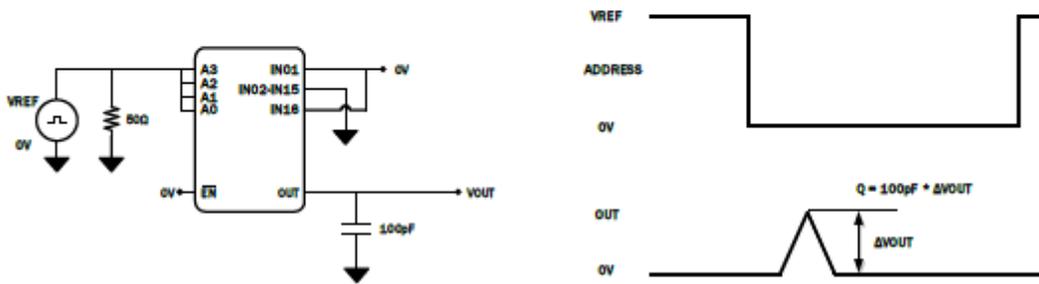


FIGURE 5. Test circuits and waveforms for ac levels – cont.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN(OFF)}$ ,  $C_{OUT(OFF)}$ ,  $V_{CT}$ ,  $V_{CTE}$ , and  $V_{ISO}$  measurements) should be measured for initial qualification and after any process or design changes which may affect input or output capacitance.
- d. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

|  |                  |                |                   |
|--|------------------|----------------|-------------------|
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TABLE IIA. Electrical test requirements.

| Test requirements                                    | Subgroups<br>(in accordance with<br>MIL-PRF-38535, table III) |  |
|--|---|--|
|  | Device<br>class Q   | Device<br>class V                          |
| Interim electrical<br>parameters (see 4.2)           | 1,7,9   | 1,7,9                                      |
| Final electrical<br>parameters (see 4.2)             | 1,2,3,7,8A, <u>1/</u><br>8B,9,10,11                           | 1,2,3, <u>1/ 2/</u><br>7,8A,8B,9,<br>10,11 |
| Group A test<br>requirements (see 4.4)               | 1,2,3,7,8A,<br>8B,9,10,11                                     | 1,2,3,7,8A,<br>8B,9,10,11                  |
| Group C end-point electrical<br>parameters (see 4.4) | 1,2,3,4,7,8A,<br>8B,9,10,11                                   | 1,2,3,4,7, <u>2/</u><br>8A,8B,9,10,11      |
| Group D end-point electrical<br>parameters (see 4.4) | 1,7,9   | 1,7,9                                      |
| Group E end-point electrical<br>parameters (see 4.4) | 1,7,9   | 1,7,9                                      |

- 1/ For device class Q, PDA applies to subgroup 1.  
For device class V, PDA applies to subgroups 1, 7, and Δ.
- 2/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

|  |                  |                |                   |
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TABLE IIB. Burn-in and operating life test delta parameters.  $T_A = +25^\circ\text{C}$ .

| Parameters  | Symbol                        | Conditions  | Delta limits      |
|---|-------------------------------|---|-------------------|
| Supply Current<br>+5.5v, +3.6v                                      | $I_{\text{SUPPLY}}$           | $V_{\text{ref}}$ and $V_{\text{en}} = V+$                               | $\pm 60$ nA       |
| Reference Current<br>+5.5v, +3.6v                                   | $I_{\text{REF}}$              | $V+$ and $V_{\text{en}} = V_{\text{ref}}$                               | $\pm 70$ nA       |
| Switch on resistance  | $R_{\text{ON}}$               | $V_S = +3.0$ V<br>$I_D = 1$ mA  | $\pm 20$ $\Omega$ |
| Switch on resistance  | $R_{\text{ON}}$               | $V_S = +4.5$ V<br>$I_D = 1$ mA  | $\pm 15$ $\Omega$ |
| Input leakage current,<br>Address and Enable pin(s)                 | $I_{\text{IH}}/I_{\text{IL}}$ | Measure inputs sequentially,<br>ground all unbiased pins                | $\pm 20$ nA       |
| Switch Off Leakage Into the<br>Source of an Unselected Channel      | $I_{\text{IN(OFF)}}$          | $V_S = +5.5$ V<br>$V_{\text{IN}} = +5$ V<br>Measure inputs sequentially | $\pm 5$ nA        |
| Switch Off Leakage Into the Drain<br>with the Part Disabled         | $I_{\text{OUT(OFF)}}$         | $V_S = +5.5$ V<br>$V_{\text{OUT}} = +5$ V                               | $\pm 5$ nA        |
| Switch On Leakage Into the<br>Source/Drain for a Selected<br>Switch | $I_{\text{OUT(ON)}}$          | $V_S = +5.5$ V<br>$V_{\text{IN}}=V_{\text{OUT}}= +5$ V                  | $\pm 5$ nA        |
| Switch Off Leakage Into the<br>Source of an Unselected Channel      | $I_{\text{IN(OFF)}}$          | $V_S = 5.5$ V<br>$V_{\text{IN}} = +.5$ V<br>Measure inputs sequentially | $\pm 5$ nA        |
| Switch Off Leakage Into the Drain<br>with the Part Disabled         | $I_{\text{OUT(OFF)}}$         | $V_S = +5.5$ V<br>$V_{\text{OUT}} = +.5$ V                              | $\pm 5$ nA        |
| Switch On Leakage Into the<br>Source/Drain for a Selected Switch    | $I_{\text{OUT(ON)}}$          | $V_S = +5.5$ V<br>$V_{\text{IN}}=V_{\text{OUT}}= +.5$ V                 | $\pm 5$ nA        |

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D, as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at  $+25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ . Testing shall be performed at initial qualification and after any process or design changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and  $60^{\circ}$  to the normal, inclusive (i.e.  $0^{\circ} \leq \text{angle} \leq 60^{\circ}$ ). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be  $\geq 100$  errors or  $\geq 10^7$  ions/cm<sup>2</sup>.
- c. The flux shall be between  $10^2$  and  $10^5$  ions/cm<sup>2</sup>/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be  $\geq 20$  micron in silicon.
- e. The test temperature shall be  $+25^{\circ}\text{C}$  and the maximum rated operating temperature  $\pm 10^{\circ}\text{C}$ .
- f. Bias conditions shall be defined by the manufacturer for the latchup measurements.
- g. For SEL test limits, see Table IB herein.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

- a. RHA test conditions (SEP).
- b. Occurrence of latchup (SEL).
- c. Occurrence of single event burn-out (SEB).
- d. Observance of single event transient (SET).

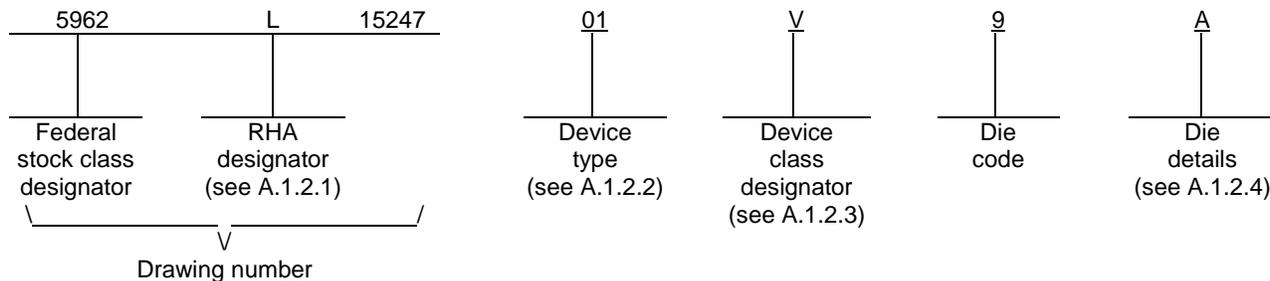
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u> | <u>Circuit function</u>   |
|--------------------|-----------------------|---|
| 01                 | ISL71830SEH           | Radiation hardened dielectrically isolated (DI) BICMOS single 16-channel analog MUX with high impedance analog input overvoltage protection |

A.1.2.3 Device class designator.

| <u>Device class</u> | <u>Device requirements documentation</u>                                 |
|---------------------|--|
| Q or V              | Certification and qualification to the die requirements of MIL-PRF-38535 |

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

| <u>Die type</u> | <u>Figure number</u> |
|-----------------|----------------------|
| 01              | A-1                  |

A.1.2.4.2 Die bonding pad locations and electrical functions.

| <u>Die type</u> | <u>Figure number</u> |
|-----------------|----------------------|
| 01              | A-1                  |

A.1.2.4.3 Interface materials.

| <u>Die type</u> | <u>Figure number</u> |
|-----------------|----------------------|
| 01              | A-1                  |

A.1.2.4.4 Assembly related information.

| <u>Die type</u> | <u>Figure number</u> |
|-----------------|----------------------|
| 01              | A-1                  |

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.5 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

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A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

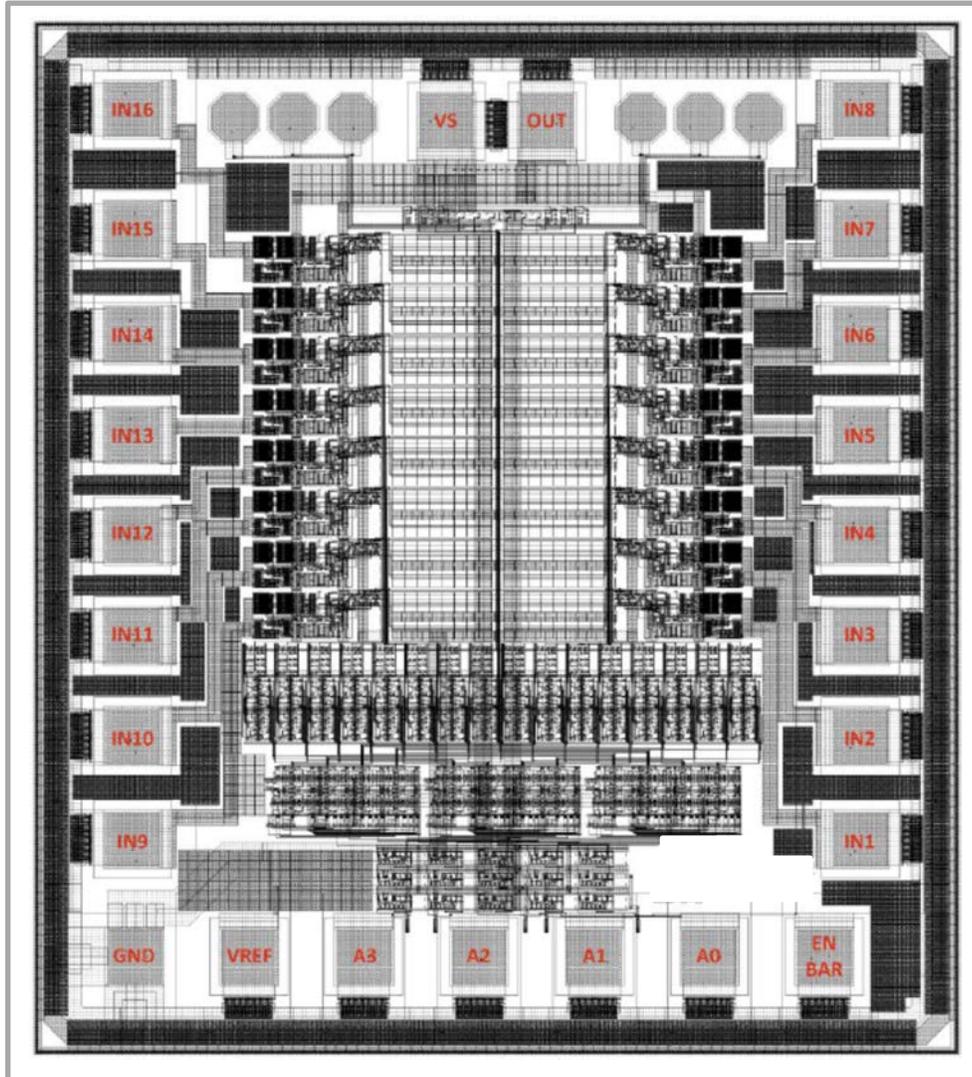
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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NOTE: Pad numbers reflect terminal numbers when placed in case outline X.

FIGURE A-1. Die bonding pad locations and electrical functions.

|   |                  |                |                   |
|---|------------------|----------------|-------------------|
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Die physical dimensions.

Die size: 2026  $\mu\text{m}$  x 2240  $\mu\text{m}$  (80 mils x 88 mils).  
Die thickness: 483 microns  $\pm$  25.4 microns.

Interface materials.

Top metallization: 300 $\text{\AA}$  TiN on 2.8 $\mu\text{m}$  AlCu, TiN removed from bond pads  
Backside metallization: Silicon

Glassivation.

Type: Silicon Nitride on Oxide  
Thickness: 12k $\text{\AA}$  Silicon Nitride on 3k $\text{\AA}$  Oxide

Substrate.

Bonded wafer dielectrically isolated.

Assembly related information.

Substrate potential: Floating  
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

|  |                  |                   |
|--|------------------|-------------------|
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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-03-14

Approved sources of supply for SMD 5962-15247 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

| Standard microcircuit drawing PIN <u>1/</u> | Vendor CAGE number | Vendor similar PIN <u>2/</u> |
|---|--------------------|------------------------------|
| 5962L1524701VXC                             | 34371              | ISL71830SEHVF                |
| 5962L1524701V9A                             | 34371              | ISL71830SEHVX                |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

34371

Vendor name and address

Intersil Corporation  
1650 Robert J. Conlan Blvd. NE  
Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.