REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update quiescent supply current (I_{DDQ}) limit to table IA. - MAA	17-10-30	Thomas M. Hess
B	Update to current boilerplate paragraphs - jwc	23-12-14	Muhammad Akbar

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					
REV STATUS			REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY Larry T. Gauder

CHECKED BY Muhammad Akbar

APPROVED BY Thomas M. Hess

DRAWING APPROVAL DATE 16-03-30

REVISION LEVEL B

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/Land-and-Maritime

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, DUAL, SEQUENTIAL, MANYGATE CONFIGURABLE LOGIC GATE WITH SCHMITT TRIGGER INPUTS AND TRI-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-15239**

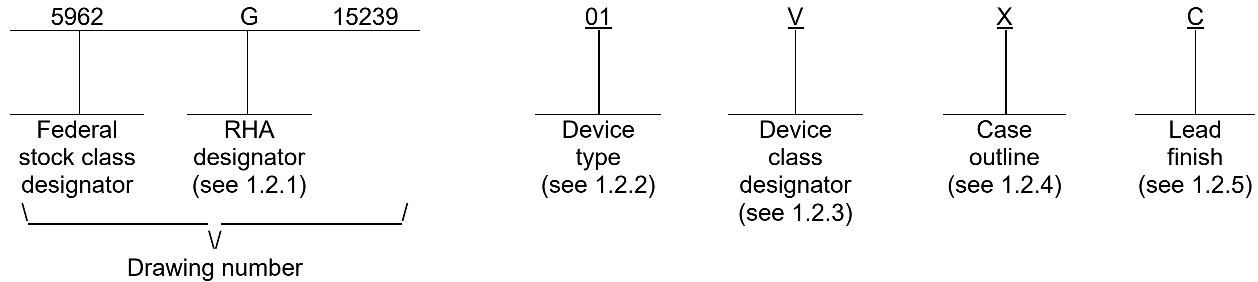
SHEET 1 OF 29

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT54ACS2S99S	Dual, sequential, ManyGate configurable logic gate with Schmitt trigger inputs and tri-state outputs
02	UT54ACS2S99S	Dual, sequential, ManyGate configurable logic gate with Schmitt trigger inputs and tri-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	20	Flat Package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD}) .... -0.3 V dc to +7.0 V dc
DC input voltage range (V_{IN}) .... -0.3 V dc to V_{DD} + 0.3 V dc
DC output voltage range (V_{OUT}) .... -0.3 V dc to V_{DD} + 0.3 V dc
DC input current, any one input (I_{IN}) .... ±10 Ma
Latch-up immunity current (I_{LU}) .... ±150mA
Storage temperature range (T_{STG}) .... -65°C to +150°C
Lead temperature (soldering, 5 seconds) .... +300°C
Thermal resistance, junction-to-case (θ_{JC}) .... 15°C/W
Junction temperature (T_J) .... +175°C
Maximum package power dissipation (P_D) .... 1.0 W 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD}) .... +3.0 V dc to +5.5 V dc
Input voltage range (V_{IN}) .... +0.0 V dc to V_{DD}
Output voltage range (V_{OUT}) .... +0.0 V dc to V_{DD}
Case operating temperature range (T_C) .... -55°C to +125°C
Maximum input rise or fall time at V_{DD} = 4.5 V (t_r, t_f) .... 1 s 5/

1.5 Radiation features. 6/

Maximum total dose available:
Device type 01 (dose rate = 50 – 300 Rad (Si)/s) .... 500K Rad (Si) 7/
Device type 02 (effective dose rate = 1 Rad (Si)/s) .... 1 Mrad (Si) 7/, 8/
Single event phenomenon (SEP):
No SEL occurs at effective LET, (see 4.4.4.3) .... ≤ 100 MeV/(mg/cm^2) 9/
No SEU occurs at effective LET, (see 4.4.4.3) .... ≤ 100 MeV/(mg/cm^2) 9

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise specified.
4/ Per MIL-STD-883 method 1012.1 section 3.4.1, P_D (Package) = (T_J(max) - T_C (max))/θ_{JC}
5/ Derate system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.
6/ Radiation testing is performed on the standard evaluation circuit.
7/ Device types 01, 02 are irradiated at dose rate = 50 – 300 Rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and are guaranteed to the maximum total dose specified.
8/ The device type 02 effective dose rate after extended room temperature anneal = 1 Rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device applies only at dose rates less than or equal to the effective dose rate.
9/ Limits are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM American Society for Testing and Materials (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org).

JEDEC INTERNATIONAL (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table(s) shall be as specified on figure 3.

3.2.4 Block or logic diagram. The block or logic diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Test circuit. The test circuit shall be as specified on figure 6.

3.2.6 Timing Waveforms. The timing waveforms shall be as specified on figures 7, 8 and 9.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	V_{DD}	Group A subgroups	Limits		Unit
							Min	Max	
Positive going input voltage threshold 2/	V_{T+}			All	3.3 V and 5.0 V	1, 2, 3		0.7 V_{DD}	V
Negative going input voltage threshold 2/	V_{T-}			All	3.3 V and 5.0 V	1, 2, 3	0.3 V_{DD}		V
Hysteresis voltage	V_H			All	3.3 V and 5.0 V	1, 2, 3	0.3		V
High level output voltage 3/	V_{OH}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} $I_{OH} = -100.0\ \mu A$		All	3.3 V and 5.0 V	1, 2, 3	V_{DD}-0.25		V
Low level output voltage 3/	V_{OL}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} $I_{OL} = +100.0\ \mu A$		All	3.3 V and 5.0 V	1, 2, 3		0.25	V
Input leakage current	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}		All	3.3 V	1, 2, 3	-1	+1	µA
		$V_{IN} = V_{DD}$ or GND		All	5.0 V	1	-1	+1	
High level output current (Source) 4/	I_{OH}	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD}$ -0.4 V		All	3.3 V	1, 2, 3	-8		mA
					5.0 V	1, 2, 3	-12		
Low level output current (Sink) 4/	I_{OL}	$V_{IN} = V_{DD}$ or V_{SS} V_{OL} = 0.4 V		All	3.3 V	1, 2, 3	+8		mA
					5.0 V	1, 2, 3	+12		
Output three-state current	I_{OZ}	$V_{OUT} = V_{DD}$ or V_{SS}		All	3.3 V and 5.0 V	1, 2, 3	-5	+5	µA
Quiescent supply current	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS}	Pre-Rad	01,02	3.6 V and 5.5 V	1, 2, 3		10	µA
			Max rated RHA	01	5.5 V	1		50	µA
			Max rated RHA	02	5.5 V	1		130	µA
Short circuit output current 5/ 6/	I_{OS}	$V_{OUT} = V_{DD}$ or V_{SS}		All	3.3 V	1, 2, 3	-200	+200	mA
					5.0 V	1, 2, 3	-300	+300	mA
Input capacitance 7/	C_{IN}	f = 1 MHz, see 4.4.1c		All	0.0 V	4		15	pF
Output capacitance 7/	C_{OUT}	f = 1 MHz, see 4.4.1c		All	0.0 V	4		15	pF
Power dissipation 4/ 8/	P_{total}	C_L = 50 pF, per switching output		All	3.3 V and 5.0 V	4, 5, 6		3.5	mW/ MHz
Functional test 9/	8/	$V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$ See 4.4.1b, T_C = 25°C		All	3.3 V and 5.0 V	7, 8	L	H	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
1F99S D-Flip-Flop								
Propagation delay time, CLK1 ↑ to 1Q	t_{PHL1} 9/	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11		21.5	ns
			All	4.5 V and 5.5V	9, 10, 11		16	
	t_{PLH1} 9/	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6 V	9, 10, 11		19.5	
			All	4.5 V and 5.5V	9, 10, 11		14	
Propagation delay time, $\overline{PRE}$ ↓ to 1Q	t_{PHL2} 9/	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11		20	ns
			All	4.5 V and 5.5V	9, 10, 11		14	
Propagation delay time, $\overline{CLR1}$ ↓ to 1Q	t_{PHL3} 9/	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11		23	
			All	4.5 V and 5.5V	9, 10, 11		17	
Propagation delay time, enable, $\overline{OEn}$ low to nQ	t_{PZL} 9/	C_L = 78 pF, see figure 4,6,9	All	3.0 V and 3.6V	9, 10, 11		12.5	ns
			All	4.5 V and 5.5V	9, 10, 11		9.0	
	t_{PZH} 9/	C_L = 78 pF, see figure 4,6,9	All	3.0 V and 3.6V	9, 10, 11		14	
			All	4.5 V and 5.5V	9, 10, 11		10	
Propagation delay time, disable, $\overline{OEn}$ high to nQ three-state	t_{PLZ} 9/	C_L = 78 pF, see figure 4,6,9	All	3.0 V and 3.6V	9, 10, 11		12	ns
			All	4.5 V and 5.5V	9, 10, 11		10	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
1F99S D-Flip-Flop – Continued.								
Propagation delay time, disable, $\overline{OEn}$ high to nQ three-state	t_{PHZ} 9/	C_L = 78 pF, see figure 4,6,9	All	3.0 V and 3.6V	9, 10, 11		16.5	ns
			All	4.5 V and 5.5V	9, 10, 11		13	
Maximum clock frequency	f_{MAX}	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11		46	MHz
			All	4.5 V and 5.5V	9, 10, 11		62	
Setup time, A1 – D1 before CLK1 ↑	t_{SU1}	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11	7		ns
			All	4.5 V and 5.5V	9, 10, 11	5		
Setup time, $\overline{PRE1}$ or $\overline{CLR1}$ before CLK1 ↑	t_{SU2}	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11	2		ns
			All	4.5 V and 5.5V	9, 10, 11	2		
Data hold time after CLK1 ↑	t_H	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11	0		ns
			All	4.5 V and 5.5V	9, 10, 11	0		
Minimum pulse width CLK1 high or low	t_{W1}	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11	6.0		ns
			All	4.5 V and 5.5V	9, 10, 11	4.5		
Minimum pulse width $\overline{PRE1}$ or $\overline{CLR1}$ low	t_{W2}	C_L = 78 pF, see figure 4,6,7	All	3.0 V and 3.6V	9, 10, 11	5.0		ns
			All	4.5 V and 5.5V	9, 10, 11	4.5		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
1L99S Transparent Latch								
Propagation delay time, CLK2 = H, A2 – D2 to 2Q	t_{PLH1} 9/	C_L = 78 pF, see figure 5,6,8	All	3.0 V and 3.6V	9, 10, 11		21.5	ns
			All	4.5 V and 5.5V	9, 10, 11		16	
	t_{PHL1} 9/	C_L = 78 pF, see figure 5,6,8	All	3.0 V and 3.6V	9, 10, 11		24.5	
			All	4.5 V and 5.5V	9, 10, 11		17.5	
Propagation delay time, CLK2 ↑ to 2Q	t_{PLH2} 9/	C_L = 78 pF, see figure 5,6,8	All	3.0 V and 3.6V	9, 10, 11		19	ns
			All	4.5 V and 5.5V	9, 10, 11		14	
	t_{PHL2} 9/		All	3.0 V and 3.6V	9, 10, 11		21.5	
			All	4.5 V and 5.5V	9, 10, 11		16	
Propagation delay time, enable, $\overline{OEn}$ low to nQ	t_{PZL} 9/	C_L = 78 pF, see figure 5,6,9	All	3.0 V and 3.6V	9, 10, 11		12.5	ns
			All	4.5 V and 5.5V	9, 10, 11		9.0	
	t_{PZH} 9/		All	3.0 V and 3.6V	9, 10, 11		14	
			All	4.5 V and 5.5V	9, 10, 11		10	
Propagation delay time, disable, $\overline{OEn}$ high to nQ three-state	t_{PLZ} 9/	C_L = 78 pF, see figure 5,6,9	All	3.0 V and 3.6V	9, 10, 11		12	ns
			All	4.5 V and 5.5V	9, 10, 11		10	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits		Unit
						Min	Max	
1L99S Transparent Latch – Continued								
Propagation delay time, disable, $\overline{OEn}$ high to nQ three-state	t_{PHZ} 9/	C_L = 78 pF, see figure 5,6,9	All	3.0 V and 3.6V	9, 10, 11		16.5	ns
			All	4.5 V and 5.5V	9, 10, 11		13	
Maximum clock frequency	f_{MAX}	C_L = 78 pF, see figure 5,6,8	All	3.0 V and 3.6V	9, 10, 11		46	MHz
			All	4.5 V and 5.5V	9, 10, 11		62	
Data setup time before CLK2 ↓	t_{SU}	C_L = 78 pF, see figure 5,6,8	All	3.0 V and 3.6V	9, 10, 11	8.0		ns
			All	4.5 V and 5.5V	9, 10, 11	5.5		
Data hold time after CLK2 ↓	t_H	C_L = 78 pF, see figure 5,6,8	All	3.0 V and 3.6V	9, 10, 11	0.0		ns
			All	4.5 V and 5.5V	9, 10, 11	0.0		
Minimum pulse width CLK2 ↑	t_W	C_L = 78 pF, see figure 5,6,8	All	3.0 V and 3.6V	9, 10, 11	6		ns
			All	4.5 V and 5.5V	9, 10, 11	5		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

1/ Device types 01, 02 are irradiated at dose rate = 50 - 300 Rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A. RHA device type 01 supplied to this drawing has been characterized through all levels M, D, P, L, R, F, and G of irradiation, but is only tested at the "G" level. RHA device type 02 supplied to this drawing has been characterized through all levels M, D, P, L, R, F, G and H of irradiation, but is only tested at the "H" level . The device type 02 effective dose rate after extended room temperature anneal = 1 Rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device applies only at dose rates less than or equal to the effective dose rate.

Each device type supplied to this drawing is guaranteed to comply with specification table IA through all RHA levels up to, and including, the maximum RHA level listed in section 1.5 Radiation features. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A=+25°C.

2/ Functional tests are conducted in accordance with the MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH} (min) +20%, -0%; V_{IL} = V_{IL} (max) +0%, -50%; as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH} (min) and V_{IL} (max).

3/ Per MIL-PRF-38535, for current density <=5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.

4/ Guaranteed by characterization.

5/ Supplied as a design limit, but not guaranteed or tested.

6/ Not more than one output may be shorted at a time for a maximum duration of one second.

7/ Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and VSS at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8/ Power dissipation specified per switching output.

9/ For propagation delay tests, all paths must be tested

TABLE IB. SEP test limits . 1/ 2/

Device type	Bias V_{DD} = 3.0 V and 4.5 V For single event upset (SEU) test 3/	Bias V_{DD} = 5.5 V For single event latchup (SEL) test. 5/
	Effective LET no upsets 4/	Effective LET no SEL
All	LET ≤100 MeV-mg/cm^2	LET ≤100 MeV-mg/cm^2

1/ For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test temperature T_A = +25°C ±10°C.
4/ Tested to a LET of ≤100 MeV-mg/cm^2 with no upsets.
5/ Worst case temperature for latchup test T_A = +125°C ±10°C.

Case outline X

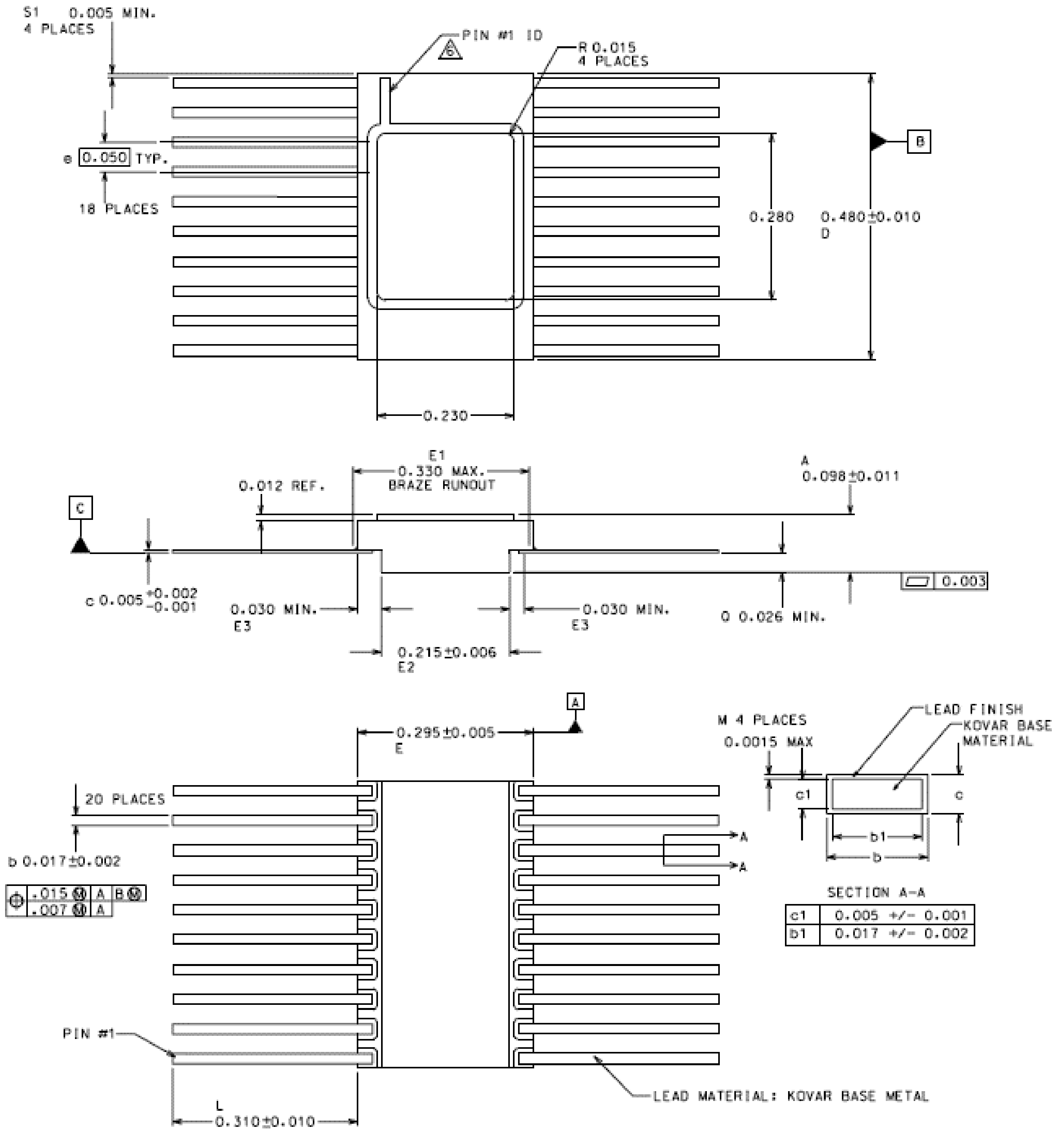


FIGURE 1. Case outline.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.087	0.109	2.210	2.769
b	0.015	0.019	0.381	0.483
c	0.004	0.007	0.102	0.178
D	0.470	0.490	11.938	12.446
E	0.290	0.300	7.366	7.620
E1	---	0.330	---	8.382
E2	0.209	0.221	5.309	5.613
E3	0.030	---	0.762	---
e	0.05 BSC		1.27 BSC	
L	0.300	0.320	7.620	8.128
Q	0.026	---	0.660	---
S1	0.005	---	0.127	---
M	---	0.0015	---	0.038

FIGURE 1. Case outline. – Continued.

Device type	All
Case outline	X
Terminal number	Terminal symbol
1	$\overline{CLR1}$
2	$\overline{PRE1}$
3	$\overline{OE1}$
4	CLK1
5	A1
6	B1
7	C1
8	D1
9	1Q
10	V_{SS}
11	NC
12	NC
13	$\overline{OE2}$
14	CLK2
15	A2
16	B2
17	C2
18	D2
19	2Q
20	V_{DD}

NC = No internal connection

Terminal description	
$\overline{OEn}$	Active Low output enable
An	A input
Bn	B input
Cn	C input
Dn	D input
nQ	3-State Output
$\overline{CLRn}$	Clear active Low
$\overline{PREn}$	Preset active Low
CLKn	Clock
V_{DD}	Power supply pin
V_{SS}	Ground pin
NC	No internal connection

FIGURE 2. Terminal connections.

Dn	Cn	Bn	An	Outputs to D_{IN}
L	L	L	L	L
L	L	L	H	H
L	L	H	L	L
L	L	H	H	H
L	H	L	L	L
L	H	L	H	L
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	L
H	L	H	L	H
H	L	H	H	L
H	H	L	L	H
H	H	L	H	H
H	H	H	L	L
H	H	H	H	L

FIGURE 3. Combinatorial Truth Table An, Bn, Cn, Dn to input (D_{IN}) of Storage Element.

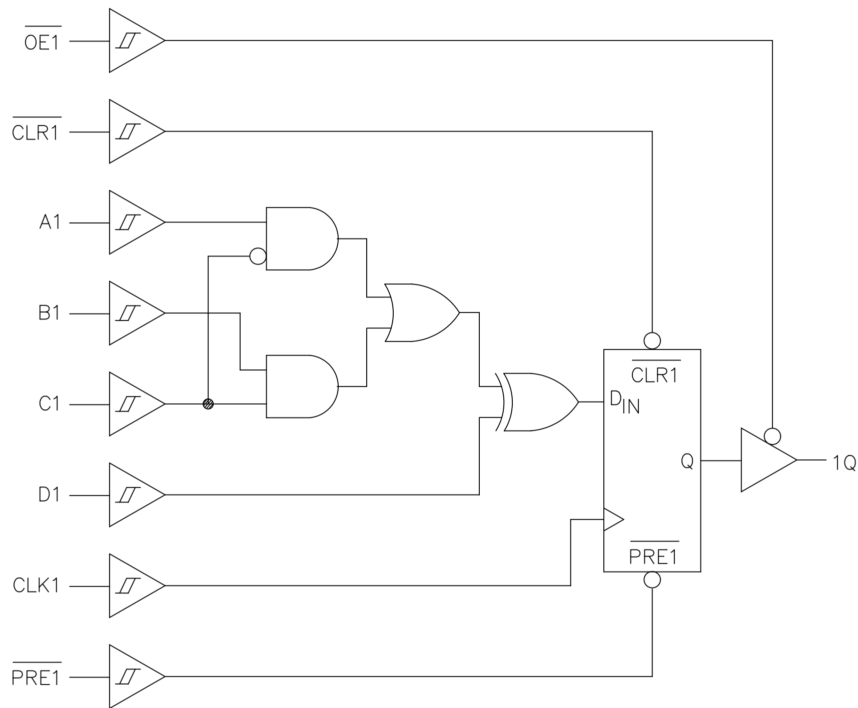


FIGURE 4. Block or Logic Diagram - 1F99 D Flip Flop.

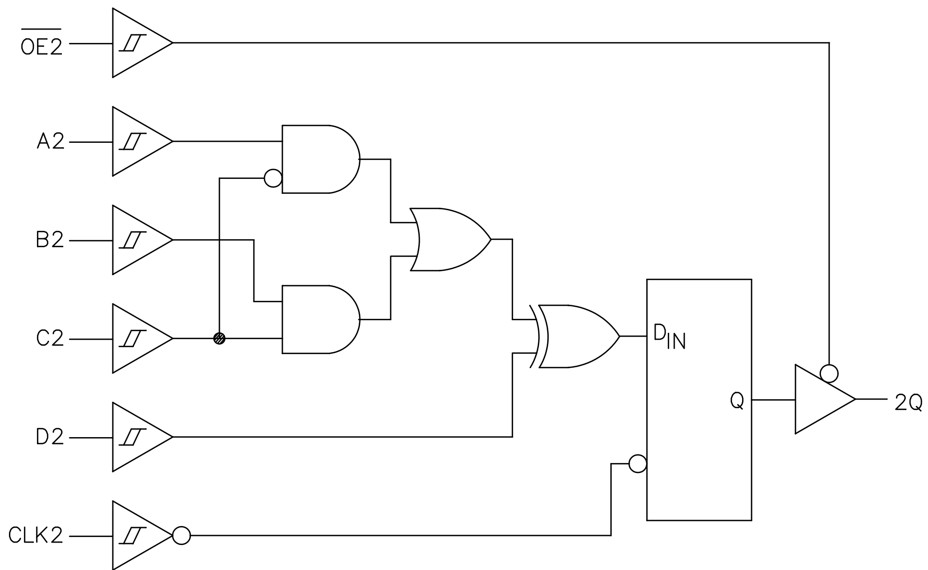
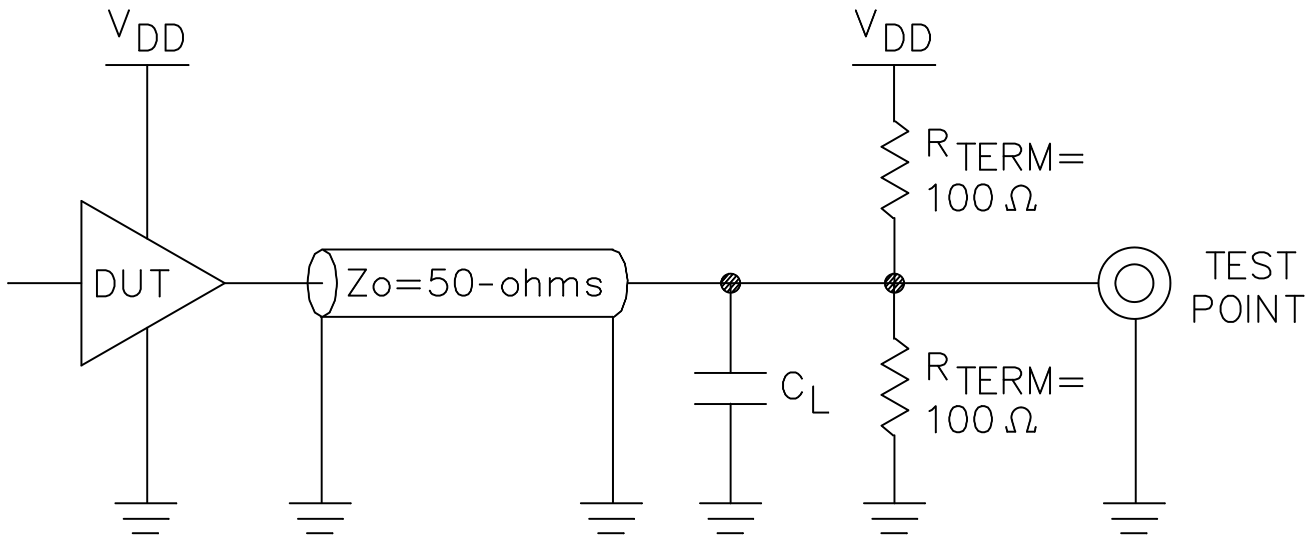


FIGURE 5. Block or Logic diagram – 1L99 Transparent Latch.



Notes: CL = 78 pF minimum or equivalent (includes scope probe and test socket).
Measurement of data output occurs at the low to high or high to low transition mid-point, typically $V_{DD}/2$.

FIGURE 6. Test circuit.

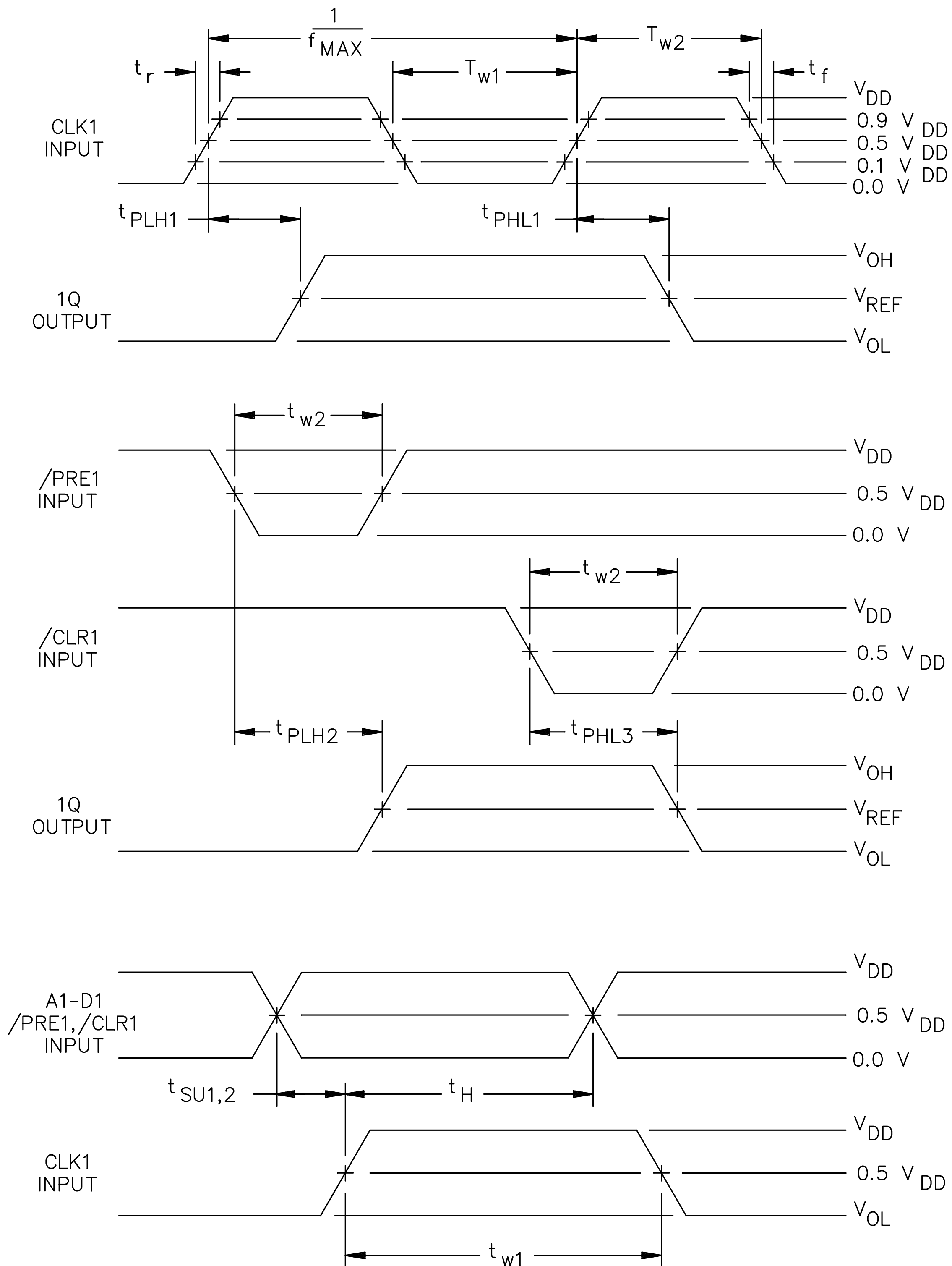


FIGURE 7. Timing waveforms – 1F99 D Flip Flop.

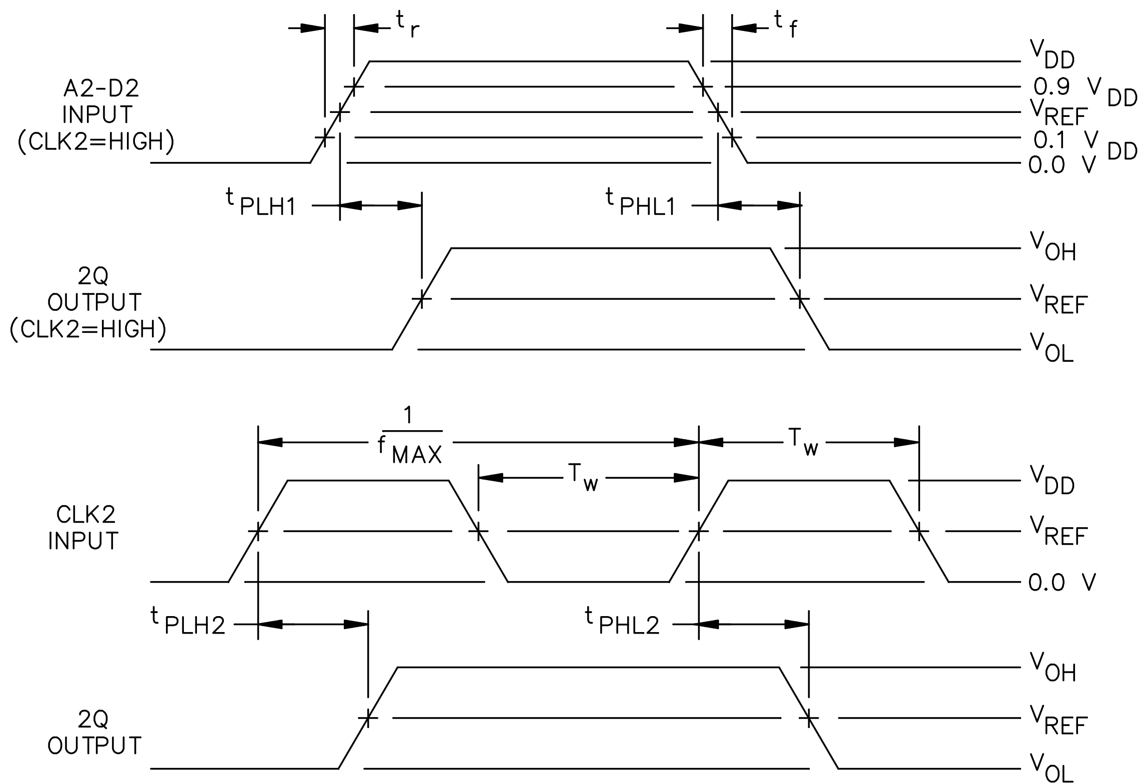


FIGURE 8. Timing waveforms – 1L99 Transparent Latch.

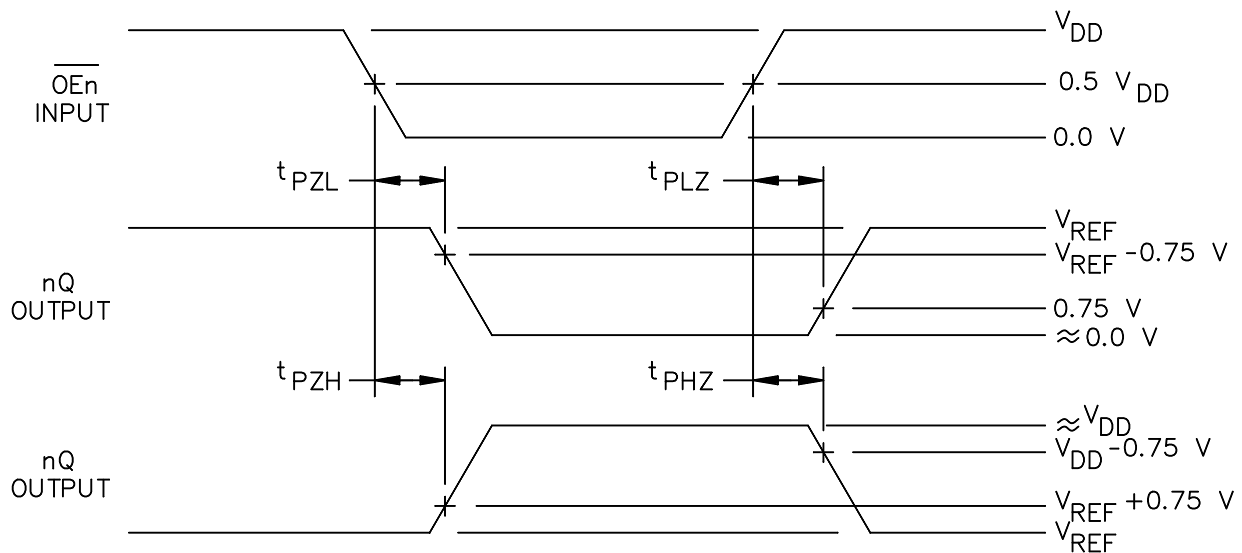


FIGURE 9. Timing waveforms – 1F99 D Flip Flop and 1L99 Transparent Latch Output Enable and Disable (High-Z).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k Rad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron irradiation. When specified in the purchase order or contract, Neutron irradiation test shall be conducted by using a neutron fluence of approximately 1 x 10^{14} neutrons/cm^2.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be the maximum rated operating temperature 25°C ±10°C for the latch-up measurements.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see table IB herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 5/

Test requirements	Subgroups (in accordance with MIL-PRF-38535, TABLE III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 4, 7, 9	1, 4, 7, 9
Static burn-in (method 1015)	Not Required	Required
Post burn-in interim electrical parameters	Not Required	1, 4, 7, 9 4/
Dynamic burn-in (method 1015)	Required	Required
Post burn-in interim electrical parameters	1, 4, 7, 9 4/	1, 4, 7, 9 4/
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11 4/
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9

1/ PDA applies to subgroup 1 (see 4.2.3). For device class V, PDA applies to subgroups 1 and 7 (see 4.2.3).
2/ The burn-in shall meet the requirements of 4.2.1a herein.
3/ On all class V lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with MIL-PRF-38535. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.
4/ Delta limits shall be required only on table IA, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.
5/ The device manufacturer may, at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias) or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table IIA).

TABLE IIB. Burn-in and operating life test delta parameters (+25°C).

Parameter 1/	Device types	
	All	
Output voltage low	V_{OL}	±100 mV
Output voltage high	V_{OH}	±100 mV
Quiescent Supply Current	I_{DDQ}	±1 µA
Input Leakage Current	I_{IN}	±100 nA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ) burn-in.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

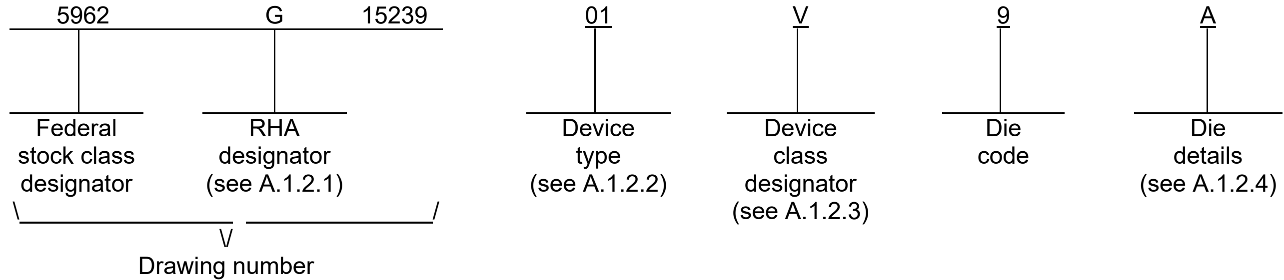
6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT54ACS2S99S	Dual, sequential, ManyGate configurable logic gate with Schmitt trigger inputs and tri-state outputs
02	UT54ACS2S99S	Dual, sequential, ManyGate configurable logic gate with Schmitt trigger inputs and tri-state outputs

.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

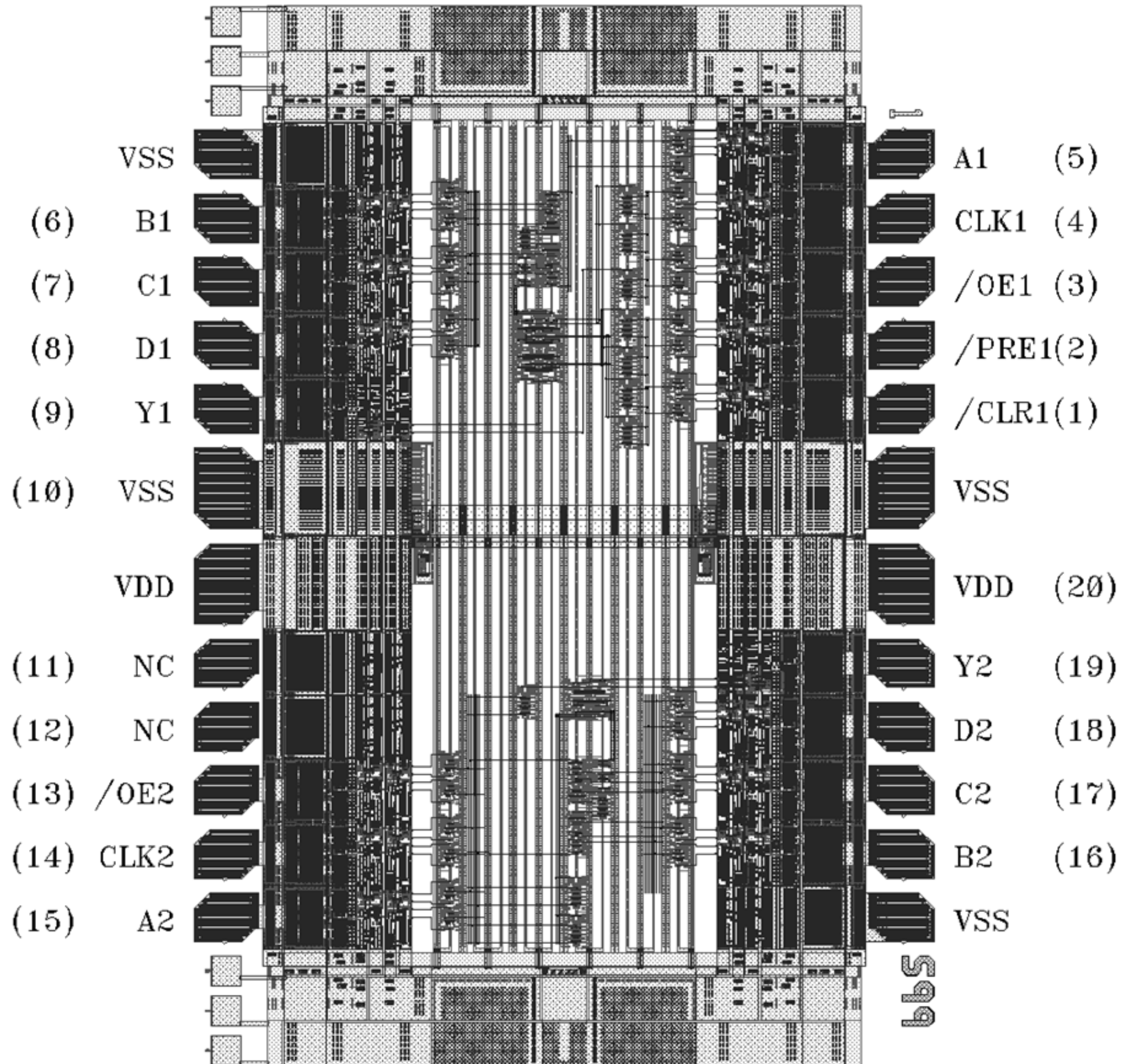
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0591.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	111 x 81 mils.
Die thickness:	17 ±1 mils

Interface materials.

Top metallization:	Si Al Cu	9.0kÅ – 12.5kÅ
Thickness:	9.0kÅ – 12.5kÅ	
Backside metallization:	None	

Glassivation.

Type:	Nitride
Thickness:	9.0 kÅ – 11.0 kÅ
Substrate:	Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to V_{SS}
Special assembly instructions:	Bond pad #10 (V_{SS}) first
	Do not wire bond the six probe ID pads

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-12-14

Approved sources of supply for SMD 5962-15239 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962G1523901QXC	65342	UTACS2S99S-XCC
5962H1523902QXC	65342	UTACS2S99S-XCC
5962G1523901QXA	65342	UTACS2S99S-XCA
5962H1523902QXA	65342	UTACS2S99S-XCA
5962G1523901VXC	65342	UTACS2S99S-XCC
5962H1523902VXC	65342	UTACS2S99S-XCC
5962G1523901VXA	65342	UTACS2S99S-XCA
5962H1523902VXA	65342	UTACS2S99S-XCA
5962G1523901V9A	65342	CAS99A_VG_DIEG
5962H1523902V9A	65342	CAS99A_VH_DIEH
5962G1523901Q9A	65342	CAS99A_QG_DIEG
5962H1523902Q9A	65342	CAS99A_QH_DIEH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Frontgrade Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.