REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add class V level device types 01-03. Add delta burn-in table IIB. Update short circuit output(I_{OSH2}) limit, propagation delay time(t_{PLHT3}) limit in table IA. – MAA.	16-10-06	Thomas M. Hess

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		
REV STATUS OF SHEETS			REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A
			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY Joshua Civiello

CHECKED BY Muhammad Akbar

APPROVED BY Thomas M. Hess

DRAWING APPROVAL DATE 16-02-22

REVISION LEVEL A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, RADIATION-HARDENED, CMOS, CONTROLLER AREA NETWORK (CAN) FD TRANSCEIVER, MONOLITHIC SILICON.

SIZE	CAGE CODE	
A	**67268**	**5962-15232**

SHEET 1 OF 32

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	R	15232	01	V	X	C
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

_______________ _______________/
V
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT64CAN3330	CAN FD transceiver with low power sleep mode
02	UT64CAN3331	CAN FD transceiver with bus isolated diagnostic loopback
03	UT64CAN3332	CAN FD transceiver with local controller baud rate match

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	8	Flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{DD})	-0.3 V dc to +6.0 V dc 2/
Voltage on any pin, (V_{IN})	-0.3 V dc to 5.5 V dc 2/
$V_{CANH/L}$	
Voltage on CANH and CANL bus terminal pin (On-orbit)	-16 V dc to +16 V dc 3/
Voltage on CANH and CANL bus terminal pin (Terrestrial)	-36 V dc to +36 V dc 3/
Input/Output current, (I_{IO}) DC current per pin @ T_J =125ºC for 20 years	$\pm$ 10 mA
Power dissipation, P_D @ T_C = 125ºC	1.67 W 4/
Case temperature range, (T_C)	-55ºC to +125ºC
Storage temperature range, (T_{STG})	-65ºC to +165ºC
Junction temperature, (T_J)	+150ºC
Thermal resistance, junction-to-case, (θ_{JC}): Case X	15ºC/W
ESD Protection (CANH, CANL), ESD_{HBM}	4000 V 5/
ESD Protection (TXD, RXD, RS, $\overline{ZZ}$, AB), ESD_{HBM}	2000 V 5/

1.4 Recommended operating conditions.

Operating supply voltage range, (V_{DD})	+3.0 V dc to +3.6 V dc
V_{CANH}	-7.0 V dc to +12 V dc
V_{CANL}	-7.0 V dc to +12 V dc
Supply voltage, (V_{SS})	0 Vdc
Voltage on TTL, ($V_{I/O}$)	0 Vdc to +5.5 Vdc
Differential input voltage, (V_{ID})	-6 Vdc to +6 Vdc
Bias input to RS pin, (RS_{BIAS})	
Bias input to RS pin for standby	0.75*V_{DD} to V_{DD}
Bias input to RS pin for slope control	10 kΩ to +100 kΩ
Bias input to RS pin for high speed (8 Mbps)	V_{SS} to 0.3 V
Case operating temperature range, (T_C)	-55ºC to +125ºC

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	100K Rad(Si) 6/
Single event phenomenon (SEP):	
No SEL occurs at effective LET, (see 4.4.4.3)	$\leq$ 117 MeV/(mg/cm^2) 7/

1/ Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

2/ All voltage values in this drawing are with respect to V_{SS}.

3/ Radiation effects can adversely affect the reliability and performance of the device during this condition. Contact a factory representative to evaluate the reliability based on the exposure to exposure to radiation

4/ Per MIL-STD-883, Method 1012.1, Section 3.4.1, $P_D=(T_J(max)-T_C(max))/\theta_{JC}$)

5/ Per MIL-STD-883, Method 3015, Table 3

6/ Per MIL-STD-883, Method 1019, Condition A

7/ SEL is performed at V_{DD} = 3.6V at 125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

JEDEC INTERNATIONAL (JEDEC)

JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block Diagrams. The block diagrams shall be as specified on figure 3.

3.2.4 Truth table. The truth table shall be as specified on figure 4.

3.2.5 Output load circuit. The output load circuit shall be as specified on figure 5.

3.2.6 Timing waveforms. The timing waveforms shall be as specified on figure 6

3.2.7 Radiation test circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.8 Functional tests. Various functional tests used to test this device are contained in the appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in Table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table IIA. The electrical tests for each subgroup are defined in Table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ -55ºC ≤ T_C ≤ +125ºC +3.0 V ≤ V_{DD} ≤ +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current maintaining a dominant output	I_{DD1}	TXD=0V, R_L=∞, RS=0V, AB=0V, $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	-	18	mA
	I_{DD2}	TXD=0V, R_L=60Ω ±1%, RS=0V, AB=0V, $\overline{ZZ}$=V_{DD}, LBK=0V	1,2,3	All		60	
Supply current receiving a dominant bus input	I_{DD3}	TXD=V_{DD}, R_L=60Ω ±1%, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{ID}=1.4V, V_{IC}=2.5V	1,2,3	All		3	mA
Supply current maintaining a Recessive output	I_{DD4}	TXD=V_{DD}, R_L=∞, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All		3	mA
	I_{DD5}	TXD=V_{DD}, R_L=60Ω ±1%, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All		3	
	I_{DD6}	TXD=V_{DD}, R_L=60Ω ±1%, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{ID}=0.0V, V_{IC}=2.5V	1,2,3	All		3	
Supply Current Operating In Sleep Mode	I_{DD7}	R_L=∞, $\overline{ZZ}$=0V, TXD=V_{DD}, RS=0V or V_{DD}, V_{ID}=0.0V, V_{IC}=2.5V	1,2,3	01		60	µA
	I_{DD7A}	R_L=60Ω ±1%, $\overline{ZZ}$=0V, TXD=V_{DD}, RS=0V or V_{DD}				60	
	I_{DD8}	R_L=60Ω ±1%, , $\overline{ZZ}$=0V, TXD=V_{DD}, RS=0V or V_{DD}				115	
Standby supply current	I_{DD9}	R_L=∞, RS=V_{DD}, TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All		1.6	mA
	I_{DD10}	R_L=60Ω ±1%, RS=V_{DD}, TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All		1.65	mA
	I_{DD11}	R_L=60Ω ±1%, RS=V_{DD}, TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{ID}=0.0V, V_{IC}=2.5V	1,2,3	All		1.6	mA
Supply Current Under High Voltage Fault 2/	I_{DD12}	R_L=∞, RS=0V, TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, $V_{CANH/L}$=+/-24V	1,2,3	All		6	mA
Supply Current Operating in Auto Loopback	I_{DD13}	R_L=∞, RS=0V, TXD=0V, AB=V_{DD}	1,2,3	03		3	mA
	I_{DD13A}	R_L=60Ω ±1%, RS=0V, TXD=0V, AB=V_{DD}	1,2,3			3	
	I_{DD13B}	R_L=60Ω ±1%, RS=0V, TXD=0V, AB=V_{DD}, V_{ID}=1.4V, V_{IC}=2.5V	1,2,3			3	
Supply Current Operating in Diagnostic Loopback	I_{DD14}	R_L=∞, RS=0V, TXD=0V, LBK=V_{DD}	1,2,3	02		3	mA
	I_{DD14A}	R_L=60Ω ±1%, RS=0V, TXD=0V, LBK=V_{DD}	1,2,3			3	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55^{\circ}C \le T_C \le +125^{\circ}C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Bus output voltage (dominant) CANH	V_{CANH1}	TXD=0V, RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	2.45	V_{DD}	V
Bus output voltage (dominant) CANL	V_{CANL1}	TXD=0V, RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	0.50	1.25	V
Bus output voltage (recessive) CANH	V_{CANH2}	TXD= V_{DD}, RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	2.0	3.0	V
Bus output voltage (recessive) CANL	V_{CANL2}	TXD=V_{DD}, RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	2.0	3.0	V
Differential output voltage (dominant)	V_{ODD1}	TXD=0V, RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	1.5	3.0	V
	V_{ODD2}	TXD=0V, RS=0V, V_{TEST} = -7 to +12V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	1.2	3.0	
Differential output voltage (recessive)	V_{ODR1}	TXD=V_{DD}, RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	–120	12	mV
	V_{ODR2}	TXD=V_{DD}, RS=0V, R_L=∞, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	–500	50	mV
Short-circuit output 3/	I_{OSH1}	V_{CANH}=-7 V, CANL=∞, TXD=0V, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	-250		mA
	I_{OSH2}	V_{CANL}=12 V, CANL=∞, TXD=0V, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All		3	
	I_{OSL1}	V_{CANL}=-7 V, CANH=∞, TXD=0V, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All	-1		
	I_{OSL2}	VCANL=12, CANH=∞,TXD=0V, RS=0V, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	1,2,3	All		250	

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55ºC < TC < +125ºC +3.0 V < VDD < +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver							
Positive-going input threshold voltage	V_{IT+}	AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{IC}=2.5V	4,5,6	All		900	mV
Negative-going input threshold voltage	V_{IT-}		4,5,6	All	500		
Hysteresis voltage	V_{HST}	V_{HST}=V_{IT+} – V_{IT-}	4,5,6	All	20		
Bias input current	I_{IR1}	V_{CANH} or V_{CANL} = 12V; TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK =0V, Other bus pin (V_{CANH} or V_{CANL}) at 0V	4,5,6	All		500	µA
	I_{IR2}	V_{CANH} or V_{CANL} = 12V and V_{DD} ≤ V_{SS}+0.3V	4,5,6	All		600	
	I_{IR3}	V_{CANH} or V_{CANL}= –7V	4,5,6	All	-610		
	I_{IR4}	V_{CANH} or V_{CANL}= –7V and V_{DD} ≤ V_{SS}+0.3V	4,5,6	All	-450		
CANH Capacitance 4/	C_H	CANH to V_{SS}, V_I=0.025*Sin(2E6πt)+2.3V, TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	4,5,6	All		50	pF
CANL Capacitance 4/	C_L	CANL to V_{SS}, V_I=0.025*Sin(2E6πt)+2.3V, TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	4,5,6	All		50	
Differential capacitance 4/	C_{ID}	CANH to CANL, V_I = 0.025*Sin(2E6πt), TXD=V_{DD}, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	4,5,6	All		25	
Differential input resistance	R_{ID}	AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	4,5,6	All	40	100	kΩ
Single ended input resistance CANH	R_H		4,5,6	All	20	50	
Single ended input resistance CANL	R_L		4,5,6	All	20	50	
Percent difference between RH and RL	R_M	2*|(RL-RH)|/(RL+RH)*100	4,5,6	All		3.0	%

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55^{\circ}C \le T_C \le +125^{\circ}C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Analog Input (RS)							
Input voltage for enabling High-speed mode (8Mbps operation)	V_{RS1}	TXD=V_{DD}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	9,10,11	All	V_{SS}	300	mV
Input Voltage for enabling Standby mode	V_{RS2}	TXD=V_{DD}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V	9,10,11	All	0.75*V_{DD}	5.5	V
High-Speed mode input current	I_{RS1}	V_{RS}=0V	9,10,11	All	-500	-100	µA
Standby mode input current	I_{RS2}	V_{RS}=0.75*V_{DD}	9,10,11	All		30	µA
	I_{RS3}	V_{RS}=5.5V	9,10,11	All		50	µA
Cold sparing leakage current	I_{RS4}	V_{RS}=5.5V or $V_{RS} \le 0.3V$, $V_{DD} \le V_{SS}+0.3V$	9,10,11	All	-20	20	µA
TTL I/O (TXD, $\overline{ZZ}$ AB, RXD, LBK)							
Input Voltage High	V_{IH}		9,10,11	All	2.00		V
Input Voltage Low	V_{IL}		9,10,11	All		0.8	V
Input leakage current on TXD	I_{IOD}	V_{in}=0V or V_{in}=5.5V	9,10,11	All	-60	100	µA
Input leakage current on pins ($\overline{ZZ}$, AB, LBK)	I_{IO}	V_{in}=0V or V_{in}=5.5V	9,10,11	All	-10	100	µA
Cold sparing leakage current (TXD, $\overline{ZZ}$ AB, RXD, LBK)	I_{CS}	V_{in}=0.0V and V_{in}=5.5V, $V_{DD} \le V_{SS}+0.3V$	9,10,11	All	-20	20	µA
Output high voltage on RXD	V_{OH}	I_{OH}=-4mA	9,10,11	All	2.4		V
Output Low voltage on RXD	V_{OL}	I_{OL}=4mA	9,10,11	All		0.4	V
Input Capacitance 3/	C_{IO}	TXD or $\overline{ZZ}$ or AB or RXD or LBK to V_{SS}, V_I=0.025*Sin(2E6πt), RS=0V	9,10,11	All		10	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55ºC ≤ T_C ≤ +125ºC +3.0 V ≤ V_{DD} ≤ +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Driver AC Electronics Characteristics							
Propagation delay time (TXD input dominant to CAN dominant 5/	t_{PLHT1}	RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		85	ns
	t_{PLHT2}	RS with 10kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125 kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		260	
	t_{PLHT3}	RS with 100kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK= 0V, V_{TXD} ≤ 125 kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		1200	
Propagation delay time, (TXD recessive to CAN recessive) 5/	t_{PHLT1}	RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		120	ns
	t_{PHLT2}	RS with 10kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50 Ω)	9,10,11	All		485	
	t_{PHLT3}	RS with 100kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50 Ω)	9,10,11	All		1650	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55ºC ≤ T_C ≤ +125ºC +3.0 V ≤ V_{DD} ≤ +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse skew (|tPHL – tPLH|) 5/	t_{SKPT1}	RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		75	ns
	t_{SKPT2}	RS with 10kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		450	
	t_{SKPT3}	RS with 100kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O 50Ω)	9,10,11	All		1250	
Differential CAN signal rise time 3/ 5/	t_{RT1}	RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All	5	80	ns
	t_{RT2}	RS with 10kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6 s, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All	14	250	
	t_{RT3}	RS with 100kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All	40	1000	
Differential CAN signal fall time 3/ 5/	t_{FT1}	RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All	20	75	ns
	t_{FT2}	RS with 10kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All	30	185	
	t_{FT3}	RS with 100kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All	40	800	
Enable time from standby deactivate to CAN dominant	t_{ENS}	TXD=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{RS} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω, RS < 0.75*V_{DD})	9,10,11	All		1.5	µs
Enable time from sleep deactivate to CAN dominant	t_{ENZ}	RS=0V, TXD=0V, R_L=60Ω ±1%, $V_{\overline{ZZ}}$ ≤ 50kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	01		7	µs

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55ºC ≤ T_C ≤ +125ºC +3.0 V ≤ V_{DD} ≤ +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Disable time from standby assert to CAN recessive	t_{DISS}	TXD=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{RS} ≤ 125kHz (Square wave , 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω, RS ≥ 0.75*V_{DD})	9,10,11	All		150	ns
Disable time from sleep assert to CAN recessive	t_{DISZ}	RS=0V, TXD=0V, R_L=60Ω ±1%, $V_{\overline{ZZ}}$ ≤ 50kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	01		100	ns
Receiver AC Electronics Characteristics							
Propagation delay time (CANH recessive to RXD recessive) 5/	t_{PLHR}	RS=0V, TXD=V_{DD}, R_L=∞ Ohms AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{CANH} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O =50Ω), V_{CANL}=1.25V	9,10,11	All		60	ns
Propagation delay time (CANH dominant to RXD dominant) 5/	t_{PHLR}	RS=0V, TXD=V_{DD}, R_L=∞ Ohms AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{CANH} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω), V_{CANL}=1.25V	9,10,11	All		60	ns
Pulse skew	t_{SKPR}	t_{SKPR} =(|t_{PHLR} – t_{PLHR}|)	9,10,11	All		25	ns
RXD output signal rise time 3/ 5/	t_{RR}	RS=0V, TXD=V_{DD}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{CANH} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω), V_{CANL}=1.50V	9,10,11	All		5	ns
RXD output signal fall time 3/ 5/	t_{FR}	RS=0V, TXD=V_{DD}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{CANH} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω), V_{CANL}=1.50V	9,10,11	All		5	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55ºC ≤ T_C ≤ +125ºC +3.0 V ≤ V_{DD} ≤ +3.6 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Transceiver Loopback AC Electronics Characteristics							
Total loop delay, TXD to RXD, dominant 5/	t_{LOOPD1}	RS=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		125	ns
	t_{LOOPD2}	R_S with 10kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		800	
	t_{LOOPD3}	R_S with 100kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		1500	
Total loop delay, TXD to RXD, recessive 5/	t_{LOOPR1}	R_S=0V, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		125	ns
	t_{LOOPR2}	R_S with 10kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		800	
	t_{LOOPR3}	R_S with 100kΩ to V_{SS}, R_L=60Ω ±1%, AB=0V or $\overline{ZZ}$=V_{DD} or LBK=0V, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	All		1650	
Loopback delay, TXD to RXD 5/	t_{LBK}	R_S=0V, R_L=60Ω ±1%, LBK=V_{DD}, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	02		20	ns
Loopback delay, TXD to RXD 5/	t_{AB1}	R_S=0V, R_L=60Ω, AB=V_{DD}, V_{TXD} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	03		20	ns
Loopback delay, CAN input to RXD 5/	t_{AB2}	R_S=0V, TXD=V_{DD}, R_L=∞ Ohms AB=V_{DD}, V_{CANH} ≤ 125kHz (Square wave, 50% duty cycle, tr ≤ 6ns, tf ≤ 6ns, Z_O=50Ω)	9,10,11	02		60	ns

See footnote next page

TABLE IA. Electrical performance characteristics - Continued.

1/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, these devices are only characterized at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C

2/ Guaranteed by characterization for $V_{CANH/L}$ = ± 36 V

3/ Guaranteed by characterization

4/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in Table IA.

5/ For C_L = 75pF or equivalent on the ATE or 15pF ±20% for bench test characterization.

TABLE IB. SEP test limits . 1/ 2/

Device Type	Single Event Latch-up (SEL) Test 3/ Bias V_{DD} = 3.6 V
	Effective LET no Latch-up
All	LET ≤117 MeV-mg/cm^2

1/ For SEP test conditions, see 4.4.4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature for latch-up test T_A = +125°C ±10°C.

Case outline X

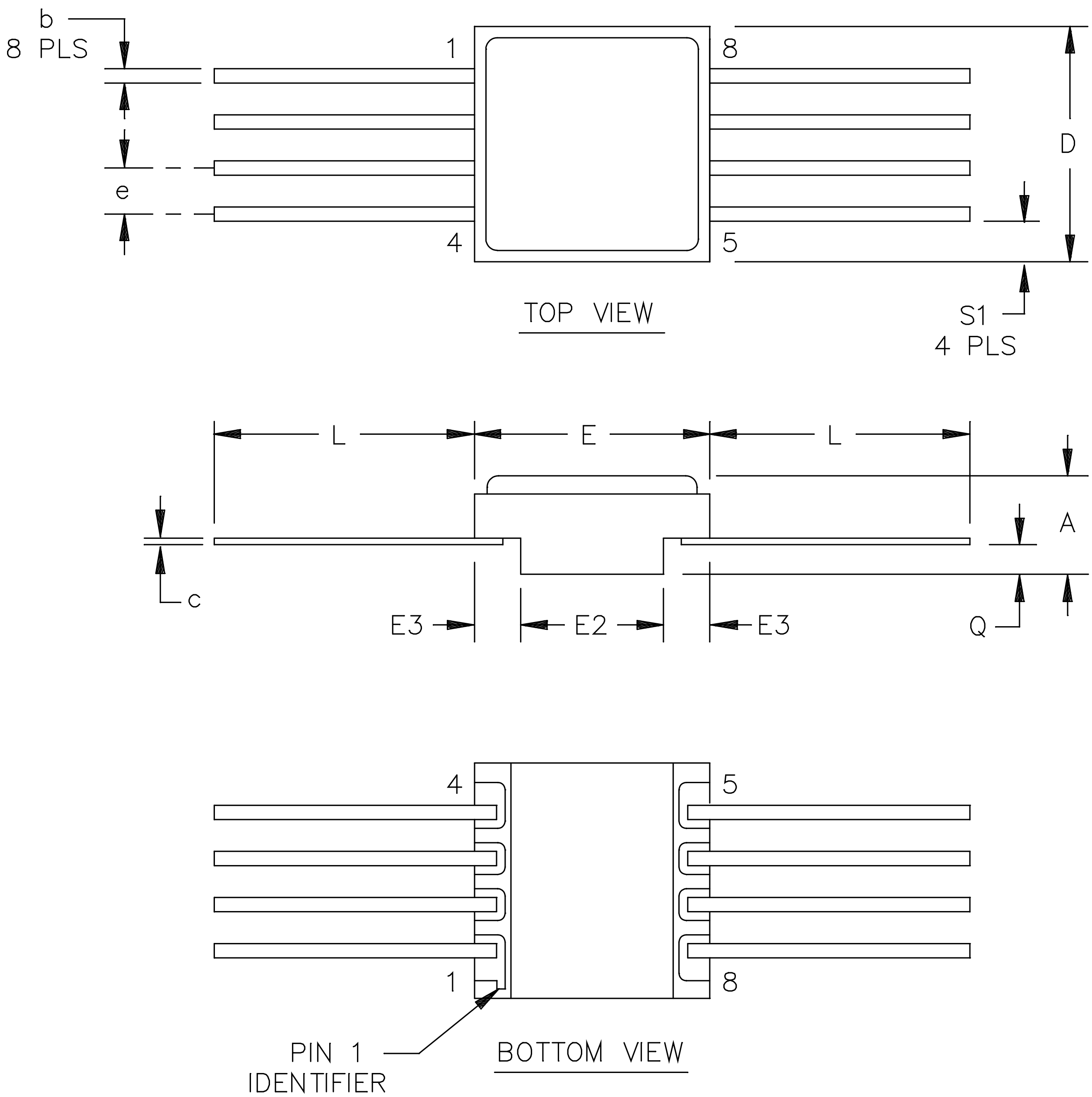


FIGURE 1. Case outline

Case outline X

Symbol	Millimeters	
	Min	Max
A	3.05 max	
b	0.38	0.48
c	0.102	0.152
D	6.35	6.61
e	1.27 typ.	
E	6.35	6.61
E2	4.32	4.58
E3	1.015 typ.	
L	8.25 max	
Q	0.66 min	
S1	0.92	1.32

NOTES:

1. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
2. The seal ring and lids are electrically connected to V_{SS}.
3. Lead finish is in accordance with MIL-PRF-38535.
4. Package material: opaque 90% minimum alumina ceramic.
5. ESD classification mark or dot is located in the pin 1 corner within area shown.

FIGURE 1. Case outline - Continued

Case X

Device type	01
Case outline	X
Terminal number	Terminal symbol
1 2 3 4 5 6 7 8	TXD V_{SS} V_{DD} RXD $\overline{ZZ}$ CANL CANH RS

Device type	02
Case outline	X
Terminal number	Terminal symbol
1 2 3 4 5 6 7 8	TXD V_{SS} V_{DD} RXD LBK CANL CANH RS

Device type	03
Case outline	X
Terminal number	Terminal symbol
1 2 3 4 5 6 7 8	TXD V_{SS} V_{DD} RXD AB CANL CANH RS

FIGURE 2. Terminal connections

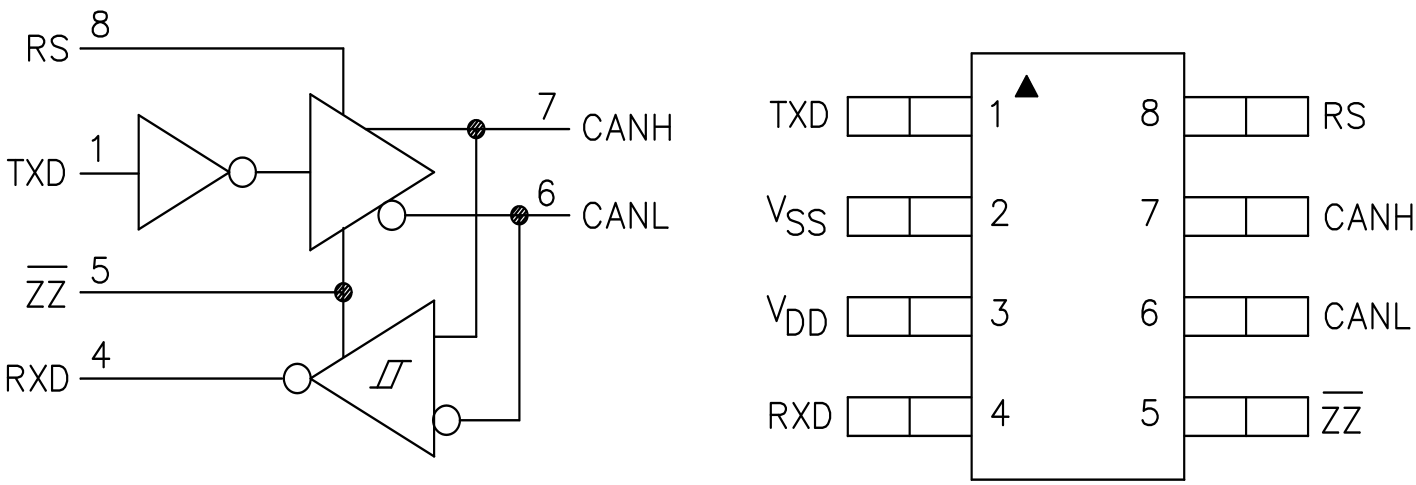


FIGURE 3. Block Diagrams Device Type 01 (Sleep)

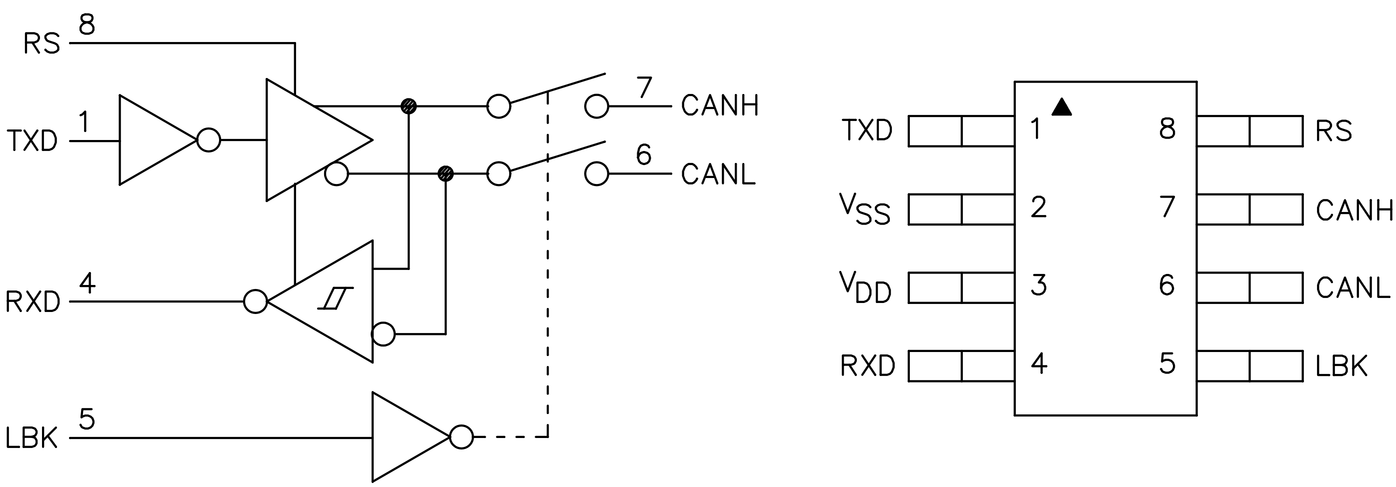


FIGURE 3. Block Diagrams Device Type 02 (Diagnostic Loopback) - continued

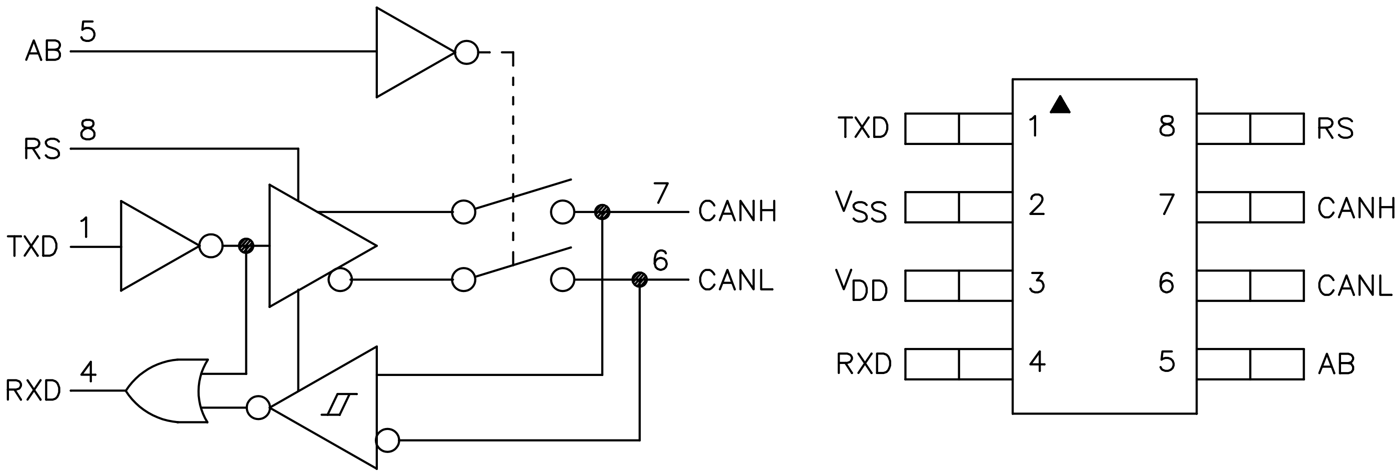
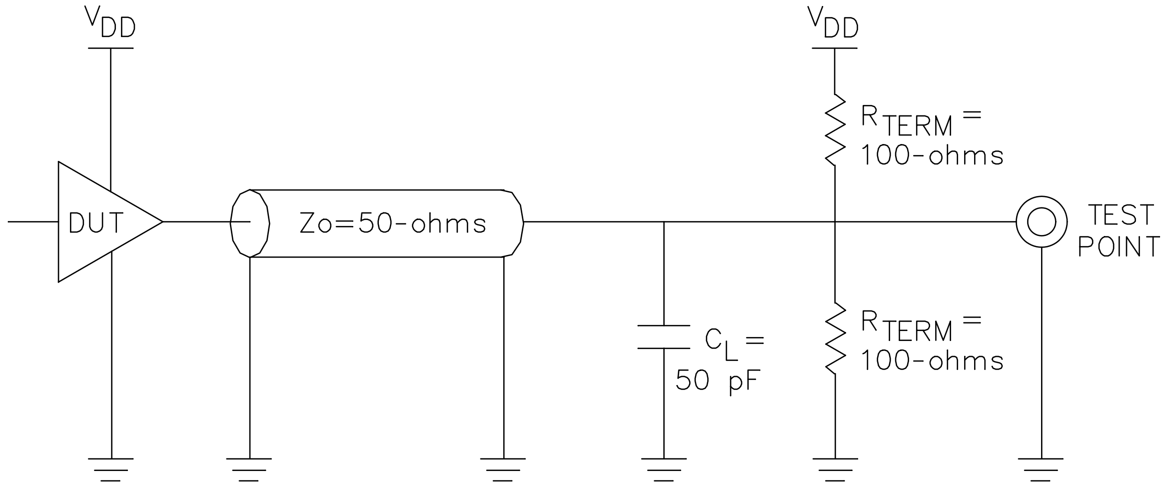


FIGURE 3. Block Diagrams Device Type 03 (Auto-Baud Loopback) - continued

INPUT		OUTPUT		MEASURED
V_{CANH}	**V_{CANL}**	**R**		**$\|V_{ID}\|$**
–6.1 V	–7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
–1 V	–7 V	L		6 V
12 V	6 V	L		6 V
–6.5 V	–7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
–7 V	–1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X

Figure 4 Differential Input Voltage Threshold Test Truth Table



Notes: 1. 50 pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point, typically, $V_{DD}/2$

FIGURE 5. Output load circuit

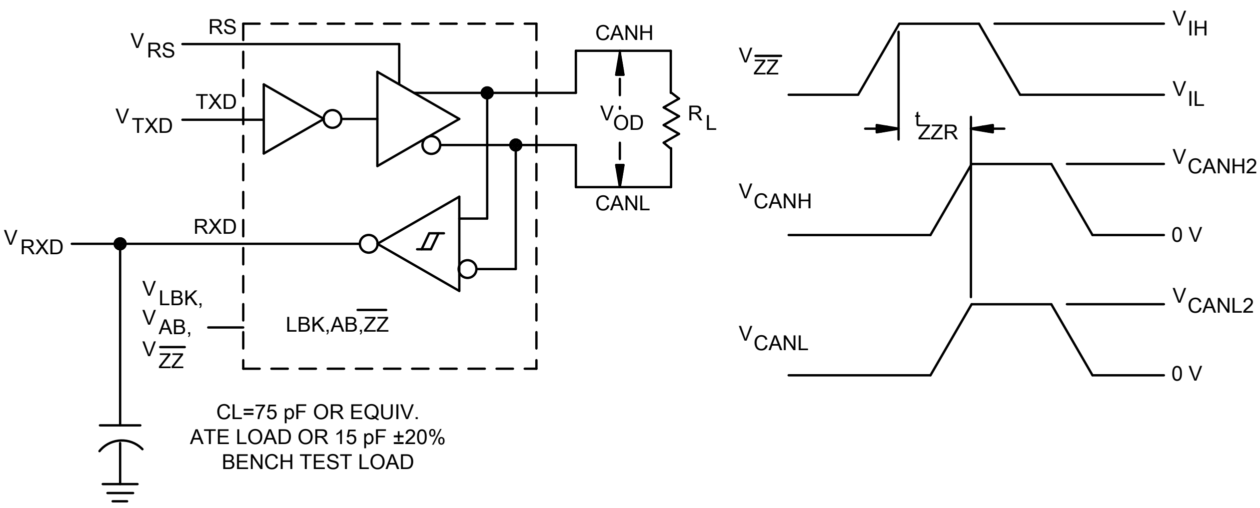


FIGURE 6. Timing waveforms (DC Test Configuration)

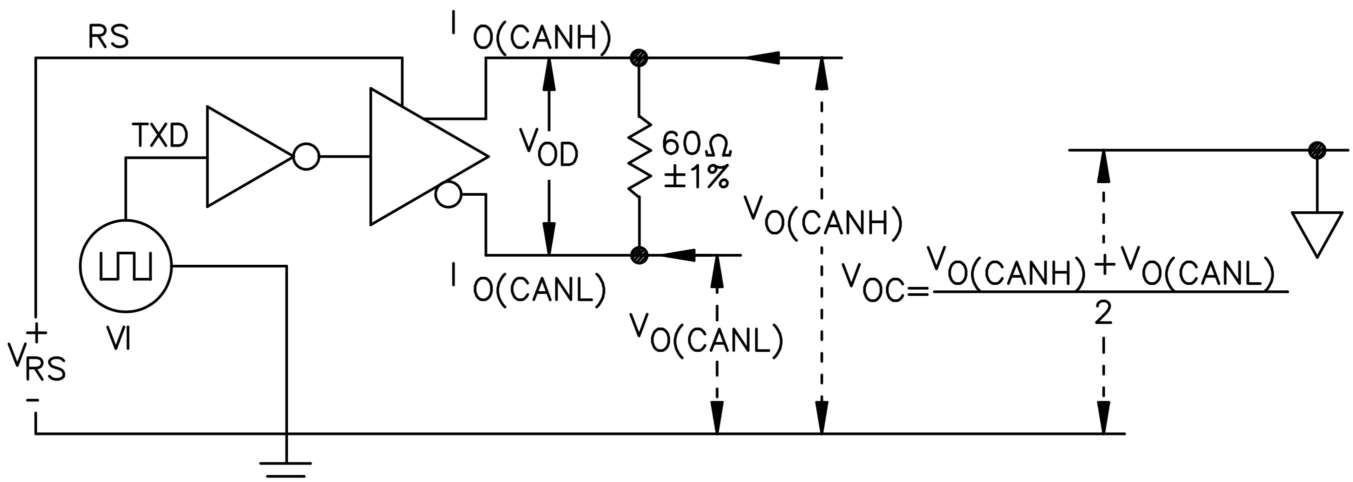


FIGURE 6 Timing waveforms (Driver Voltage, Current, and Test Definition) - Continued

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-15232
DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990		REVISION LEVEL A	SHEET 21

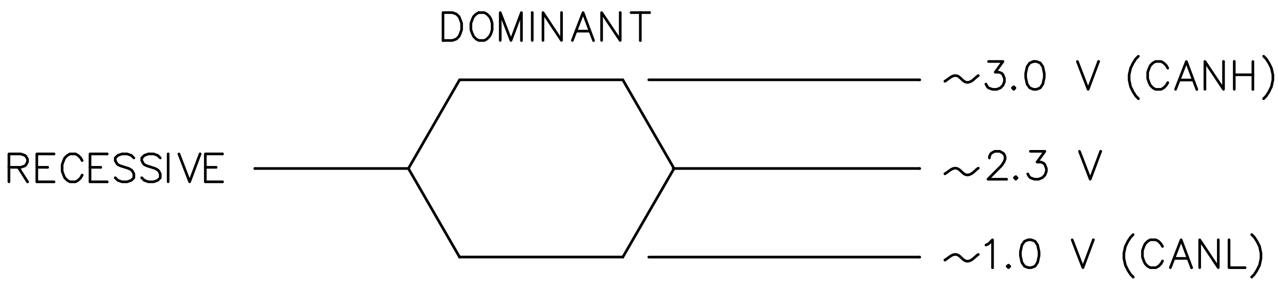


FIGURE 6 Timing waveforms (Bus Logic State Voltages Definitions) - continued

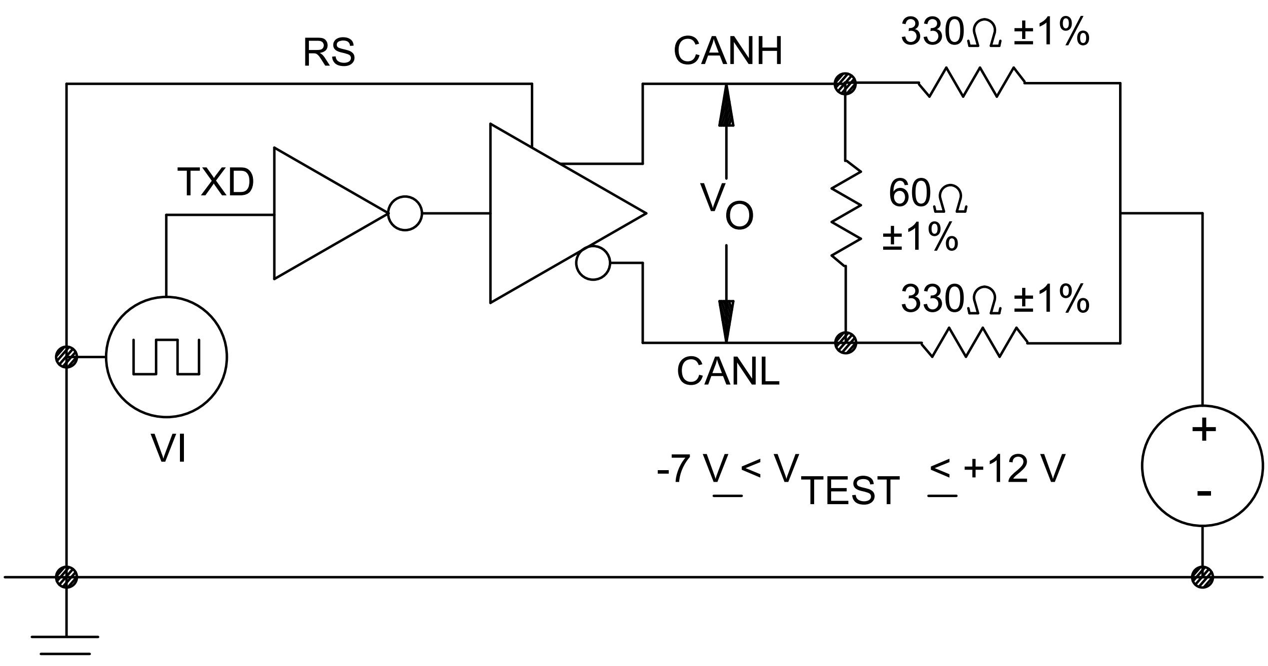


FIGURE 6 Timing waveforms (Driver V_{OD}) - Continued

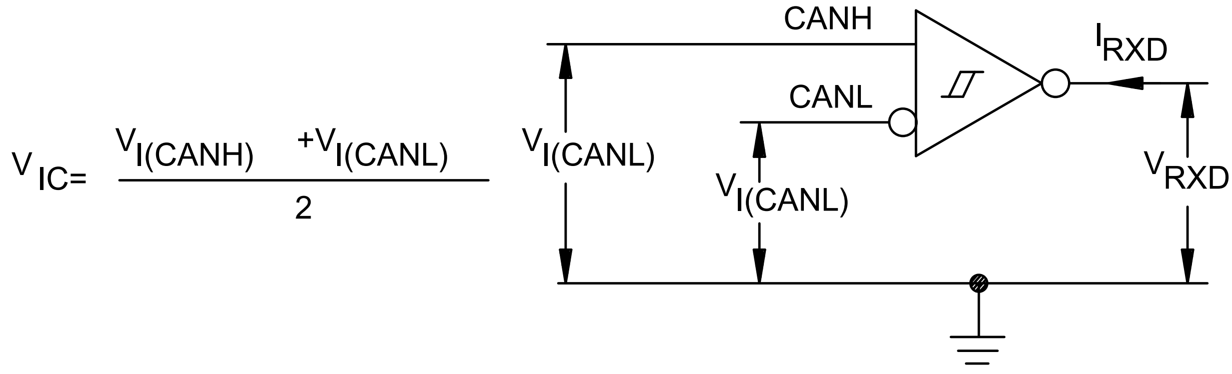


FIGURE 6 Timing waveforms (Receiver Voltage and Current Definitions) - Continued

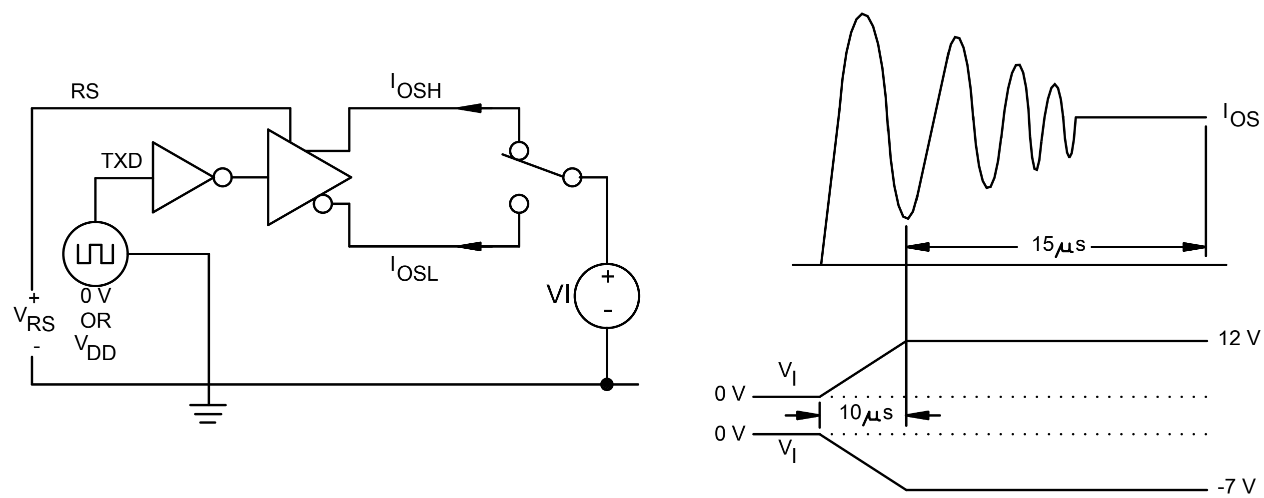


FIGURE 6 Timing waveforms (IOS Test Circuit and Waveforms) - Continued

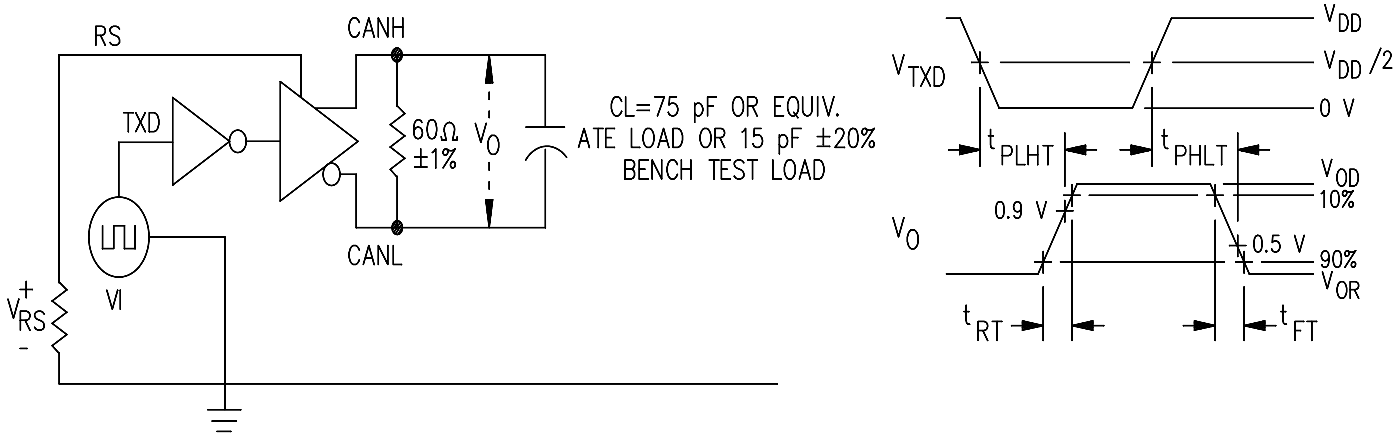


FIGURE 6 Timing waveforms (Drive Test Circuit and Voltage Waveforms) - Continued

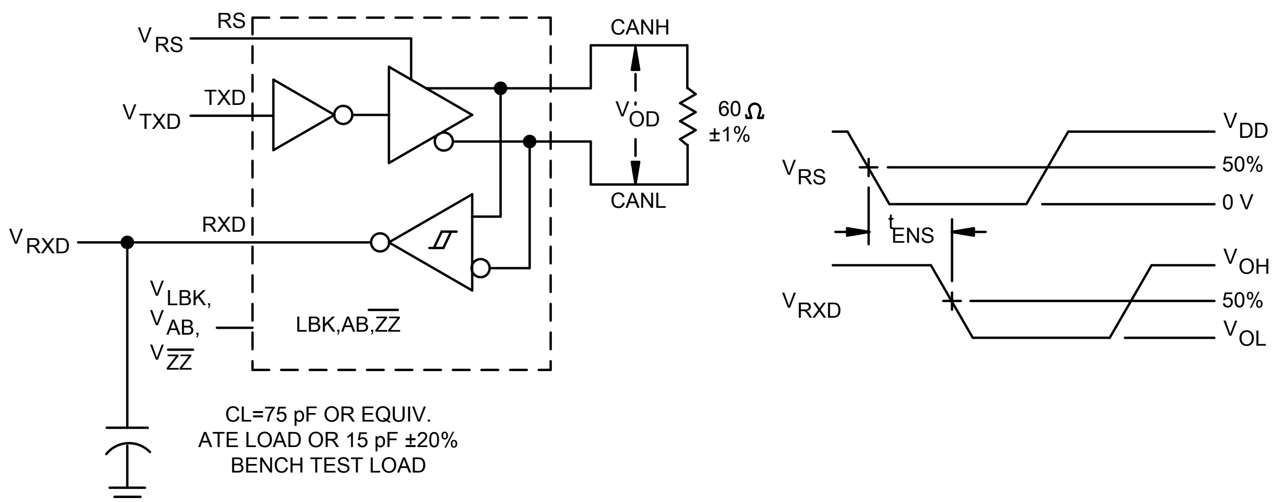


FIGURE 6 Timing waveforms (t_{ENS} and t_{DISS} Test Circuit and Voltage Waveforms) - Continued

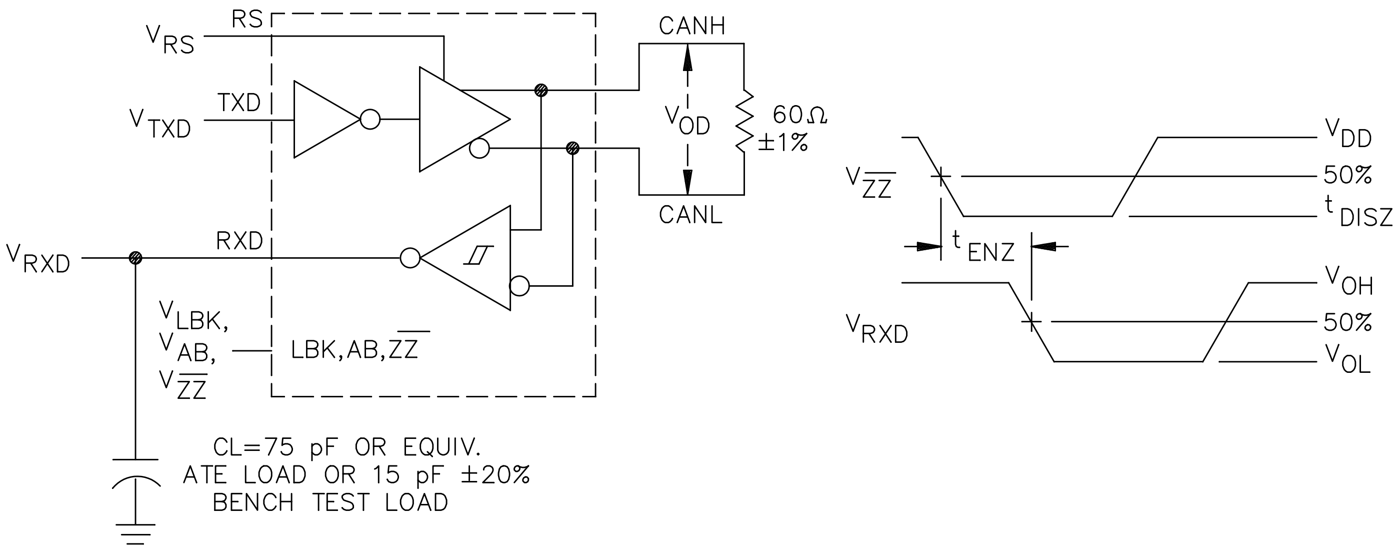


FIGURE 6 Timing waveforms (tENZ Test Circuit and Voltage Waveforms) - Continued

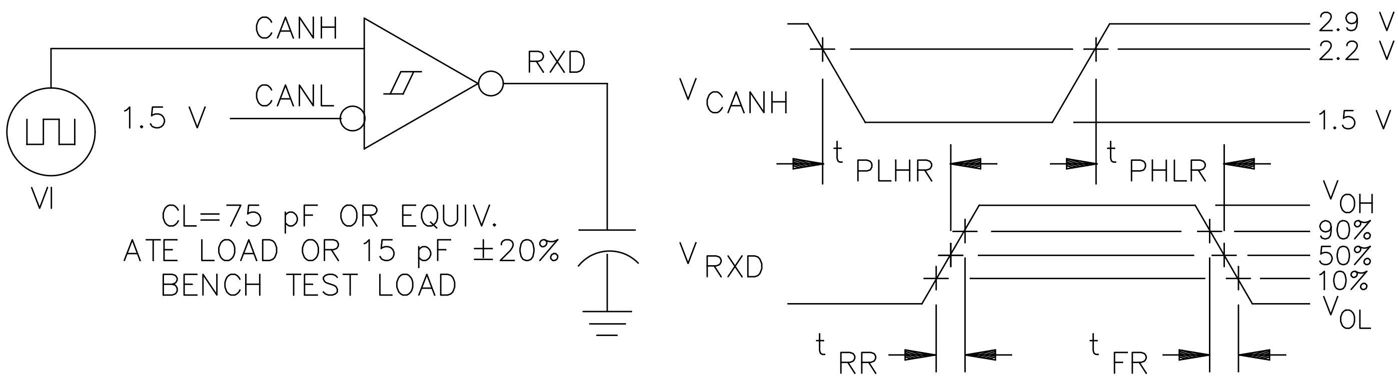


FIGURE 6 Timing waveforms (Receiver Test Circuit and Voltage Waveforms) - Continued

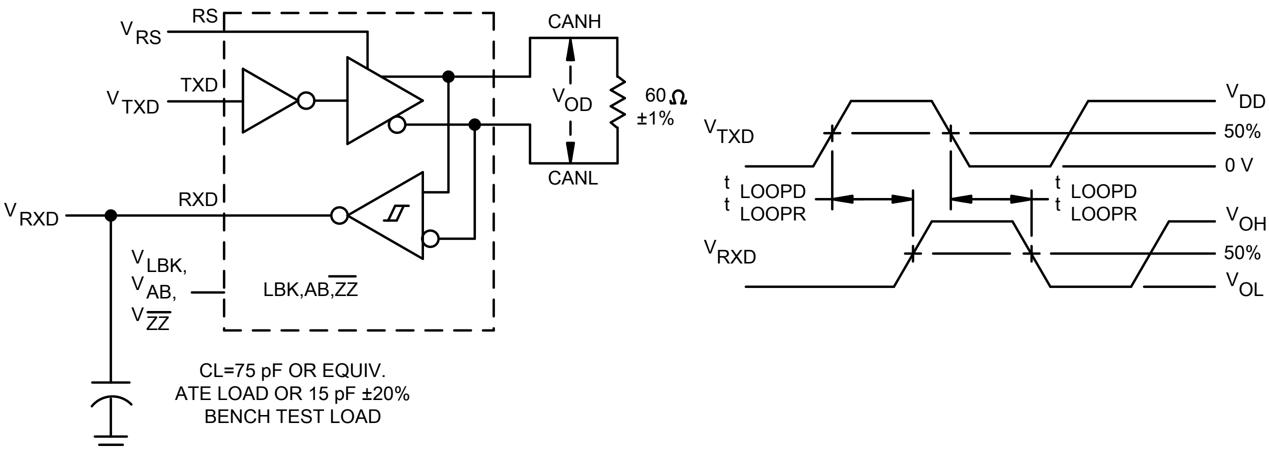


FIGURE 6 Timing waveforms (t_{LOOP} Test Circuit and Voltage Waveforms) - Continued

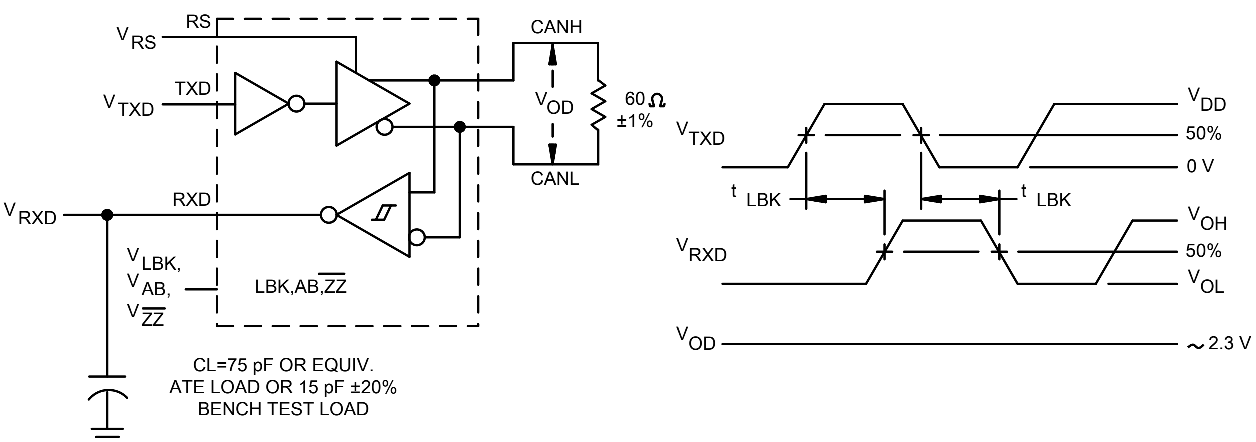


FIGURE 6 Timing waveforms (t_{LBK} Test Circuit and Voltage Waveforms) - Continued

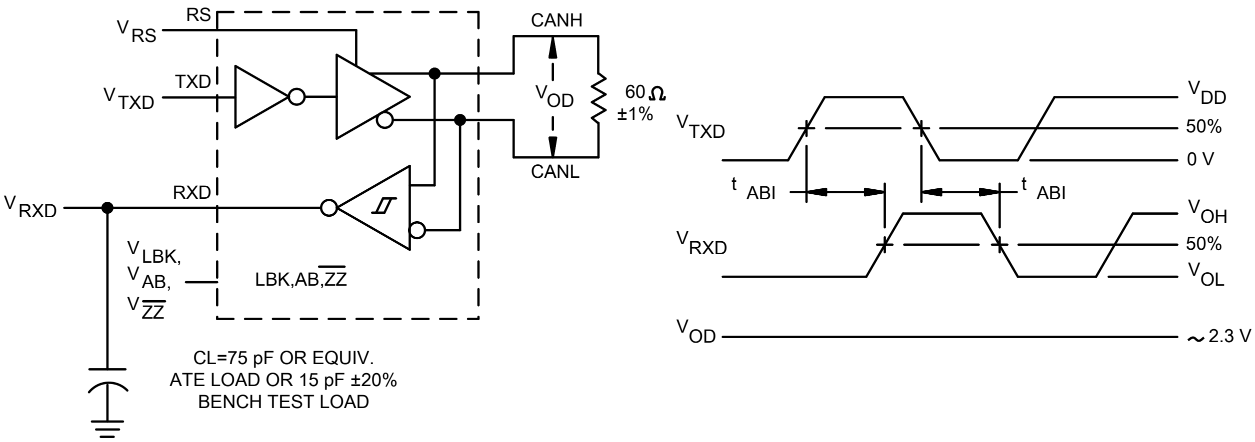


FIGURE 6 Timing waveforms (t_{AB1} Test Circuit and Voltage Waveforms) - Continued

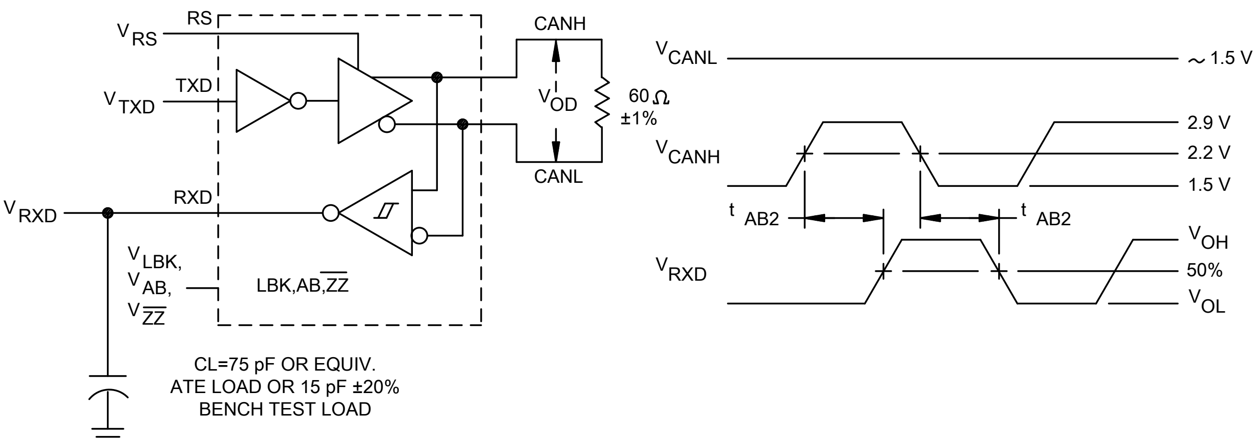


FIGURE 6 Timing waveforms (t_{AB2} Test Circuit and Voltage Waveforms) - Continued

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron irradiation. When specified in the purchase order or contract, Neutron irradiation test shall be conducted by using a neutron fluence of approximately 1×10^{14} neutrons/cm^2.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^6 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be the maximum rated operating temperature ±10°C for the latch-up measurements.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see table IB herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 5/

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,7,9	1,4,7,9
Static burn-in (method 1015)	Not Required	Required
Post burn-in interim electrical parameters	1,4,7,9	1,4,7,9 4/
Dynamic burn-in (method 1015)	Required	Required
Post burn-in interim electrical parameters	1,4,7,9	1,4,7,9 4/
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11 4/
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9

1/ PDA applies to subgroup 1 (see 4.2.3). For device class V, PDA applies to subgroups 1 and 7 (see 4.2.3).
2/ The burn-in shall meet the requirements of 4.2.1a herein.
3/ On all class V lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with MIL-PRF-38535. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.
4/ Delta limits shall be required only on table IA, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.
5/ The device manufacturer may, at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias) or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table IIA).

TABLE IIB. Burn-in and operating life test delta parameters (+25°C).

Parameters 1/	Device type	
	All	
Input voltage low, 3.0V	VIL30	± 100mV
Input voltage high, 3.0V	VIH30	± 100mV
Input voltage low, 3.6V	VIL36	± 100mV
Input voltage high, 3.6V	VIH30	± 1 00mV
Supply current maintaining a dominant output	IDD1	± 500µA
Supply current maintaining a dominant output	IDD2	± 3000µA
Supply current maintaining a recessive output	IDD4	± 300µA
Supply current maintaining a recessive output	IDD5	± 300µA
Standby supply current	IDD9	± 300µA
Standby supply current	IDD10	± 300µA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta burn-in

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614)692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Observed single event transient (SET).

c. Occurrence of latch-up (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-10-06

Approved sources of supply for SMD 5962-15232 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1523201QXC	65342	UT64CAN3330XQC
5962R1523202QXC	65342	UT64CAN3331XQC
5962R1523203QXC	65342	UT64CAN3332XQC
5962R1523201VXC	65342	UT64CAN3330XVC
5962R1523202VXC	65342	UT64CAN3331XVC
5962R1523203VXC	65342	UT64CAN3332XVC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. dba Cobham Semiconductor Solutions 4350 Centennial Blvd. Colorado Springs, CO 80907-7370