REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35	36																		
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

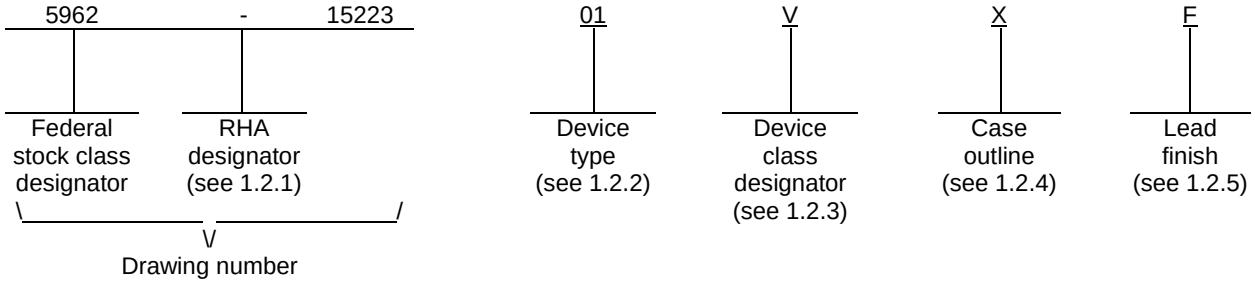
REV STATUS OF SHEETS														
REV														
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Muhammad Akbar	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Muhammad Akbar	
	APPROVED BY Thomas M. Hess	MICROCIRCUIT, 200 GHz SiGe BIPOLAR, LOW POWER 10BIT 1.5 Gsps ANALOG TO DIGITAL CONVERTER (ADC) WITH 1:1/2/4 DEMULTIPLEXER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 15-09-23	
AMSC N/A	REVISION LEVEL	SIZE A / CAGE CODE **67268** / **5962-15223**
		SHEET 1 OF 36

1. SCOPE

1.1 Scope. This drawing documents product assurance class level consisting of space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device class V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	EV10AS180A	10bit 1.5Gsps 200GHz bipolar DEMux ADC

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1.a	255	Ceramic land grid array (CLGA-Au pad termination)
Y	See figure 1.b	255	Ceramic column grid array (CI-CGA-Solder column interposer)
Z	See figure 1.c	255	Ceramic column grid array (CCGA-Cu spiral column)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device class V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Parameter	Symbol	Comments	Value	Unit
VCC5 supply voltage	VCC5	4/	GND to 6	V
VCC3 supply voltage	VCC3	4/	GND to 4.0	V
VCCO supply voltage	VCCO	4/	GND to 3.0	V
Analog input voltages	VIN or VINN	Common Mode	Min :2.0V Max 4.0V	V
Maximum difference between VIN and VINN	|VIN - VINN|		2 .0 (4 Vpp=+13dBm in 100Ω)	V
Clock input voltage	VCLK or VCLKN	Common Mode	Min :2.0V Max 4.0V	V
Maximum difference between VCLK and VCLKN	|VCLK - VCLKN|		1.5 (3 Vpp)	V
Analog input settings	VA	OA, GA, SDA, SA	-0.3 to VCC3 + 0.3	V
Control inputs	VD	SDAEN, TM0, TM1, DECN, RS0, RS1, RSTN	-0.3 to VCC3 + 0.3	V
Junction Temperature	T_J		170°C	°C
Storage Temperature	T_{STG}		-65°C to 150°C	°C

1.4 Recommended operating conditions.

Parameter	Symbol	Comments	Typ	Unit
Power supplies	V_{CC5}	No specific power supply sequencing required during power ON/OFF 4/ 5/	5.2	V
	V_{CC3}		3.3	V
	V_{CC0}		2.5	V
Differential analog input voltage (Full Scale)	V_{IN} -V_{INN}	100 Ω differential	500	mVpp
Clock input power level (Ground common mode)	P_{CLK} P_{CLKN}	100 Ω differential input	4	dBm
Operating Temperature Range	Tc, Tj	For functionality	Tc= -55°C to T_J = 125°C	°C

1/ Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Exposure to absolute maximum rating and beyond may damage the device. There is no guaranty of functionality out of the operating conditions range. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

2/ Maximum ratings enable active inputs with ADC powered off.

3/ Maximum ratings enable floating inputs with ADC powered on.

4/ The power-up of the 3 power supplies has to be completed within a limited time. Long exposure to partial powered ON supplies may damage the device.

5/ To benefit of the internal power on reset, VCC3 should be applied before VCC5. **Power Up Reset:** A power up reset ensures to synchronize internal signals and ensures output data to be properly ordered. It is generated internally by the digital section of the ADC (on VCC3 power supply) and is de-activated when VCC5 reaches 80% of its steady state value. No sequencing is required on VCCO. If VCC3 is not applied before VCC5, RSTN reset is strongly recommended to properly synchronize ADC signals [see figure 5(5.4 power up reset timing diagram)].

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device class V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figures 1.a, 1.b and 1.c.

3.2.2 Terminal connections. The terminal connections, pin out table and function description shall be as specified respectively on figures 2.1, 2.2 and 2.3.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Input and output protection networks shall be as specified on figure 6.

3.2.7 Thermal characteristic shall be as specified on figure 7.

3.2.9 Solderability test for BGA/CGA packages: Solderability test for case outline Y or Z for column grid array(CGA) or ball grid array(BGA) package has been verified during solder column or ball attachment process in accordance with method 2003 of MIL-STD-883.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device class V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device class V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device class V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Handling precaution. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling. These components are categorized as ESDS class 1C in accordance with MIL-PRF-38535.

3.9 Mounting and storage recommendation. In order to avoid the risk of solderability (or wettability) it is recommended to mount the component onto the PCB within 2 years after the date of sealing.

TABLE I. Electrical performance characteristics.

Test description	Symbol	Conditions 1/ -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Power supply voltages: Analog(V_{CC5}), Analog core and digital(V_{CC3}) and Output buffer(V_{cc0})	V_{CC5}		01	1, 2, 3	5.0	5.5	V
	V_{CC3}				3.15	3.45	
	V_{CC0}				2.4	2.6	
Leakage current measurement on input data Bits	I_{IH}_DECN	V_{CCA5} = 5.2V V_{CCA3} = 3.3V V_{CCD} = 2.5V	01	1, 2, 3	20	150	µA
	I_{IH}_TM0				20	150	
	I_{IH}_TM1				20	150	
	I_{IH}_SDAEN				20	150	
	I_{IH}_RS0				20	150	
	I_{IH}_RS1				20	150	
	I_{IH}_GA				50	200	
	I_{IH}_OA				100	300	
	I_{IH}_SDA				20	200	
	I_{IH}_SA				-150	150	
	I_{IH}_RESET				-150	150	
	I_{IL}_DECN				-700	450	
	I_{IL}_TM0				-700	450	
	I_{IL}_TM1				-700	450	
	I_{IL}_SDAEN				-700	450	
	I_{IL}_RS0				-700	450	
	I_{IL}_RS1				-700	450	
	I_{IL}_GA				-200	200	
	I_{IL}_OA				-400	200	
	I_{IL}_SDA				-150	200	
	I_{IL}_SA				-150	50	
	I_{IL}_RESET				-150	50	
Power supply current with nominal power supply (1:1 MUX)	I_{VCCA5_D1V1}	V_{CCA5} = 5.2V V_{CCA3} = 3.3V V_{CCD} = 2.5V	01	1, 2, 3	50	85	mA
	I_{VCCA3_D1V1}			1, 2, 3	200	330	mA
	I_{VCCD_D1V1}			1, 2, 3	50	110	mA
Power dissipation with nominal power supply (1:1 MUX)	P_{D_D1V1}			1, 2, 3	1300	1900	mW

See footnote end of the table

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions 1/ -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Power supply current with nominal power supply (1:2 MUX)	I_{VCCA5_D1V2}	V_{CCA5} = 5.2V V_{CCA3} = 3.3V V_{CCD} = 2.5V	01	1, 2, 3	50	85	mA
	I_{VCCA3_D1V2}			1, 2, 3	200	335	mA
	I_{VCCD_D1V2}			1, 2, 3	50	160	mA
Power dissipation with nominal power supply (1:2 MUX)	P_{D_D1V2}			1, 2, 3	1300	2000	mW
Power supply current with nominal power supply (1:4 MUX)	I_{VCCA5_D1V4}	V_{CCA5} = 5.2V V_{CCA3} = 3.3V V_{CCD} = 2.5V	01	1, 2, 3	50	85	mA
	I_{VCCA3_D1V4}			1, 2, 3	200	335	mA
	I_{VCCD_D1V4}			1, 2, 3	50	240	mA
Power dissipation with nominal power supply (1:4 MUX)	P_{D_D1V4}			1, 2, 3	1300	2300	mW
Low levels on output pins	V_{OL}_A0, ,A9, B0, B9, C0, C9,D0 D9		01	1, 2, 3	800	1275	mV
Low levels on complemented output pins	V_{OL}_A0N, A9N, B0N, B9N, C0N,C9N,D0N D9N		01	1, 2, 3	800	1275	mV
Low levels on Data ready output pins	V_{OL}_DR,DRN		01	1, 2, 3	800	1275	mV
High levels on output pins	V_{OH}_A0, ,A9, B0, B9, C0, C9,D0 D9		01	1, 2, 3	1225	1700	mV
High levels on complemented output pins	V_{OH}_A0N, A9N, B0N, B9N, C0N,C9N,D0N D9N		01	1, 2, 3	1225	1700	mV
High levels on Data ready output pins	V_{OH}_DR,DRN		01	1, 2, 3	1225	1700	mV
Swing on output pins	SWING_A0,,A9, B0, B9,C0,,C9,D0…D9		01	1, 2, 3	180	430	mV
Swing on complemented output pins	SWING_A0N, ,A9N, B0N, B9N, C0N, ,C9N,D0ND9N		01	1, 2, 3	180	430	mV
Swing on Data ready output pins	SWING_DR, DRN		01	1, 2, 3	180	430	mV

See footnote end of the table

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions 1/ -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Common Mode on output pins	CM_A0, A9, B0, B9, C0, C9,D0 D9		01	1, 2, 3	1125	1375	mV
Common Mode on complemented output pins	CM_A0N, A9N, B0N, B9N, C0N, C9N,D0N, D9N		01	1, 2, 3	1125	1375	mV
Common Mode on Data ready output pins	CM_DR, DRN		01	1, 2, 3	1125	1375	mV
Lvds Low levels on output pins	VOL_lvds_A0, A9, B0, B9, C0, C9,D0…D9		01	1, 2, 3	800	1275	mV
Lvds Low levels on complemented output pins	VOL_lvds_A0N, A9N, B0N, B9N, C0N, C9N, D0N…D9N		01	1, 2, 3	800	1275	mV
Lvds Low levels on Data ready output pins	VOL_DR_lvds, DRN_lvds		01	1, 2, 3	800	1275	mV
Lvds High levels on output pins	VOH_lvds_A0,…,A9, B0, B9,…C0,,C9,D0…D9		01	1, 2, 3	1225	1600	mV
Lvds High levels on complemented output pins	VOH_lvds_A0N, A9N, B0N, B9N, C0N,,C9N,D0N, D9N		01	1, 2, 3	1225	1600	mV
Lvds High levels on Data ready output pins	VOH_DR_llvds, DRN_llvds		01	1, 2, 3	1225	1600	mV
Lvds Swing on output pins	SWING_lvds_A0,…,A9, B0,…, B9,…C0,…,C9,D0…D9		01	1, 2, 3	49	450	mV
Lvds Swing on complemented output pins	SWING _lvds_A0N, A9N, B0N, B9N, C0N, ,C9N, D0N…D9N		01	1, 2, 3	49	450	mV
Lvds Swing on Data ready output pins	SWING_lvds _DR, DRN		01	1, 2, 3	49	450	mV
Lvds Common Mode on output pins	CM_lvds _ A0,…,A9, B0, B9,…C0,…,C9,D0…D9		01	1, 2, 3	1125	1375	mV
Lvds Common Mode on complemented output pins	CM_lvds_A0N, A9N, B0N, B9N, C0N, C9N, D0N…D9N		01	1, 2, 3	1125	1375	mV
Lvds Common Mode on Data ready output pins	CM_ lvds_DR, DRN		01	1, 2, 3	1125	1375	mV

See footnote end of the table

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions 1/ -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Dynamic performance at Fc= 1.5Gsps / Fin = 750MHz Input level -3dBFs/ Typical power supplies	A_ENOBFS_M3dBFS		01	4, 5, 6	7.4		bits
	A_SNR_M3dBFS				50		dBFS
	A_THD_M3dBFS				48		dBFS
	A_SFDR_M3dBFS				50		dBFS
Dynamic performance at Fc= 1.5Gsps / Fin = 750MHz Input level : -12dBFs/ Typical power supplies	A_ENOBFS_M12dBFS		01	4, 5, 6	7.8		bits
	A_SNR_M12dBFS				52		dBFS
	A_THD_M12dBFS				49		dBFS
	A_SFDR_M12dBFS				52		dBFS
Dynamic performance at Fc= 1.5Gsps / Fin = 1800MHz Input level -3dBFs/ Typical power supplies	A_ENOBFS_M3dBFS		01	4, 5, 6	7.2		bits
	A_SNR_M3dBFS				49		dBFS
	A_THD_M3dBFS				47		dBFS
	A_SFDR_M3dBFS				50		dBFS
Dynamic performance at Fc= 1.5Gsps / Fin = 1800MHz Input level -12dBFs/ Typical power supplies	A_ENOBFS_M12dBFS		01	4, 5, 6	7.8		bits
	A_SNR_M12dBFS				52		dBFS
	A_THD_M12dBFS				49		dBFS
	A_SFDR_M12dBFS				52		dBFS

See footnote end of the table

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions 1/ -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Output offset adjustment	Offset_Voie		01	7, 8A, 8B	472	552	LSB
	CorMaxVoie				20	60	LSB
	OffCorMaxVoie				513	573	LSB
	CorMinVoie				-60	-20	LSB
	OffCorMinVoie				451	511	LSB
Gain measurement	FullScale_gain min_M3DBFS		01	7, 8A, 8B		1	dBFS
	FullScale gain_nom				0.9	1.1	dBFS
	FullScale_gain max_M3DBFS				1		dBFS
	Correction_gain% min_M3DBFS				-13	-6	%
	Correction_gain_% _max_M3DBFS				6	13	%
SDA functionality check	SDA_on_Amplitude		01	7, 8A, 8B	680	770	LSB
	SDA_on_Cod_Mil				480	565	LSB
	SDA_Cor_sda_min				-70	-30	LSB
	SDA_Cor_sda_max				30	70	LSB
Switching performance and characteristics							
Maximum clock frequency	1:1 DEMUX ratio		01	9, 10, 11		700	MHz
	1:2 DEMUX ratio					1500	MHz
	1:4 DEMUX ratio					1500	MHz
Maximum data output rate per port	1:1 DEMUX ratio		01	9, 10, 11		700	Msps
	1:2 DEMUX ratio					750	Msps
	1:4 DEMUX ratio					375	Msps
ADC setting time (Vin-Vinn=400mVpp)	TS		01	9, 10, 11	770 typical		ps
ADC step response			01	9, 10, 11	16 typical		ps
Clock duty cycle			01	9, 10, 11	40	60	%

See footnote end of the table

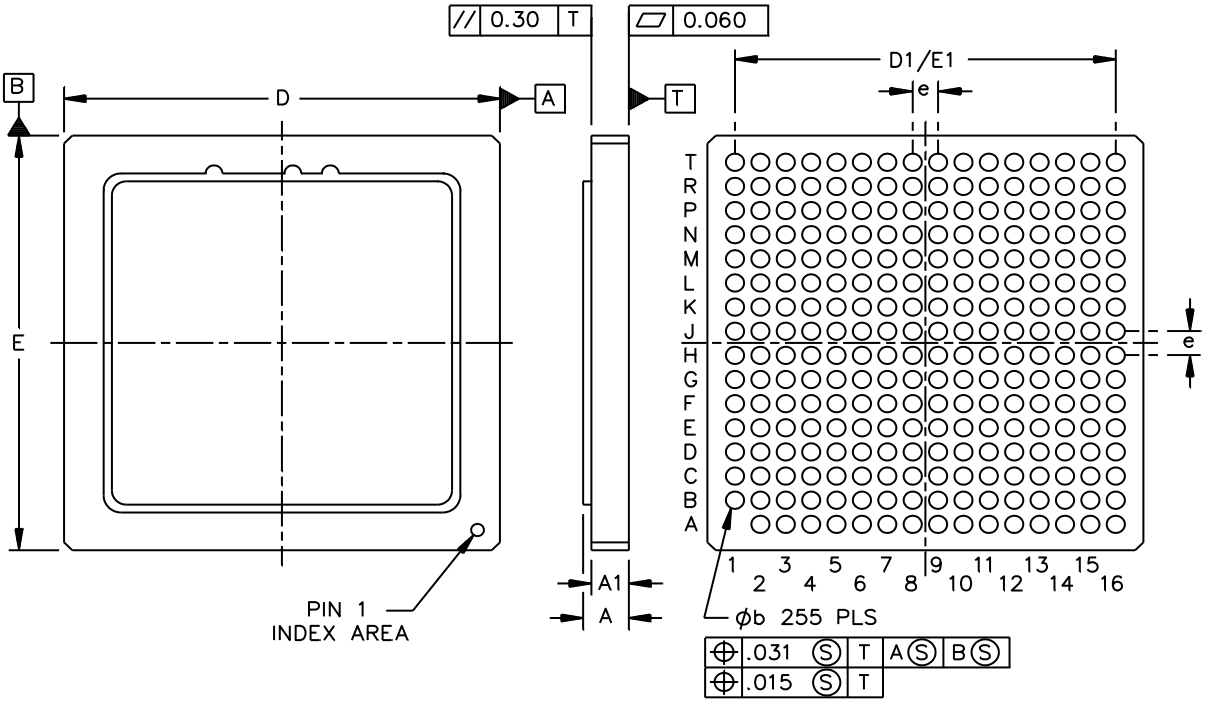
TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions 1/ -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Minimum clock pulse width (high)	TC1		01	9, 10, 11	0.25	0.375	ns
Minimum clock pulse width (low)	TC2		01	9, 10, 11	0.25	0.375	ns
Output rise/fall time for data	t_R/t_F		01	9, 10, 11	320	480	ps
Output rise/fall time for data ready	t_R/t_F		01	9, 10, 11	510	890	ps
Output DATA to DATA ready propagation delay	TD1	1:1 DEMUX 750MSps sampling rate	01	9, 10, 11	1.08	1.20	ns
	TD1	1:2 DEMUX 1.5GSps sampling rate			0.84	1.10	ns
	TD1	1:4 DEMUX 1.5GSps sampling rate			1.45	1.55	ns
DATA ready to DATA output propagation delay	TD2	1:1 DEMUX 750MSps sampling rate	01	9, 10, 11	0.16	0.24	ns
	TD2	1:2 DEMUX 1.5GSps sampling rate			0.31	0.49	ns
	TD2	1:4 DEMUX 1.5GSps sampling rate			1.1	1.25	ns

1/. Group A, subgroup 3, 6, 8B, 11 tests are guaranteed for Tc = -55°C.

Case outline. “X”

LGA255 top, bottom & side view (Seal ring connected to AGND)



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	2.01	2.45	D1/E1	19.05 TYP	
A1	1.62	1.98	e	1.27 TYP	
b	0.76	0.96			
D/E	20.8	21.2			

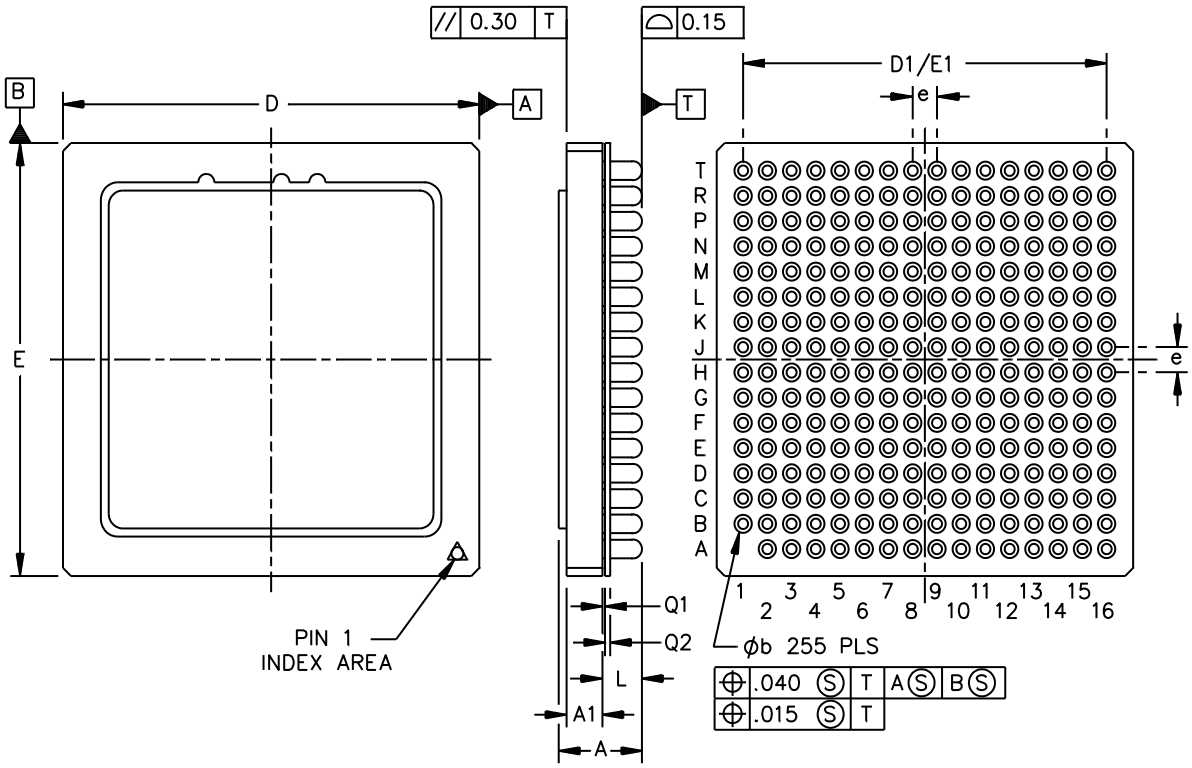
Notes:

1. Metal lid 0.38mm thickness + 0.5mm solder with 16.38mm SQ lid. Finish Au plated over nickel.
2. All exposes metal must be plated electroless nickel thickness 1.27~8.99 micron and Au plated 1.50 micron minimum.

FIGURE 1.a - Case outline “X”

Case outline. “Y”

Ci-CGA255 top, bottom & side view (seal ring connected to AGND)



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	4.02	4.58	D1/E1	19.05 TYP	
A1	1.65	1.95	e	1.27 TYP	
b	0.79	0.99	L	1.62 TYP	
D/E	20.8	21.2			

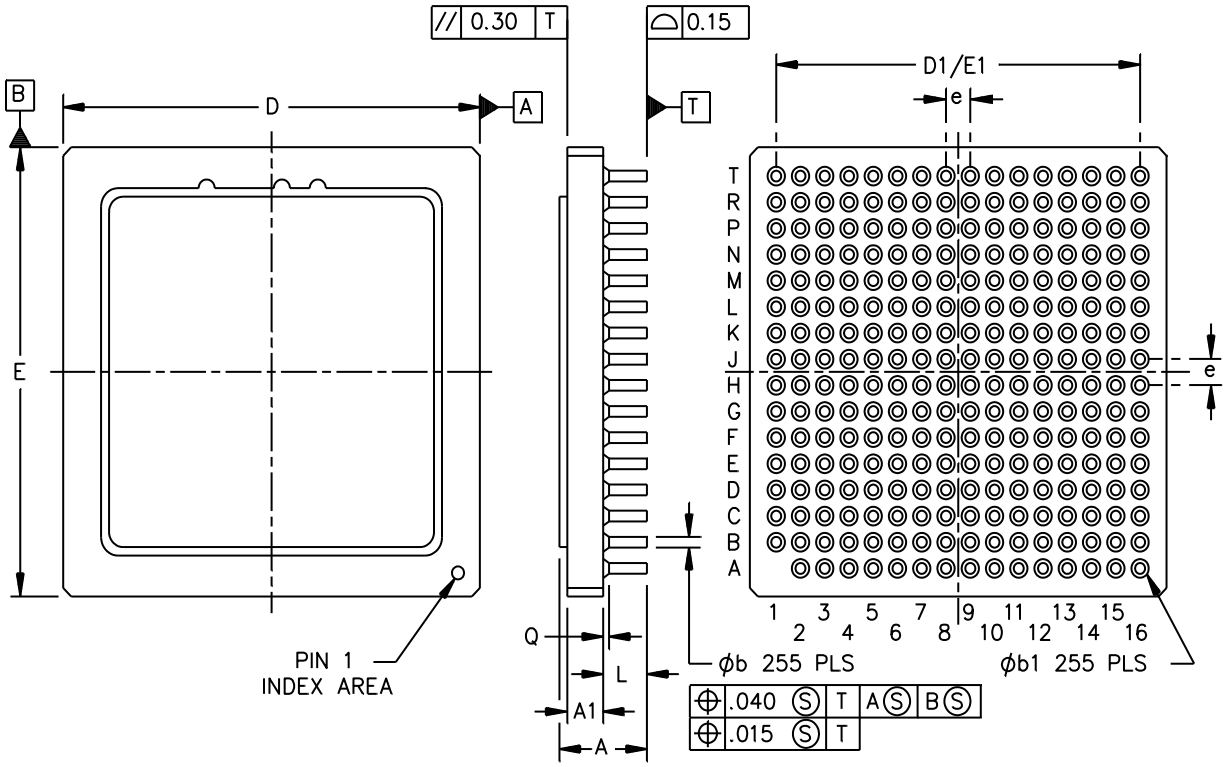
Notes:

1. Triangle patterned on top A1 corner 550 µm side width triangle. Chamfer 0.4 all 4side. No column on A1 corner
2. All exposes metal must be plated electroless nickel thickness 1.27~8.99 micron and Au plated 1.50 micron minimum. Assembly of SCI on LGA using 63/37 tin/lead solder bump. Column alloy composition of 90/10 lead/tin.

FIGURE 1.b Case outline “Y”

Case outline "Z"

CCGA255 top, bottom & side view (seal ring connected to AGND)



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	4.05	4.81	D1/E1	19.05 TYP	
A1	1.62	1.98	e	1.27 TYP	
b	0.41	0.61	L	2.00	2.40
D/E	20.8	21.2			

Notes:

1. Circle dot patterned on top A1 corner 570 µm diameter. Chamfer 0.4 all 4side. No column on A1 corner.
2. All exposes metal must be plated electroless nickel thickness 1.27~8.99 micron and Au plated 1.50 micron minimum. Assembly of columns on LGA using 63/37 tin/lead solder. Column alloy composition of tin (Sn) 20% and lead(Pb) 80% with copper spiral.

FIGURE 1.c Case outline "Z"

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		VCCO	NC (DGND)	B4	B5	B7	B8	NC (DGND)	**DR**	C8	C7	C5	C4	NC (DGND)	VCCO	DGND	A
B	DGND	VCCO	NC (DGND)	B4N	B5N	B7N	B8N	NC (DGND)	**DRN**	C8N	C7N	C5N	C4N	NC (DGND)	VCCO	DGND	B
C	NC (DGND)	NC (DGND)	VCCO	DGND	B6N	B6	B9	B9N	C9N	C9	C6	C6N	DGND	VCCO	NC (DGND)	NC (DGND)	C
D	B3	B3N	DGND	VCCO	VCCO	DGND	DGND	DGND	DGND	DGND	DGND	VCCO	VCCO	DGND	C3N	C3	D
E	B2	B2N	B1	DGND	DGND	DGND	VCCO	VCCO	VCCO	VCCO	DGND	DGND	DGND	C1	C2N	C2	E
F	B0	B0N	B1N	DGND	VCCO	DGND	DGND	VCCO	VCCO	DGND	DGND	VCCO	DGND	C1N	C0N	C0	F
G	NC (DGND)	NC (DGND)	A9N	DGND	VCCO	VCCO	AGND	AGND	AGND	AGND	VCCO	VCCO	DGND	D9N	NC (DGND)	NC (DGND)	G
H	A8	A8N	A9	DGND	DGND	VCCO	AGND	AGND	AGND	AGND	VCCO	DGND	DGND	D9	D8N	D8	H
J	A7	A7N	A6N	DGND	DGND	VCC3	AGND	AGND	AGND	AGND	VCC3	DGND	DGND	D6N	D7N	D7	J
K	A5	A5N	A6	VCC3	VCC3	VCC3	AGND	AGND	AGND	AGND	VCC3	VCC3	VCC3	D6	D5N	D5	K
L	A4	A4N	A3	DGND	DGND	DGND	VCC5	VCC5	VCC5	VCC5	DGND	DGND	DGND	D3	D4N	D4	L
M	A2	A2N	A3N	DGND	DGND	NC (DGND)	AGND	VCC5	AGND	VCC5	NC (DGND)	NC (DGND)	DGND	D3N	D2N	D2	M
N	A1	A1N	DIODE C	OA	DGND	NC (DGND)	AGND	VCC5	AGND	VCC5	DGND	DGND	DGND	DECN	D1N	D1	N
P	A0	A0N	DIODE A	GA	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	SA	D0N	D0	P
R	DGND	DGND	DGND	NC (DGND)	NC (DGND)	**CLKN**	AGND	AGND	AGND	AGND	AGND	SDAEN	RS1	TM1	DGND	DGND	R
T	DGND	DGND	DGND	RSTN	NC (DGND)	**CLK**	AGND	AGND	**VIN**	**VINN**	AGND	SDA	RS0	TM0	DGND	DGND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

FIGURE 2.1. Terminal connections.

Pinout Table CLGA255

Signal Name	Pin number	Description	Direction	Equivalent Simplified Schematics
POWER SUPPLIES				
VCC5	L7, L8, L9, L10, M8, M10, N8, N10	5.2V analog supply (Front-end Track & Hold circuitry) Referenced to AGND	N/A	
VCC3	J6, J11, K4, K5, K6, K11, K12, K13	3.3V power supply (ADC Core, Regeneration and Logic, DEMUX circuitry and Timing circuitry) Referenced to AGND	N/A	
VCCO	A2, A15, B2, B15, C3, C14, D4, D5, D12, D13, E7, E8, E9, E10, F5, F8, F9, F12, G5, G6, G11, G12, H6, H11	2.5V digital power supply (output buffers) Referenced to DGND	N/A	
AGND	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M7, M9, N7, N9, P6, P7, P8, P9, P10, P11, R7, R8, R9, R10, R11, T7, T8, T11	Analog Ground AGND plane should be separated from DGND on the board (the two planes can be connected by 0 ohm resistors)	N/A	
DGND	A16, B1, B16, C4, C13, D3, D6, D7, D8, D9, D10, D11, D14, E4, E5, E6, E11, E12, E13, F4, F6, F7, F10, F11, F13, G4, G13, H4, H5, H12, H13, J4, J5, J12, J13, L4, L5, L6, L11, L12, L13, M4, M5, M13, N5, N11, N12, N13, P5, P12, P13, R1, R2, R3, R15, R16, T1, T2, T3, T15, T16	Ground for output buffers DGND plane should be separated from AGND on the board (the two planes can be connected by 0 ohm resistors)	N/A	

FIGURE 2.2. Pin out table.

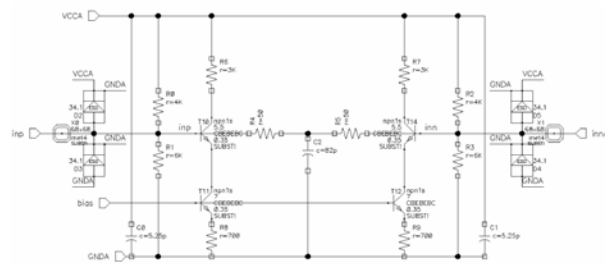
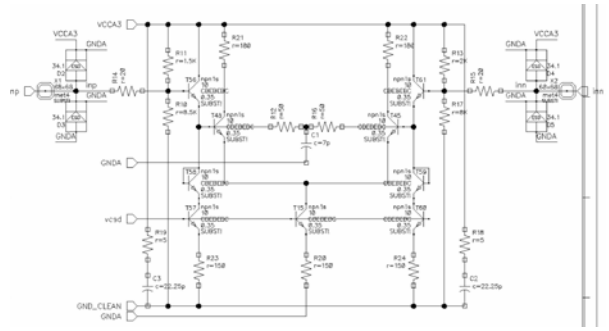
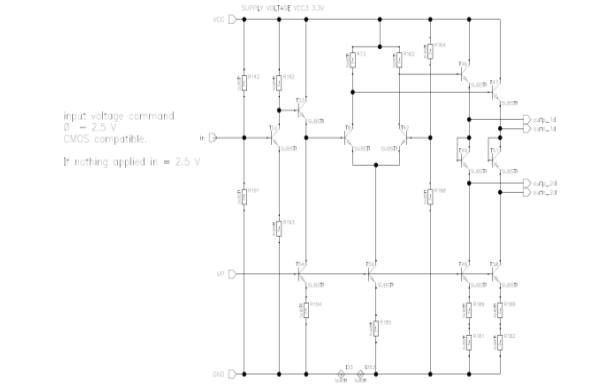
ANALOG INPUTS				
VIN VINN	T9 T10	Analog input (differential) with internal common mode at 3.1V It should be driven in AC coupling. Analog input is sampled and converted (10-bit) on each positive transition of the CLK input. Equivalent internal differential 100 Ω input resistor.	I	
CLOCK INPUTS				
CLK CLKN	T6 R6	Master sampling clock input (differential) with internal common mode at 2.65V It should be driven in AC coupling. Equivalent internal differential 100 Ω input resistor.	I	
RSTN	T4	Reset input (single-ended)	I	

FIGURE 2.2. Pin out table. - Continued.

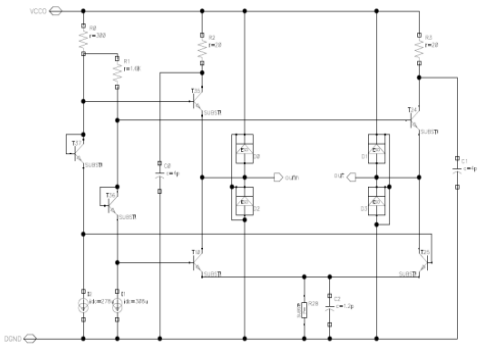
DIGITAL OUTPUTS				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N	P1, P2 N1, N2 M1, M2 L3, M3 L1, L2 K1, K2 K3, J3 J1, J2 H1, H2 H3, G3	In-phase (Ai) and inverted phase (AiN) digital outputs on DEMUX Port A (with i = 0…9) Differential LVDS signal DA0 is the LSB, DA9 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100 Ω differential resistor placed as close as possible to the differential receiver.	O	

FIGURE 2.2. Pin out table. - Continued.

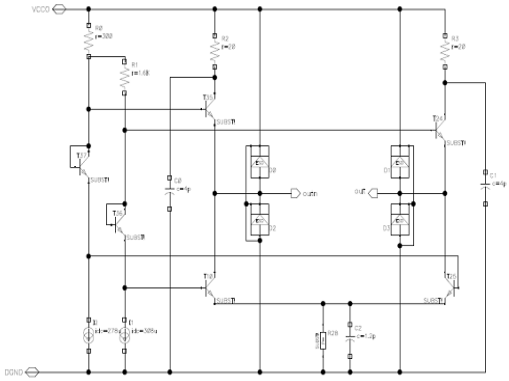
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N	F1, F2 E3, F3 E1, E2 D1, D2 A4, B4 A5, B5 C6, C5 A6, B6 A7, B7 C7, C8	In-phase (ABi) and inverted phase (BiN) digital outputs on DEMUX Port B (with i = 0…9) Differential LVDS signal B0 is the LSB, B9 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100 Ω differential resistor placed as close as possible to the differential receiver.	O	

FIGURE 2.2. Pin out table. - Continued.

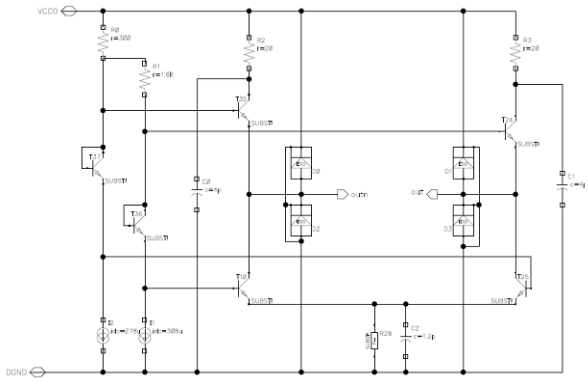
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N	F16, F15 E14, F14 E16, E15 D16, D15 A13, B13 A12, B12 C11, C12 A11, B11 A10, B10 C10, C9	In-phase (Ci) and inverted phase (CiN) digital outputs on DEMUX Port C (with i = 0…9) Differential LVDS signal C0 is the LSB, C9 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100 Ω differential resistor placed as close as possible to the differential receiver.	O	

FIGURE 2.2. Pin out table. - Continued.

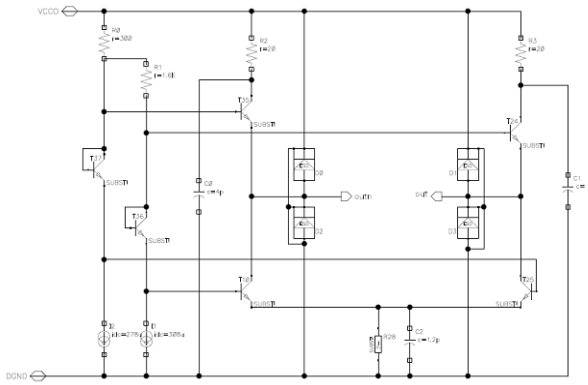
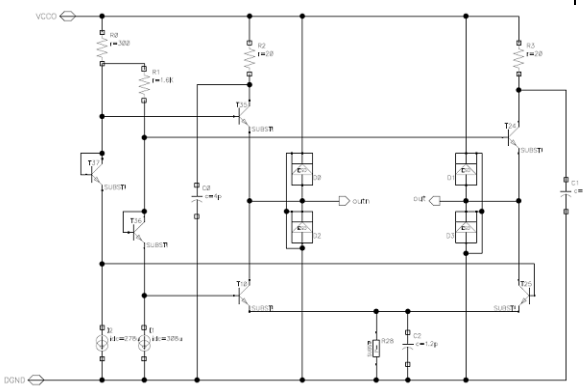
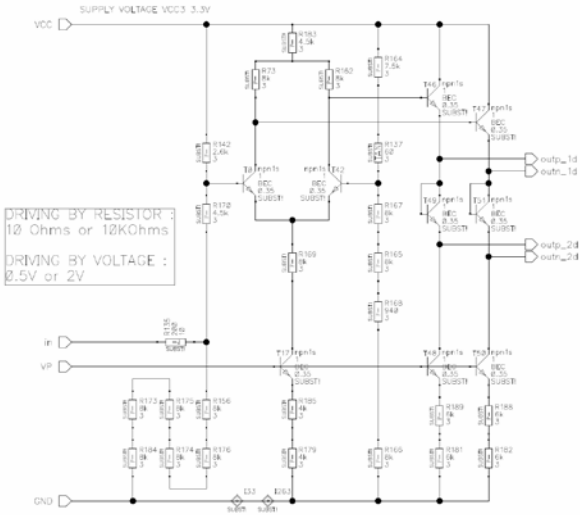
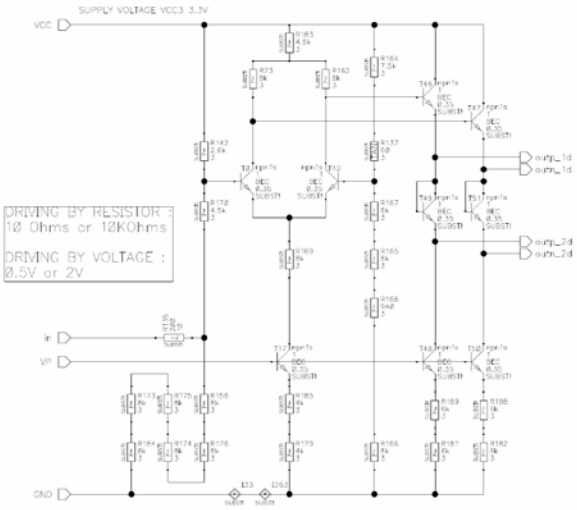
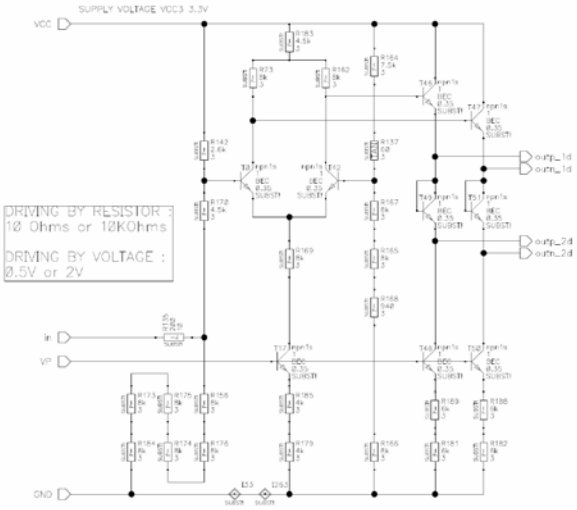
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N	P16, P15 N16, N15 M16, M15 L14, M14 L16, L15 K16, K15 K14, J14 J16, J15 H16, H15 H14, G14	In-phase (Di) and inverted phase (DiN) digital outputs on DEMUX Port D (with i = 0…9) Differential LVDS signal D0 is the LSB, D9 is the MSB The differential digital output data is transmitted at clock rate divide by DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by 100 Ω differential resistor placed as close as possible to the differential receiver.	O	

FIGURE 2.2. Pin out table. - Continued.

DR DRN	A9 B9	In-phase (DR) and inverted phase (DRN) global data ready digital output clock Differential LVDS signal The differential digital output clock is used to latch the output data on rising and falling edge. The differential digital output clock rate is (CLK/2) divided by the DMUX ratio (provided by RS0 and RS1 pins). This differential digital output clock should be terminated by 100 Ω differential resistor placed as close as possible to the differential receiver.	O	
ADDITIONAL FUNCTIONS				
DECN	N14	Decimation Function Enable (single-ended)	I	

TM0, TM1	T14, R14	Test Mode	I	
RS0, RS1	T13, R13	DEMUX Ratio Selection	I	
SDAEN	R12	SDAEN = Sampling delay adjust enable *SDA = Sampling delay adjust*	I	

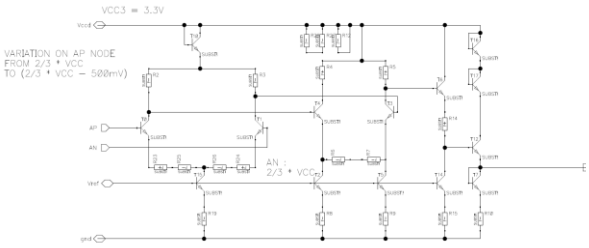
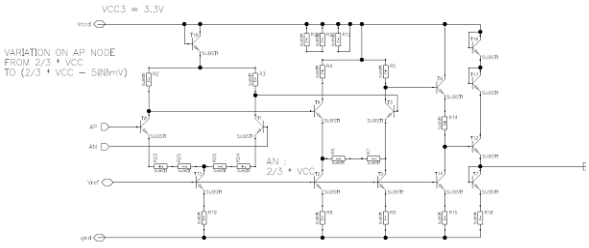
SDA	T12		I	
GA	P4	Gain Adjust	I	
OA	N4	Offset Adjust	I	
SA	P14	Swing adjust	I	
DIODEA	P3	Die Junction temperature monitoring (DIODEA = anode, DIODEC = cathode)	I	
DIODEC	N3		O	
NC	A3, A8, A14 B3, B8, B14 C1, C2, C15, C16 G1, G2, G15, G16 M6, M11, M12 N6 R4, R5, T5	Not connected pins, connect to ground (DGND)	N/A	

FIGURE 2.2. Pin out table. - Continued.

Functional Description

Name	Function
V_{CC5}	5.2V Power supply
V_{CC3}	3.3V Power supply
V_{CC0}	2.5V Power supply
AGND	Analog Ground
DGND	Digital Ground
VIN,VINN	Differential Analog Input
CLK,CLKN	Differential Clock Input
[A0:A9] [A0N:A9N]	Differential Output Data on port A
[B0:B9] [B0N:B9N]	Differential Output Data on port B
[C0:C9] [C0N:C9N]	Differential Output Data on port C
[D0:D9] [D0N:D9N]	Differential Output Data on port D
DR,DRN	Global Differential Data Ready
SA	Analog tuning to adjust output swing
RS0; RS1	DEMUX Ratio select
RSTN	External reset
TM0, TM1	Test Mode pins
SDA	Sampling Delay Adjust input
SDAEN	Sampling Delay Adjust Enable
GA	Gain Adjust input.
OA	Offset adjust input
DECN	Decimation enable
DIODEA, DIODEC	Diode for die junction temperature monitoring

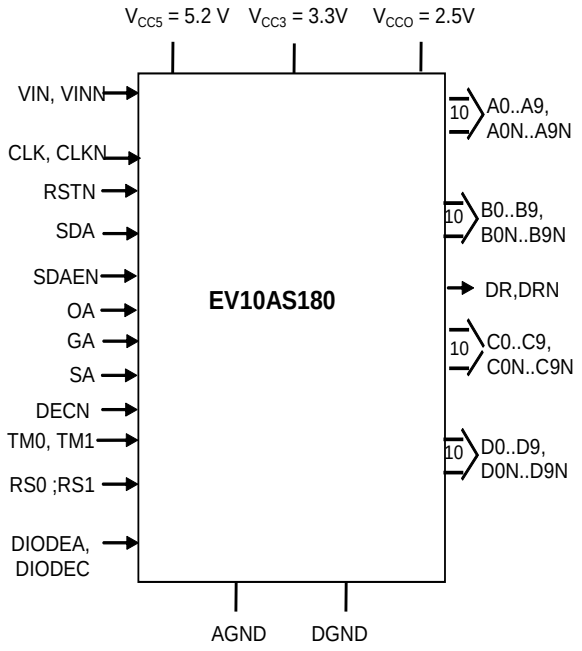
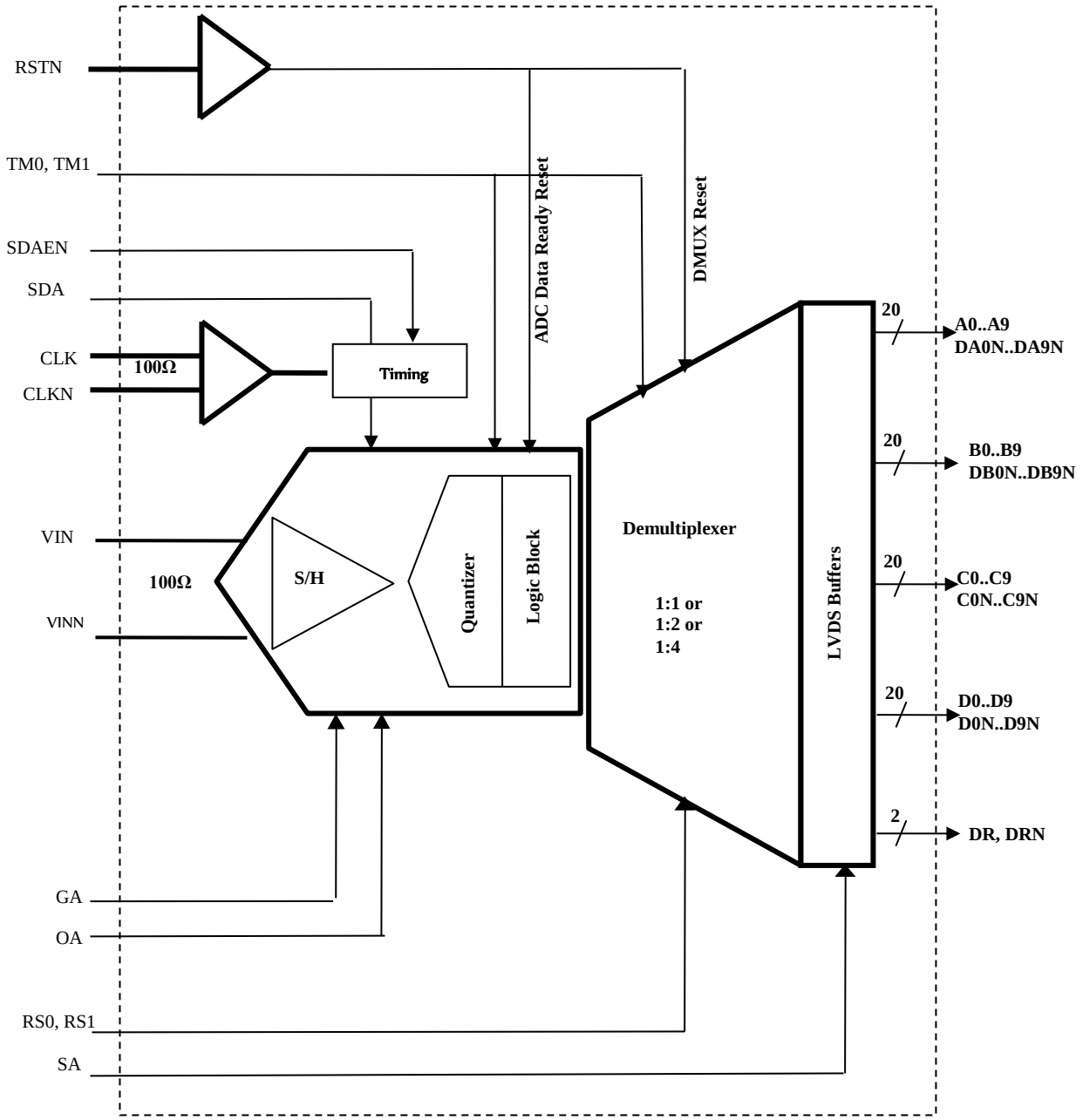


FIGURE 2.3. Functional diagram

Differential analog input	Voltage level	Digital output
		Binary MSB (bit 9)…….....LSB (bit 0)
> + 250.25 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1
+ 250.25 mV + 249.75 mV	Top end of full scale + ½ LSB Top end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
+ 125.25 mV + 124.75 mV	$^{3}/_{4}$ full scale + ½ LSB $^{3}/_{4}$ full scale - ½ LSB	1 1 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1
+ 0.25 mV - 0.25 mV	Mid scale + ½ LSB Mid scale - ½ LSB	1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1
- 124.75 mV - 124.25 mV	$^{1}/_{4}$ full scale + ½ LSB $^{1}/_{4}$ full scale - ½ LSB	0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
- 249.75 mV - 250.25 mV	Bottom end of full scale + ½ LSB Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
< - 250.25 mV	< Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0

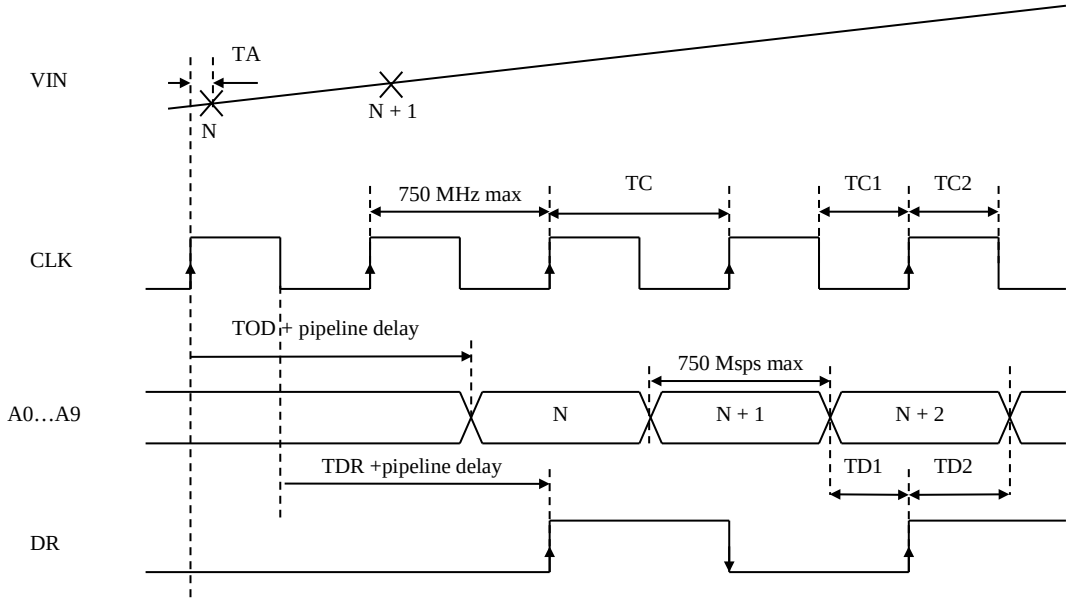
FIGURE 3. Truth table.



NOTES: The EV10AS180A is a 10-bit 1.5Gsps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100Ω differential output buffers.
The EV10AS180A works in fully differential mode from analog inputs up to digital outputs. It operates in the first Nyquist and L-Band (Fin ranging from DC to 1800 MHz). DEMUX Ratio (1:1 or 1:2 or 1:4) can be selected with the 2 pins RS0, RS1.
DEMUX outputs are synchronous on each port. A differential Data Ready output is available to indicate when the outputs are valid. The Data Ready DR, DRN is common to the 4 ports. A power up reset ensures to synchronize internal signals and ensures output data to be properly ordered. An external Reset (RSTN) can also be used.

FIGURE 4. Block diagram.

5.1. Timing Diagram for 1:1 DEMUX principle of operation



5.2. Timing Diagram for 1:2 DEMUX principle of operation

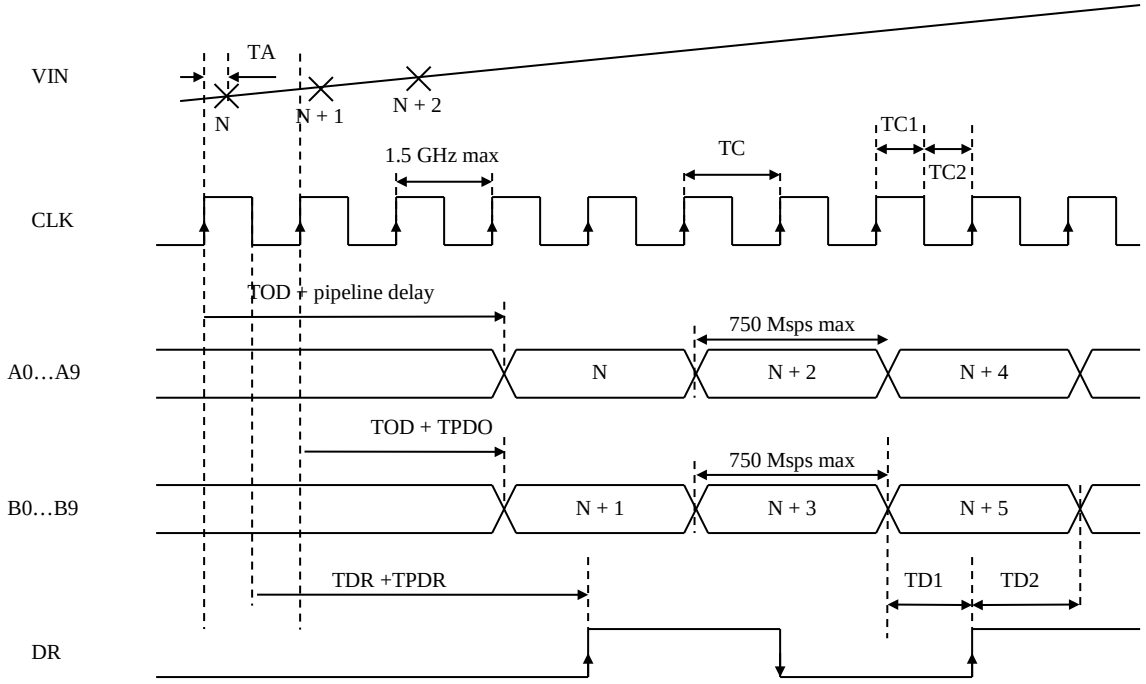


FIGURE 5. Timing waveforms.

5.3. Timing Diagram for 1:4 DEMUX principle of operation

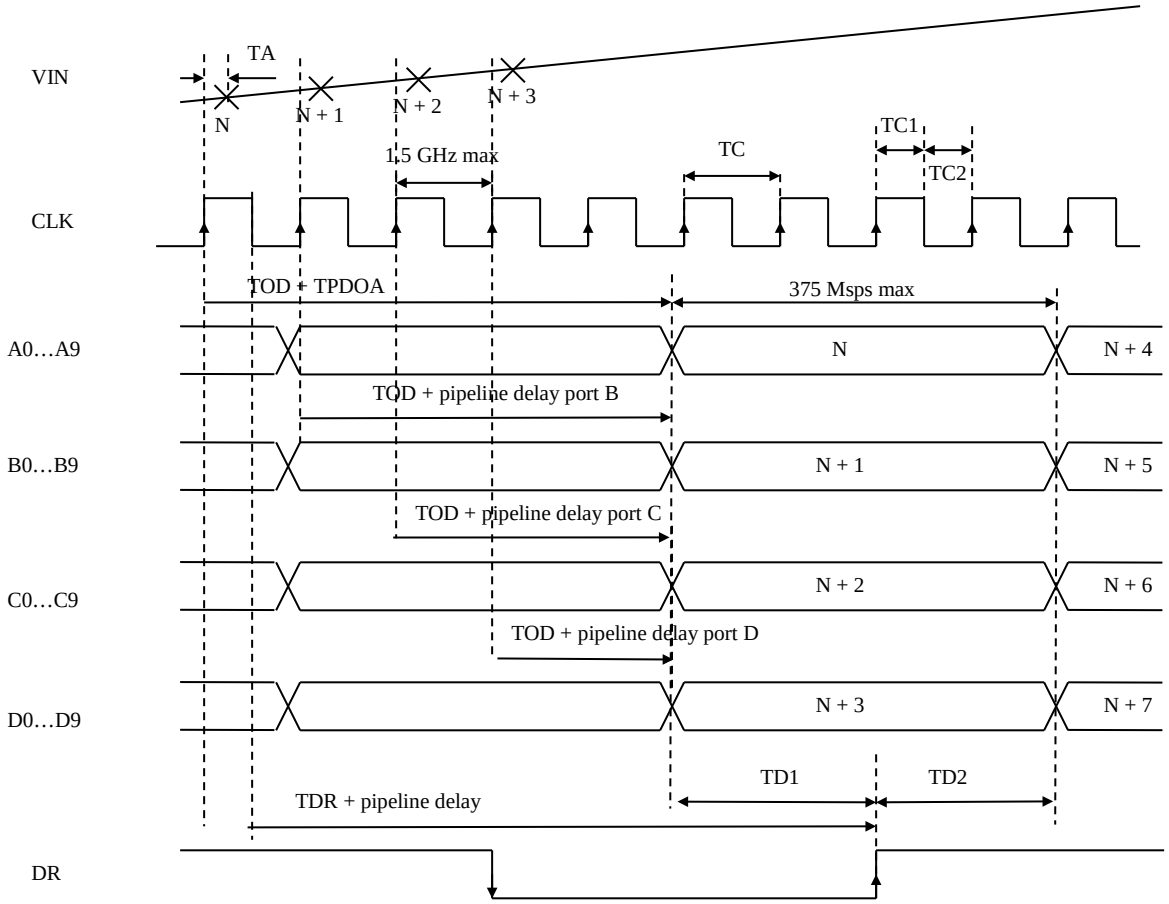
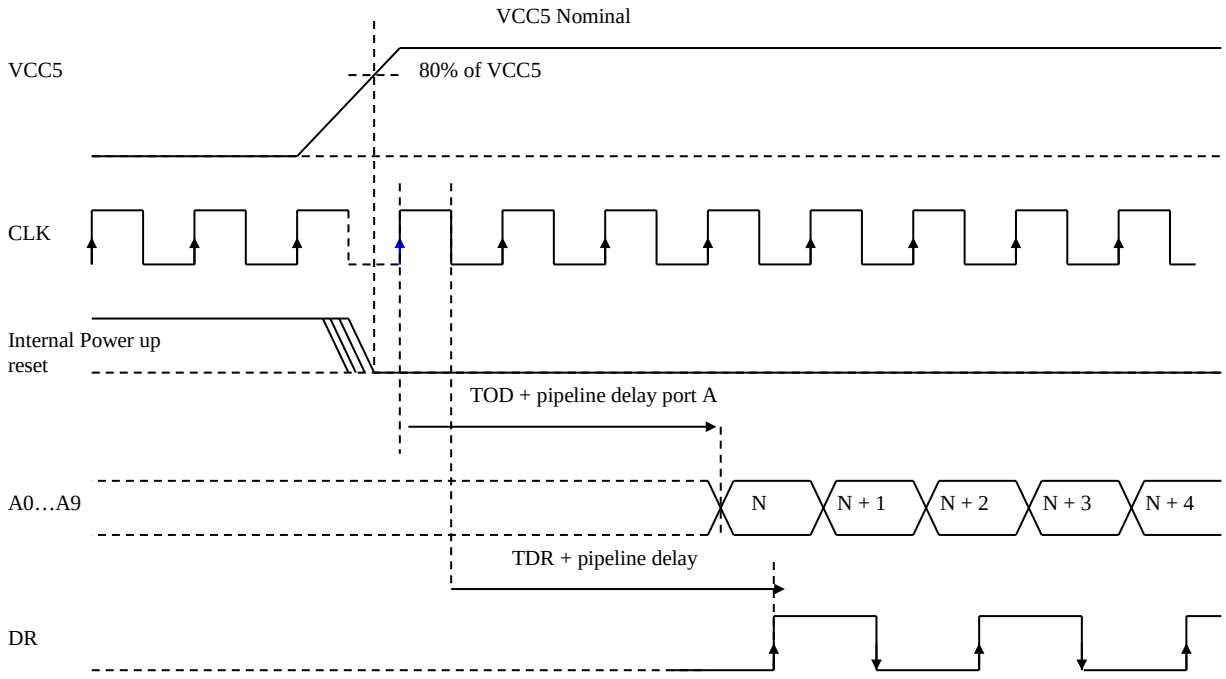


FIGURE 5. Timing waveforms- Continued.

5.4 Power up reset timing diagram 1:1DEMUX



Note : Assuming VCC3 is already switched on.

5.5 External RESET timing diagram 1:1DEMUX

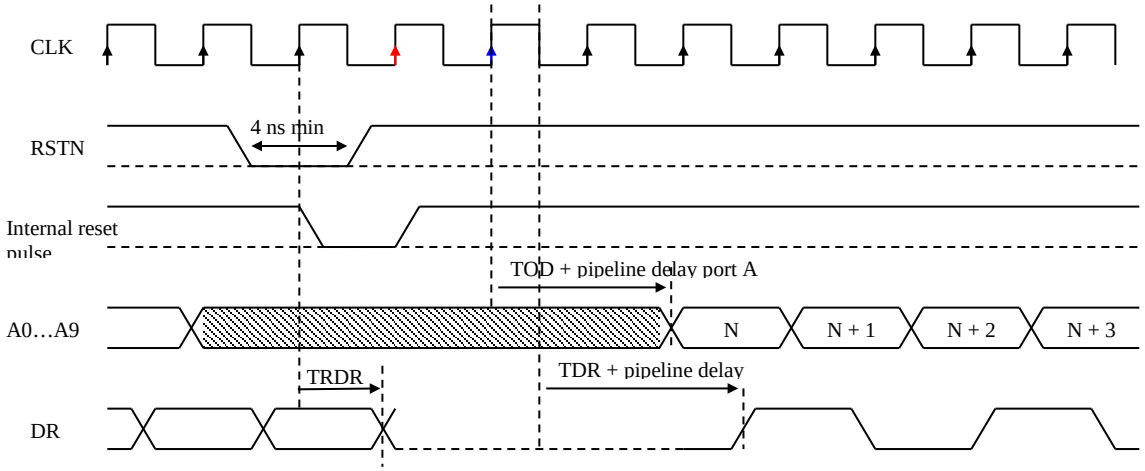
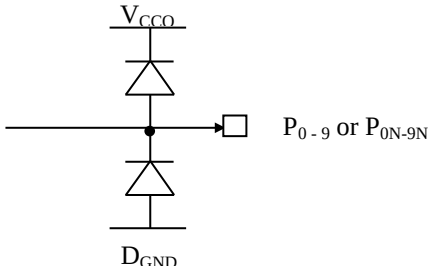
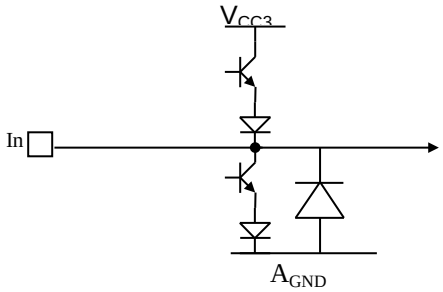


FIGURE 5. Timing waveforms- Continued.

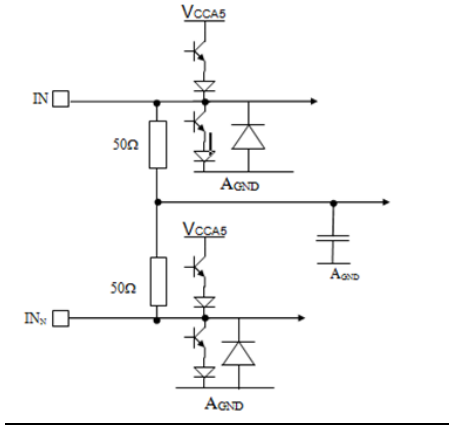
Digital LVDS output ESD protections (P0…P9N) Port P – Port A, B, C, D, DR, DRN



Control input buffer ESD protections (SA, SDA, OA, GA, SDAEN, TM0, TM1, DECN, RS0, RS1, RSTN)



Analog input ESD protections (V_{IN}, V_{INN} and CLK,CLKN)



Power supplies ESD protections

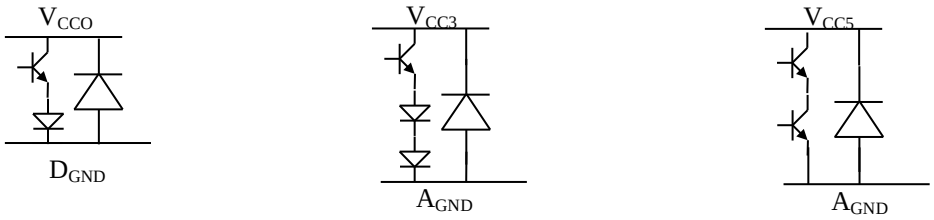


FIGURE 6. Input and output protection networks

Thermal Characteristics

Typical Assumptions

- Die thickness = 300 µm
- No convection
- Pure conduction
- No radiation

R_{TH}	Heating zone	Ci CGA	CCGA	Unit
Junction-> Bottom of columns	18% die area : 4820x4820 µm	10.5	11.7	°C/W
Junction-> Board (JEDEC JESD51-8) Boad size = 39x39mm, 1.6 mm Thickness)		13.7	15.2	°C/W
Junction -> Top of Lid		16.0	18.4	°C/W
$T_{jhot\ spot} - T_{Jdiode}$		2.2	2.2	°C/W

Typical Assumptions:

- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
- Board size 114.3 × 76.2 mm, 1.6 mm thickness

R_{TH}	Heating zone	Ci CGA	CCGA	Unit
Junction -> Ambient	18% die area : 4820x4820 µm	26.0	26.0	°C/W
$T_{jhot\ spot} - T_{Jdiode}$		2.2	2.2	°C/W

FIGURE 7. Die Thermal Characteristics

4. VERIFICATION

4.1 Sampling and inspection. For device class V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device class V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.2.2 Deviation/addition from MIL-PRF-38535.

a. “Nondestructive bond pull test” (TM 2023) is replaced by “Destructive bond pull test” (TM 2011) monitoring.

b. “Constant acceleration” (TM 2001) is deleted from screening. Group D4 shall be applied on each assembly lot.

c. “Reverse Bias Burn-in” is not applicable on technology use for EV10AS180A product (200GHz SiGe Bipolar). However,100% Static burn-in shall be performed in accordance with MIL-PRF-38535.

d. Burn-in is performed at T_A=105°C that gives a Tj = ~165°C in LGA packages and estimated case temperature during burn in and HTOL is Tc = T_A burn-in (105°C) + 20°C => Tc = ~125°C

4.3 Qualification inspection for device class V. Qualification inspection for device class V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1, 2, 3, 7, 8A, 8B, 9, 10,1 1 1/	1,2,3,7,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Dynamic burn-in (method 1015)	Required	Required
4	Final electrical parameters	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1,2,3,7,8A,8B,9, 10,11 1/
5	Group A test requirements 3/	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
6	Group C end-point electrical parameters 3/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/	1,2,3,7,8A,8B, 9,10,11 2/
7	Group D end-point electrical parameters 4/	1, 2, 3, 7, 8A, 8B 9,10,11	1, 2, 3, 7, 8A, 8B 9,10,11
8	Group E end-point electrical parameters 3/	-	-
9	Column attach 5/	1, 7, 9	1, 7, 9

1/ Indicates PDA applies to subgroup 1 and 7.
2/ For device class V, performance of delta limits shall be specified in table IIB.
3/ LGA packages only
4/ LGA package for all tests, plus CGA device for Column Pull and Salt Atmosphere.
5/ Solderability test shall be performed in accordance with TM 2003.

Table IIB. Burn-in delta drift limits at +25ºC. 1/ 2/

Test description	**Test Symbol**	**Test limits**		**Units**
		Low	High	
Power supply current	I_{CC5}	-8	+8	%
Power supply current	I_{CC3}	-8	+8	%
Power supply current	I_{CC0}	-8	+8	%
Data output VOH and VOL	VOL	-50	50	mV
	VOH	-50	50	mV
Offset voltage		-5	+5	LSB

1/ These parameters shall be recorded before and after the required burn-in to determine delta limits.
2/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall be as per the corresponding test defined in TABLE I. The drift value shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in Table IIA herein.

a. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM Standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0º ≤ angle ≤ 60º). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon. However, the particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip. Range of the ion which shall be sufficiently penetrate well beyond the deepest part of the sensitive volume of the devices to detect latch-up.

e. The test temperature shall be +25ºC ±10ºC for single event upset testing and at the maximum rated operating temperature ±10ºC for single event upset testing.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device class V Packing is not individual: Devices are packed within trays.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device class V. Sources of supply for device class V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 CGA packages lead finish: Microcircuits devices for column grid array (CGA) packages are supplying to this drawing with terminal lead finish mark “F”. However, terminal lead finish F is tin (Sn) and lead (Pb) alloy with copper spiral column, and solder column material contains compositions of Sn= 20% and Pb=80% and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-09-23

Approved sources of supply for SMD 5962-15223 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1522301VXC	F8385	EV10AS180AMLG-V
5962-1522301VYF	F8385	EV10AS180AMGS-V
5962-1522301VZF	F8385	EV10AS180AMGC-V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8385	e2V Semiconductors Avenue De Rochepleine BP 123 Saint Egreve CEDEX 38521, France.

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.