REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35																			
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

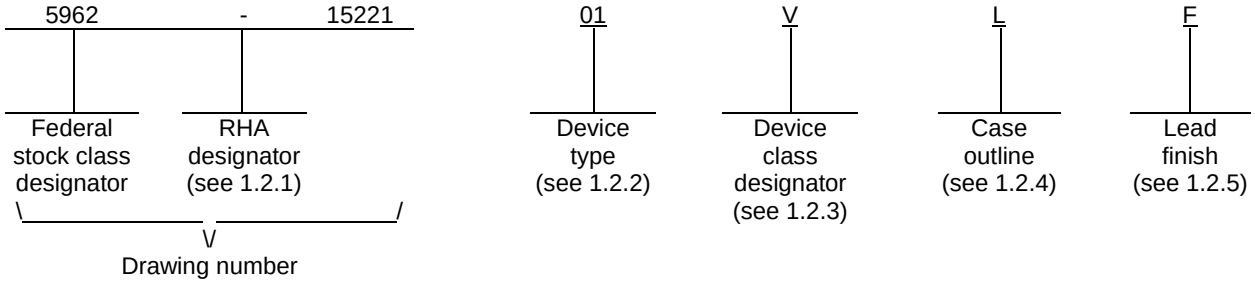
REV STATUS OF SHEETS														
REV														
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Muhammad Akbar	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Muhammad Akbar	
	APPROVED BY Thomas M. Hess	MICROCIRCUIT, SiGe BIPOLAR, LOW POWER 10BIT 3Gsps DIGITAL TO ANALOG CONVERTER WITH 4/2:1 MULTIPLEXER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 15-08-20	
AMSC N/A	REVISION LEVEL	SIZE A / CAGE CODE **67268** / **5962-15221**
		SHEET 1 OF 35

1. SCOPE

1.1 Scope. This drawing documents product assurance class level consisting of space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device class V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	EV10DS130A	10bit 3Gsps 200GHz bipolar Mux DAC

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1.a	255	Ceramic land grid array (CLGA-Au pad termination)
Y	See figure 1.b	255	Ceramic column grid array (CI-CGA-Solder column interposer)
Z	See figure 1.c	255	Ceramic column grid array (CCGA-Cu spiral column)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device class V.

1.3 Absolute maximum ratings. 1/ 2/ 3/ 4/ 5/ 6/

Absolute Maximum ratings

Parameter	Symbol	Value	Unit
Positive Analogue supply voltage	V_{CCA5}	6.0	V
Positive Analogue supply voltage	V_{CCA3}	4.0	V
Positive Digital supply voltage	V_{CCD}	4.0	V
Digital inputs (on each single-ended input) and IDC , SYNC, SYNCN, signal Port P = A, B, C, D $V_{IL\ maximum}$ $V_{IH\ minimum}$ Digital input maximum Differential mode Swing	[P0..P9], [P0NP9N] IDC_P, IDC_N SYNC, SYNCN	GND–0.3 VCCA3 2.0	V V Vpp
Master clock input: $V_{IL\ maximum}$ $V_{IH\ minimum}$ Master clock maximum differential mode Swing	CLK, CLKN	1.5 3.5 2.5	V V Vpp
Control functions inputs $V_{IL\ maximum}$ $V_{IH\ minimum}$	MUX, MODE[0..1], PSS[0..2], OCDS[0..1]	-0.4V V_{CCD}+0.4	V V
Gain Adjustment function	GA	-0.3V,V_{CCA3}+0.3	V
Junction Temperature	T_J	170°C	°C
Storage temperature	T_{STG}	-65°C to 150°C	°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.

3/ All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

4/ Maximum ratings enable active inputs with DAC powered off.

5/ Maximum ratings enable floating inputs with DAC powered on.

6/ DSP clock and STVF, HTVF output buffers must not be shorted to ground nor positive power supply.

1.4 Recommended operating conditions.

Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit	Note
Positive analogue supply voltage	V_{CCA5}		5.0	V	2, 4
Positive analogue supply voltage	V_{CCA3}		3.3	V	1, 2, 4
Positive digital supply voltage	V_{CCD}		3.3	V	2, 4
Digital inputs (on each single-ended input) and IDC , SYNC signals $V_{IL\ maximum}$ $V_{IH\ minimum}$ Differential mode Swing	[P0..P9], [P0N..P9N] IDC_P, IDC_N SYNC, SYNCN		1.075 1.425 700	V V mVpp	3
Control functions inputs	MUX, OCDS, PSS, MODE	V_{IL} V_{IH}	0 V_{CCD}	V V	
Master clock input power level (Differential mode)	P_{CLK}		3	dBm	3
Gain Adjustment function	GA	Range	0 V_{CCA3}	V	
Operating Temperature Range	Tc, Tj	class V	Tc= -55°C to T_J = 125°C	°C	

_____

1. For low temperature it is recommended to operate at maximum analog supplies (V_{CCA3}) level.

2. For power up sequence on the EV10DS130A devices the followings instruction must be implemented in order to obtain the guaranteed performances and functionality; and the following rules shall be followed when powering the device (see figure 7 ”Power Up Sequencing”)

It is necessary to raise V_{CCA5} power supply within the range 5.20V up to a recommended maximum of 5.60V during at least 1ms at power up. Then the supply voltage has to settle within 500 ms to a steady nominal supply voltage within a range of 4.75V up to 5.25V. A power-up sequence on V_{CCA5} that does not comply with the above recommendation will not compromise the functional operation of the device. Only the noise floor will be affected.

At power-up a SYNC pulse is internally and automatically generated when the following sequence is satisfied: V_{CCD}, V_{CCA3} and V_{CCA5}. To cancel the SYNC pulse at power-up, it is necessary to apply the sequence: V_{CCA5}, V_{CCA3}, V_{CCD}. (V_{CCA3} cannot reach 0.5V until V_{CCA5} is greater than 4.5V. V_{CCD} cannot reach 0.5V until V_{CCA3} is greater than 3.0V). Any other sequence may not have a deterministic SYNC behaviour.

Relationship between power supplies:

Within the applicable power supplies range, the following relationship shall always be satisfied $V_{CCA3} \geq V_{CCD,}$ taking into account AGND and DGND planes are merged and power supplies accuracy.

3. Analog output is in differential. Single-ended operation is not recommended. Guaranteed performances are only in differential configuration.

4. The rise time for any of the power supplies (V_{CCD}, V_{CCA5} and V_{CCA3}) shall be ≤ 10 ms. No power-down sequencing is required.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device class V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figures 1.a, 1.b and 1.c.

3.2.2 Terminal connections. The terminal connections, pin out table and function description shall be as specified respectively on figures 2.1, 2.2 and 2.3.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Input and output protection networks shall be as specified on figure 6.

3.2.7 Power up sequence as specified on figure 7.

3.2.8 Thermal characteristic shall be as specified on figure 8.

3.2.9 Solderability test for BGA/CGA packages: Solderability test for case outline S or C for column grid array(CGA) or ball grid array(BGA) package has been verified during solder column or ball attachment process in accordance with method 2003 of MIL-STD-883.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device class V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device class V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device class V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Handling precaution. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling. These components are categorized as ESDS class 1C in accordance with MIL-PRF-38535.

3.9 Mounting and storage recommendation. In order to avoid the risk of solderability (or wettability) it is recommended to mount the component onto the PCB within 2 years after the date of sealing.

TABLE I. Electrical performance characteristics.

Test description	Symbol	Conditions -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit Min	Limit Max	Units
Input Data Bits differential resistance measurement	R	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	1	80	120	Ω
				2, 3	80	120	
Leakage current measurement on input data Bits	I_{L_min}		01	1	-160	-260	µA
				2, 3	-150	-270	
	I_{L_max}	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	1	160	260	µA
				2, 3	160	270	
Power supply current with nominal power supply (2:1 MUX)	I_{VCCA5} (Analog mode)	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	1	64	90	mA
				2, 3	62	92	
	I_{VCCA3} (Analog mode)		01	1	79	122	mA
				2, 3	74	125	
	I_{VCCD} (Digital mode)		01	1	118	177	mA
				2, 3	111	185	
Power dissipation with nominal power supply (2:1 MUX)	P_D		01	1	795	1420	mW
				2, 3	695	1500	
Power supply current with nominal power supply (4:1 MUX)	I_{VCCA5} (Analog mode)		01	1	64	90	mA
				2, 3	62	92	
	I_{VCCA3} (Analog mode)		01	1	79	122	mA
				2, 3	74	125	
	I_{VCCD} (Digital mode)		01	1	139	205	mA
				2, 3	129	213	
Power dissipation with nominal power supply (4:1 MUX)	P_D		01	1	795	1520	mW
				2, 3	695	1600	
Power supply current with maximum power supply (2:1 MUX)	I_{VCCA5} (Analog mode)	V_{CCA5} = 5.25V V_{CCA3} = 3.45V V_{CCD} = 3.45V 1/ , 5/ 7/	01	1	64	91	mA
				2, 3	61	92	
	I_{VCCA3} (Analog mode)		01	1	89	138	mA
				2, 3	84	139	
	I_{VCCD} (Digital mode)		01	1	132	190	mA
				2, 3	119	197	
Power dissipation with maximum power supply (2:1 MUX)	P_D		01	1	795	1600	mW
				2, 3	695	1620	
Power supply current with maximum power supply (4:1 MUX)	I_{VCCA5} (Analog mode)		01	1	64	91	mA
				2, 3	61	92	
	I_{VCCA3} (Analog mode)		01	1	89	137	mA
				2, 3	84	139	
	I_{VCCD} (Digital mode)		01	1	154	154	mA
				2, 3	139	229	
Power dissipation with maximum power supply (4:1 MUX)	P_D		01	1	795	1710	mW
				2, 3	695	1750	

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Power supply current with minimum power supply (2:1 MUX)	I_{VCCA5} (Analog mode)	V_{CCA5} = 4.75V V_{CCA3} = 3.15V V_{CCD} = 3.15V 1/ , 5/ 7/	01	1	63	87	mA
				2, 3	60	89	
	I_{VCCA3} (Analog mode)			1	69	111	
				2, 3	60	114	
	I_{VCCD} (Digital mode)			1	108	162	
				2, 3	94	169	
Power dissipation with minimum power supply (2:1 MUX)	P_D		01	1	795	1260	mW
				2, 3	695	1300	
Power supply current with minimum power supply (4:1 MUX)	I_{VCCA5} (Analog mode)			1	63	87	mA
				2, 3	60	89	
	I_{VCCA3} (Analog mode)			1	69	111	
				2, 3	60	114	
	I_{VCCD} (Digital mode)			1	126	187	
				2, 3	109	196	
Power dissipation with minimum power supply (4:1 MUX)	P_D			1	795	1350	mW
				2, 3	695	1400	
Clock inputs common mode	CM_CLOCKP		01	7, 8A, 8B	2.4	2.6	V
	CM_CLOCKN				2.4	2.6	
Clock input Differential input impedance/resistance	Z_CLOCK		01		80	120	Ω
Analog output Full-scale differential output voltage	Full-scale_GA_Max		01	7, 8A, 8B	1.02		V
	Full-scale_GA_Typ				1.02	1.08	
	Full-scale_GA_Min					0.98-	
Analog output DC gain adjustment (GA)	2/ 3/		01			5	%
Analog output DC gain sensitivity to power supply	2/ 3/		01			6	
Analog output Internal differential resistance/impedance with nominal power supply	Z_Output		01	1, 2, 3	90	110	Ω
LVDS logic compatibility Differential outputs voltage at common mode(for codes 0, 2048 and 4096) with nominal power supply	CM_OUT_In_MidCode		01	1, 2, 3	4.48	4.66	V
	CM_OUTN_In_MidCode		01	1, 2, 3	4.48	4.66	V
DSP clock output LVDS swing voltage with nominal power supply	Swing_DSP_CLK		01	1, 2, 3	0.24	0.45	V
	Swing_DSP_CLKN				0.24	0.45	V

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
DSP CLK Frequency (MUX 2:1, OCDS and IUCM modes with logic 0 and 1)	DSP_freq_OCDS00_IUCM0	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	9,10,11	373	377	MHz
	DSP_freq_OCDS01_IUCM0				186	189	
	DSP_freq_OCDS10_IUCM0				92	95	
	DSP_freq_OCDS11_IUCM0				45	48	
DSP CLK Frequency (MUX 4:1, OCDS and IUCM modes with logic 0 and 1)	DSP_freq_OCDS00_IUCM0				373	377	
	DSP_freq_OCDS01_IUCM0				186	189	
	DSP_freq_OCDS10_IUCM0				92	95	
	DSP_freq_OCDS11_IUCM0				45	48	
DSP CLK Frequency (MUX 2:1, OCDS and IUCM modes with logic 0 and 1)	DSP_freq_OCDS00_IUCM1				186	189	
	DSP_freq_OCDS01_IUCM1				92	95	
	DSP_freq_OCDS10_IUCM1				45	48	
	DSP_freq_OCDS11_IUCM1				22	25	
DSP CLK Frequency (MUX 4:1, OCDS and IUCM digital function with logic 0 and 1)	DSP_freq_OCDS00_IUCM1			9,10,11	186	189	
	DSP_freq_OCDS01_IUCM1				92	95	
	DSP_freq_OCDS10_IUCM1				45	48	
	DSP_freq_OCDS11_IUCM1				22	25	
DSP CLK delay measurement with digital function PSS logic 0 and 1	PSS001	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	9,10,11	0.49	0.51	ns
	PSS010				0.99	1.01	
	PSS011				1.49	1.51	
	PSS100				1.99	2.01	
	PSS101				2.49	2.51	
	PSS110				2.99	3.01	
	PSS111				3.49	3.51	
Digital output function Flags STVF and HTVF levels and functional verification	VOL_STVF	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	1, 2, 3	0,8	0.8-	V
	VOL_HTVF			1, 2, 3	0,8	0.8	
	VOH_STVF			1	2.3		
				2, 3	2.1		
	VOH_HTVF			1	2.3		
				2, 3	2.1		

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
NRTZ mode (First Nyquist zone) MUX 4:1 clock = 3GSps Fout = 100MHz 0 dBFS	High Spur Level	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4		-56	dBm
				5, 6		-54	
	SFDR@100M_3G_NRZ			4		-57	dBc
				5, 6		-55	
Fclock = 3GSps Fout = 100MHz Power supply : typ MUX : 4 :1 mode : NRTZ level : 0 dBFS	High Spur Level			4		-62	dBm
				5, 6		-60	
	SFDR@100M_3G_RNRZ			4		-60	dBc
				5, 6		-58	
Fclock = 3GSps Fout = 700MHz MUX : 4 :1 mode : NRTZ level : 0 dBFS	High Spur Level			4		-57	dBm
				5, 6		-55	
	SFDR@700M_3G_RNRZ			4		-53	dBc
				5, 6		-51	
Fclock = 3GSps Fout = 1800MHz Power supply : typ MUX : 4 :1 mode : NRTZ level : 0 dBFS	High Spur Level			4		-57	dBm
				5, 6		-55	
	SFDR@1G8_3G_RNRZ			4		-52	dBc
				5, 6		-50	
Fclock = 3GSps Fout = 1600MHz Power supply : typ MUX : 4 :1 mode : RTZ level : 0 dBFS	High Spur Level			4		-57	dBm
				5, 6		-55	
	SFDR@1G6_3G_RTZ			4		-49	dBc
				5, 6		-47	
Fclock = 3GSps Fout = 2900MHz Power supply : typ MUX : 4 :1 mode : RTZ level : 0 dBFS	High Spur Level	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4		-58	dBm
				5, 6		-56	
	SFDR@2G9_3G_RTZ			4		-50	dBc
				5, 6		-48	
Fclock = 3GSps Fout = 1600MHz Power supply : typ MUX : 4 :1 mode : RF level : 0 dBFS	High Spur Level	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4		-51	dBm
				5, 6		-49	
	SFDR@1G6_3G_RF			4		-44	dBc
				5, 6		-42	

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Fclock = 3GSps Fout = 3800MHz Power supply : typ MUX : 4 :1 mode : RF level : 0 dBFS	High Spur Level	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4		-53	dBm
				5, 6		-51	
	SFDR@3G8_3G			4		-45	dBc
				5, 6		-43	
Fclock = 3GSps Fout = 4400MHz Power supply : typ MUX : 4 :1 mode : RF level : 0 dBFS	High Spur Level	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4		-56	dBm
				5, 6		-54	
	SFDR@4G4_3G			4		-45	dBc
				5, 6		-43	
Fclock = 1.5GSps Fout = 700MHz Power supply : typ MUX : 2 :1 mode : NRTZ level : 0 dBFS	High Spur Level			4		-54	dBm
				5, 6		-52	
	SFDR@700M_3G			4		-52	dBc
				5, 6		-50	
Fclock = 3GSps Fout = 100MHz Power supply : typ MUX : 4 :1 mode : NRZ level : -3 dBFS	High Spur Level			4		-59	dBm
				5, 6		-57	
	SFDR-3dBFS@100M_3G			4		-58	dBc
				5, 6		-56	
Fclock = 3GSps Fout = 700MHz Power supply : typ MUX : 4 :1 mode : NRTZ level : -3 dBFS	High Spur Level			4		-62	dBm
				5, 6		-60	
	SFDR-3dBFS@700M_3G			4		-57	dBc
				5, 6		-53	
Fclock = 3GSps Fout = 1800MHz Power supply : typ MUX : 4 :1 mode : RTZ level : -3 dBFS IUCM enabled	High Spur Level			4		-62	dBm
				5, 6		-60	
	SFDR@1G8_3G			4		-45	dBc
				5, 6		-43	

TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit		Units
					Min	Max	
Functional test with minimum swing on data In Fclock = 3GSps Fout = 1600MHz Power supply : typ MUX : 4 :1, mode : RTZ level : 0 dBFS IUCM disabled	Digital input Swing High Spur Level	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4		-57	dBm
				5, 6		-51	
	Digital input Swing SFDR@1G6_3G			4		-49	dBc
				5, 6		-44	
Functional test with Maximum swing on data In Fclock = 3GSps Fout = 1600MHz Power supply : typ MUX : 4 :1, mode : RTZ level : 0 dBFS IUCM disabled	Digital input Swing High Spur Level			4		-57	dBm
				5, 6		-51	
	Digital input Swing SFDR@1G6_3G			4		-49	dBc
				5, 6		-44	
NPR measurement with a -14dB Loading Factor noise from 20MHz to 900MHz and a 25MHz wide notch centered on 450MHz NPR measurement on 1st Nyquist - Mode NRZ	NPR@LF=-14dB			4	44		dB
				5, 6	43		
	ENOBeq@LF=-14dB			4	sanction from NPR value		**Bit**
	SNReq@LF=-14dB			5, 6			**dB**
NPR measurement with a -14dB Loading Factor noise from 20MHz to 900MHz and a 25MHz wide notch centered on 450MHz NPR measurement on 1st Nyquist - Mode NRTZ	NPR@LF=-14dB			4	45		dB
				5, 6	44		
	ENOBeq@LF=-14dB			4	sanction from NPR value		**Bit**
	SNReq@LF=-14dB			5, 6			**dB**
NPR measurement with a -14dB Loading Factor noise from 1520MHz to 2200MHz and a 25MHz wide notch centered on 1850MHz NPR measurement on 2nd Nyquist - Mode RTZ	NPR@LF=-14dB			4	38		dB
				5, 6	37		
	ENOBeq@LF=-14dB			4	sanction from NPR value		**Bit**
	SNReq@LF=-14dB			5, 6			**dB**
NPR measurement with a -14dB Loading Factor noise from 1520MHz to 2200MHz and a 25MHz wide notch centered on 1850MHz NPR measurement on 2nd Nyquist - Mode RF	NPR@LF=-14dB			4	36		dB
				5, 6	35		
	ENOBeq@LF=-14dB			4	sanction from NPR value		**Bit**
	SNReq@LF=-14dB			5, 6			**dB**

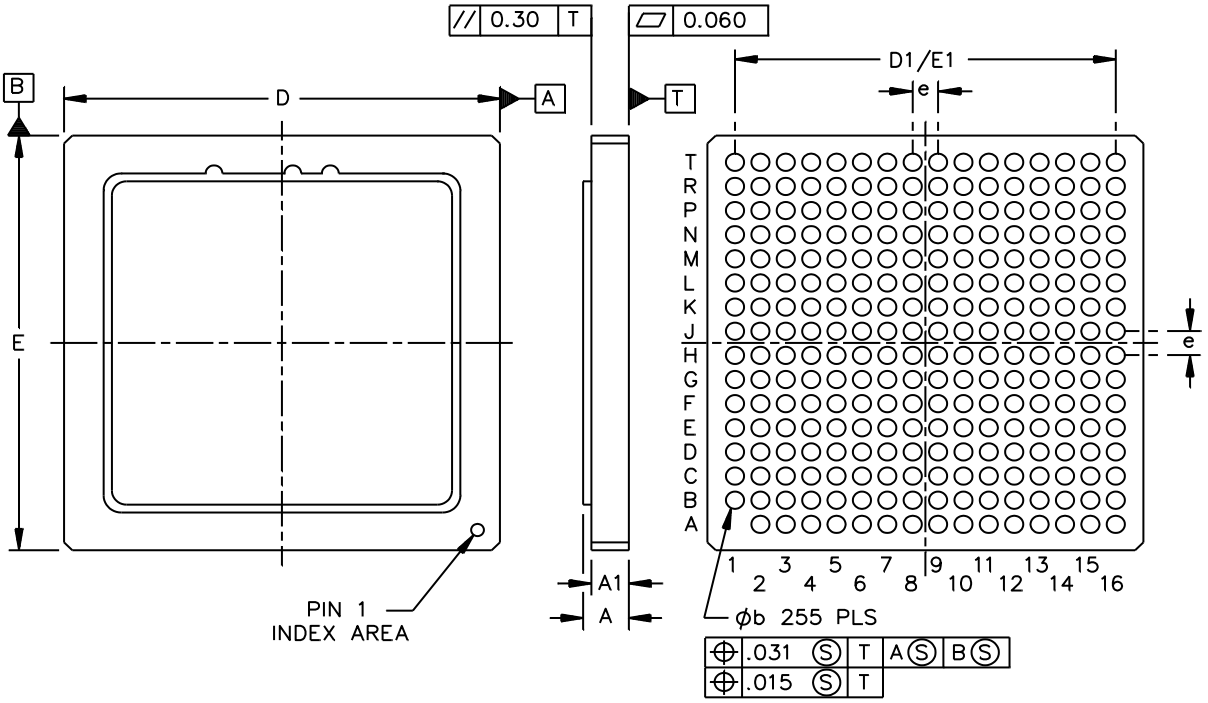
TABLE I. Electrical performance characteristics – continued.

Test description	Test Symbol	Conditions -55°C ≤ T_J ≤ +125°C unless otherwise specified	Device Type	Group A Subgroups	Limit Min	Limit Max	Units
NPR measurement with a -14dB Loading Factor noise from 2200MHz to 2880MHz and a 25MHz wide notch centered on 2550MHz NPR measurement on 2nd Nyquist - Mode RF	NPR@LF=-14dB	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4	-	36	dB
				5, 6	-	35	
	ENOBeq@LF=-14dB			4	sanction from NPR value		bit
	SNReq@LF=-14dB			5, 6			dB
NPR measurement with a -14dB Loading Factor noise from 3050MHz to 3700MHz and a 25MHz wide notch centered on 3375MHz NPR measurement on 3rd Nyquist - Mode RF	NPR@LF=-14dB			4	-	36	dB
				5, 6	-	35	
	ENOBeq@LF=-14dB			4	sanction from NPR value		bit
	SNReq@LF=-14dB			5, 6			dB
Self Noise Density at codes 0 and 4095 vs modes (NRZ,RNRZ,RTZ,RF)	SND_NRZ_0	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	4		-154	dBm/Hz
				5, 6		-150	
	SND_NRZ_4096			4		-154	
				5, 6		-150	
	SND_RNRZ_0			4		-140	
				5, 6		-138	
	SND_RNRZ_4096			4		-140	
				5, 6		-138	
	SND_RTZ_0			4		-140	
				5, 6		-139	
	SND_RTZ_4096			4		-140	
				5, 6		-139	
	SND_RF_0			4		-138.5	
				5, 6		-138	
	SND_RF_4096			4		-138.5	
				5, 6		-138	
INL / DNL measurement	DNL_min100k3G	V_{CCA5} = 5.0V V_{CCA3} = 3.3V V_{CCD} = 3.3V 1/ , 5/ 7/	01	7	-	-0,80	LSB
				8A, 8B	-	-0.90	
	DNL_max100k3G			7	0.80	-	
				8A, 8B	0.90		
	INL_min100k3G			7	-	-1.2	
				8A, 8B	-	-1.5	
	INL_max100k3G			7	1.2	-	
				8A, 8B	1.5	-	

1. For use in higher Nyquist zone, it is recommended to use higher power clock within the limit.
2. Initial gain error corresponds to the deviation of the DC gain center value from unity gain. The DC gain adjustment (GA function) ensures that the initial gain deviation can be cancelled. The DC gain sensitivity to power supplies is given according the rule: GainSensVsSupply = |Gain@VccMin – Gain@VccMax| / Gain@Vccnom
3. Single-ended operation is not recommended, this line is given for better understanding of what is output by the DAC.
4. In order to modify the V_{OL}/V_{OH} value, potential divider could be used.
5. Sink or source.
6. Within the applicable power supplies range, the following relationship shall always be satisfied V_{CCA3} V_{CCD}, taking into account AGND and DGND planes are merged and power supplies accuracy.
7. Group A, subgroup 3, 6, 8B, 11 tests are guaranteed for Tc = -55°C.

Case outline. “X”

LGA255 top, bottom & side view (Seal ring connected to AGND)



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	2.01	2.45	D1/E1	19.05 TYP	
A1	1.62	1.98	e	1.27 TYP	
b	0.76	0.96			
D/E	20.8	21.2			

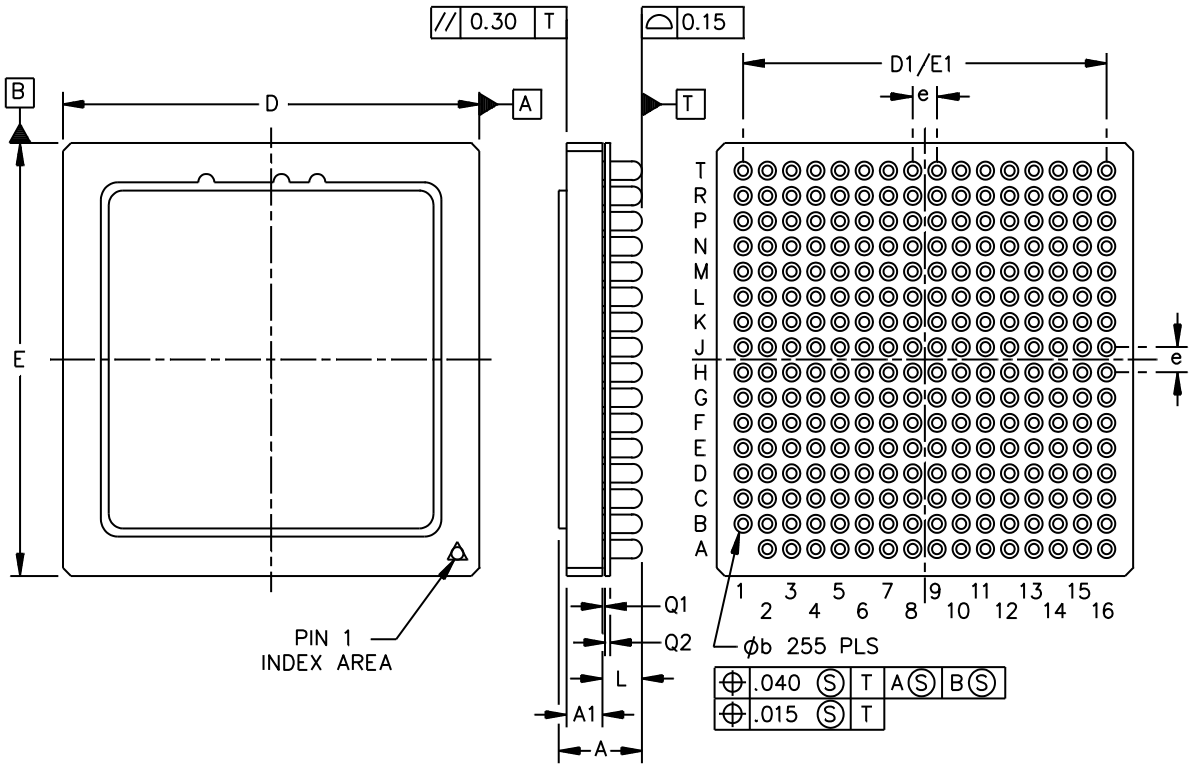
Notes:

1. Metal lid 0.38mm thickness + 0.5mm solder with 16.38mm SQ lid. Finish Au plated over nickel.
2. All exposes metal must be plated electroless nickel thickness 1.27~8.99 micron and Au plated 1.50 micron minimum.

FIGURE 1.a - Case outline “X”

Case outline. “Y”

Ci-CGA255 top, bottom & side view (seal ring connected to AGND)



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	4.02	4.58	D1/E1	19.05 TYP	
A1	1.65	1.95	e	1.27 TYP	
b	0.79	0.99	L	1.62 TYP	
D/E	20.8	21.2			

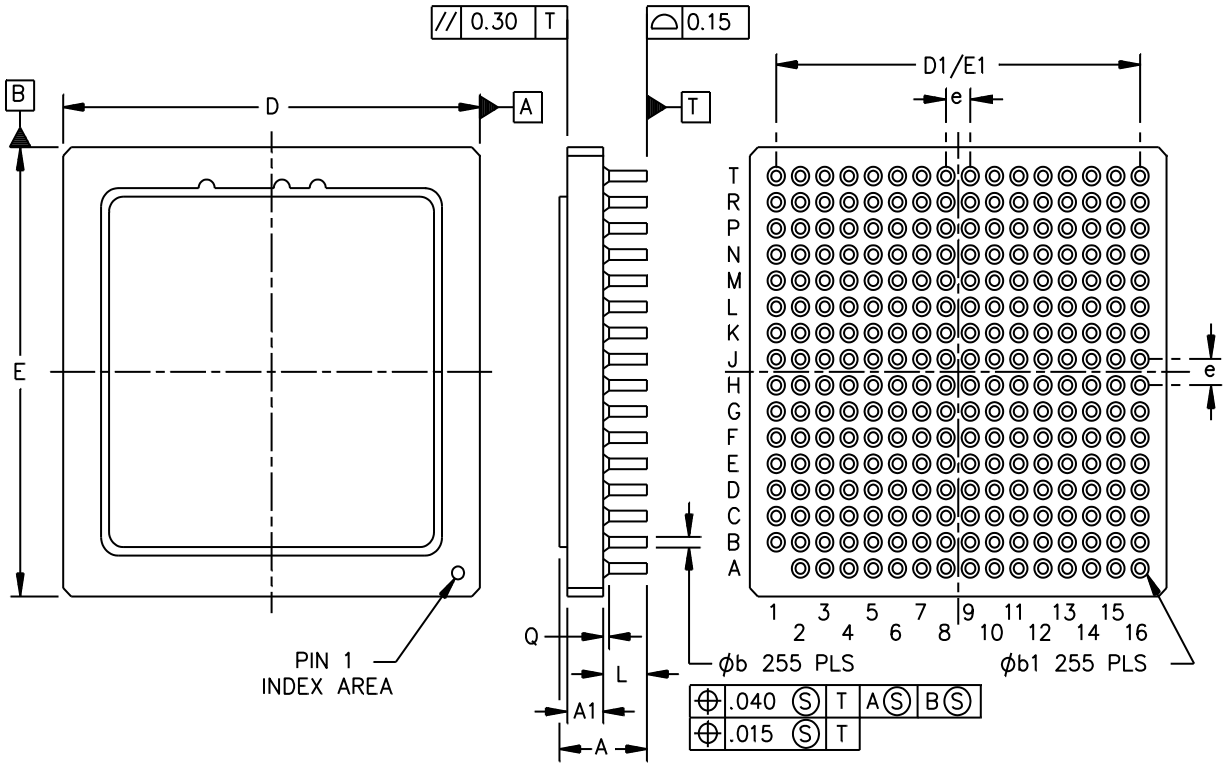
Notes:

1. Triangle patterned on top A1 corner 550 µm side width triangle. Chamfer 0.4 all 4side. No column on A1 corner
2. All exposes metal must be plated electroless nickel thickness 1.27~8.99 micron and Au plated 1.50 micron minimum. Assembly of SCI on LGA using 63/37 tin/lead solder bump. Column alloy composition of 90/10 lead/tin.

FIGURE 1.b Case outline “Y”

Case outline "Z"

CCGA255 top, bottom & side view (seal ring connected to AGND)



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	4.05	4.81	D1/E1	19.05 TYP	
A1	1.62	1.98	e	1.27 TYP	
b	0.41	0.61	L	2.00	2.40
D/E	20.8	21.2			

Notes:

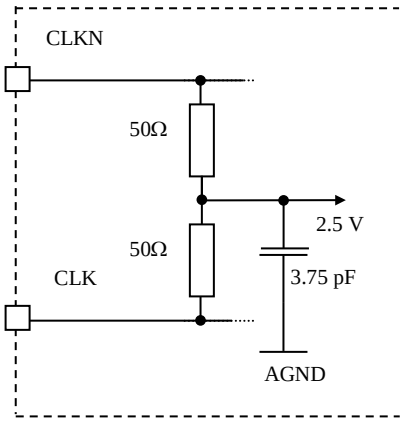
1. Circle dot patterned on top A1 corner 570 µm diameter. Chamfer 0.4 all 4side. No column on A1 corner.
2. All exposes metal must be plated electroless nickel thickness 1.27~8.99 micron and Au plated 1.50 micron minimum. Assembly of columns on LGA using 63/37 tin/lead solder. Column alloy composition of tin (Sn) 20% and lead(Pb) 80% with copper spiral.

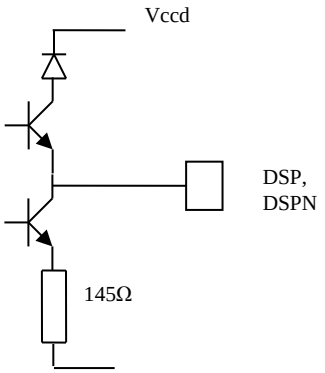
FIGURE 1.c Case outline "Z"

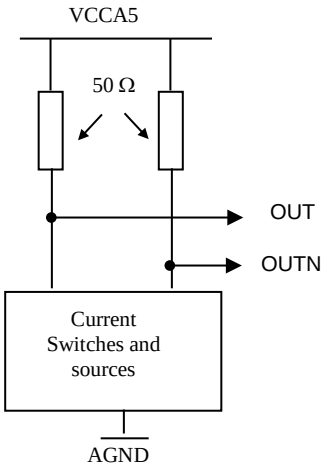
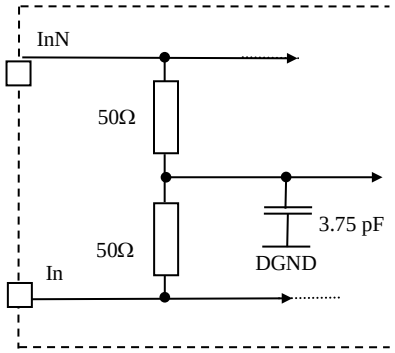
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		VCCD	B2	B3	B6	B8	B7	B9	C9	C7	C8	C6	C3	C2	VCCD	DGND	A
B	DGND	VCCD	B2N	B3N	B6N	B8N	B7N	B9N	C9N	C7N	C8N	C6N	C3N	C2N	VCCD	DGND	B
C	B1	B1N	VCCD	DGND	B5N	B5	B4	B4N	C4N	C4	C5	C5N	DGND	VCCD	C1N	C1	C
D	B0	B0N	DGND	VCCD	VCCD	DGND	DGND	DGND	DGND	DGND	DGND	VCCD	VCCD	DGND	C0N	C0	D
E	NC	NC	NC	DGND	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	DGND	NC	NC	NC	E
F	A8	A8N	NC	DGND	VCCD	DGND	DGND	VCCD	VCCD	DGND	DGND	VCCD	DGND	NC	D8N	D8	F
G	A9	A9N	A7N	DGND	VCCD	VCCD	AGND	AGND	AGND	AGND	VCCD	VCCD	DGND	D7N	D9N	D9	G
H	A6	A6N	A7	DGND	DGND	VCCD	AGND	AGND	AGND	AGND	VCCD	DGND	DGND	D7	D6N	D6	H
J	A4	A4N	NC	DGND	DGND	VCCA3	AGND	AGND	AGND	AGND	VCCA3	DGND	DGND	NC	D4N	D4	J
K	A1	A1N	NC	VCC3	VCCA3	VCCA3	AGND	AGND	AGND	AGND	VCCA3	VCCA3	VCC3	NC	D1N	D1	K
L	A5	A5N	A0	DGND	DGND	DGND	VCCA5	VCCA5	VCCA5	VCCA5	DGND	DGND	DGND	D0	D5N	D5	L
M	A3	A3N	A0N	DGND	DGND	DIODE	AGND	VCCA5	AGND	VCCA5	NC or DGND	IUCM	DGND	D0N	D3N	D3	M
N	NC	NC	DSPN	HTVF	DGND	STVF	AGND	VCCA5	AGND	VCCA5	DGND	DGND	DGND	OCDS 0	NC	NC	N
P	A2	A2N	DSP	GA	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	OCDS 1	D2N	D2	P
R	DGND	DGND	DGND	IDC_P	SYNCN	CLKN	AGND	AGND	AGND	AGND	AGND	MODE 1	PSS1	PSS2	DGND	DGND	R
T	DGND	DGND	DGND	IDC_N	SYNC	CLK	AGND	AGND	OUT	OUTN	AGND	MODE 0	PSS0	MUX	DGND	DGND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

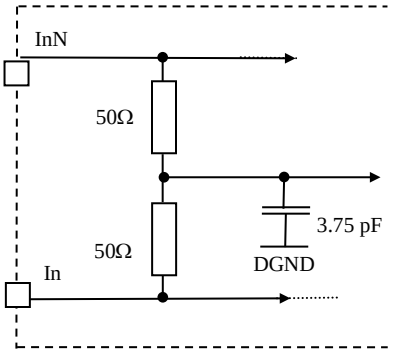
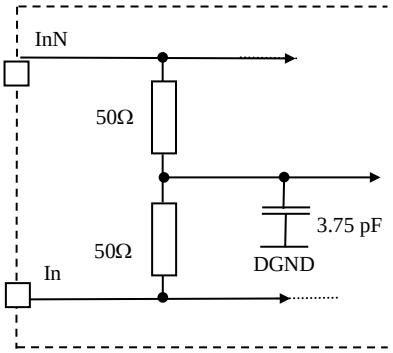
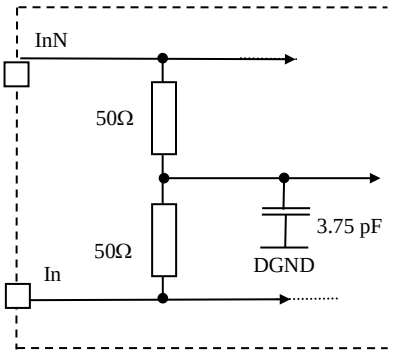
FIGURE 2. Terminal connections.

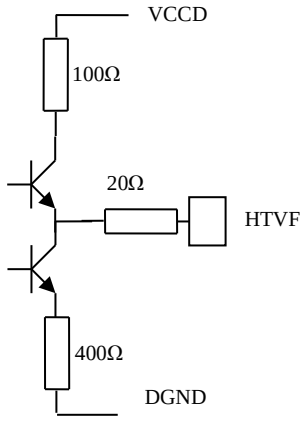
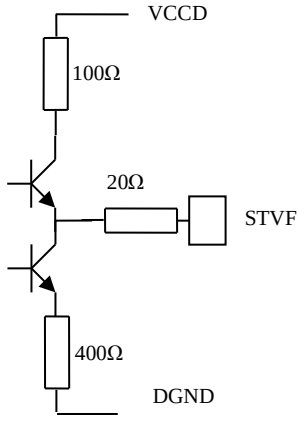
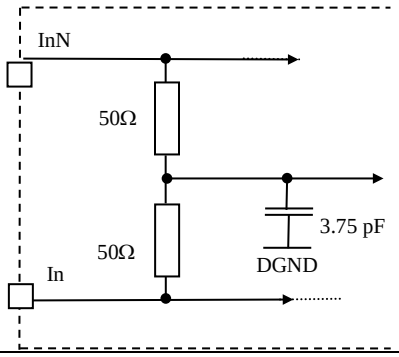
Pinout Table CLGA255

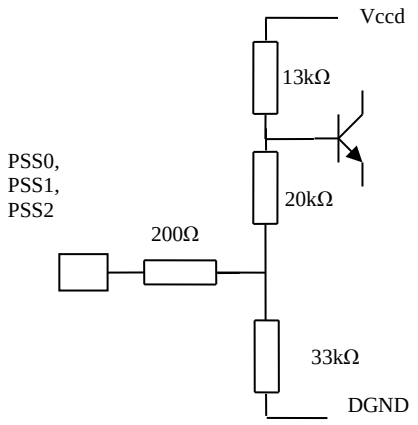
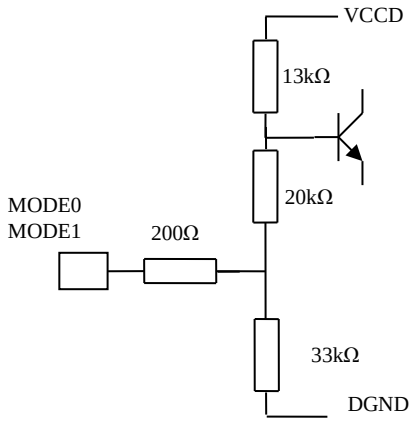
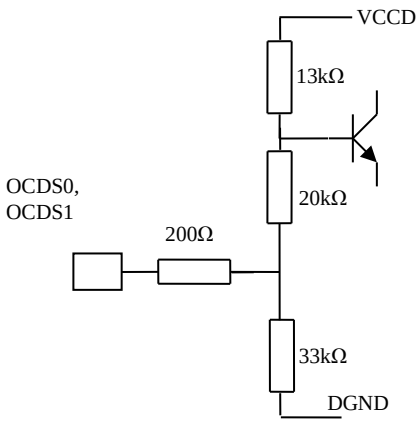
Signal Name	Pin number	Description	Direction	Equivalent simplified schematics
Power supplies				
V_{CCA5}	L7, L8, L9, L10, M8, M10, N8, N10	5V analogue power supplies Referenced to AGND		
V_{CCA3}	J6, J11, K4, K5, K6, K11, K12, K13	3.3V analogue power supply Referenced to AGND		
V_{CCD}	A2, A15, B2, B15, C3, C14, D4, D5, D12, D13, E7, E8, E9, E10, F5, F8, F9, F12, G5, G6, G11, G12, H6, H11	3.3V digital power supply Referenced to DGND		
AGND	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M7, M9, N7, N9, P6, P7, P8, P9, P10, P11, R7, R8, R9, R10, R11, T7, T8, T11	Analogue Ground		
DGND	A16, B1, B16, C4, C13, D3, D6, D7, D8, D9, D10, D11, D14, E4, E5, E6, E11, E12, E13, F4, F6, F7, F10, F11, F13, G4, G13, H4, H5, H12, H13, J4, J5, J12, J13, L4, L5, L6, L11, L12, L13, M4, M5, M13, N5, N11, N12, N13, P5, P12, P13, R1, R2, R3, R15, R16, T1, T2, T3, T15, T16	Digital Ground		
Clock signals				
CLK, CLKN	T6, R6	Sampling clock signal input (In-phase and inverted phase)	I	

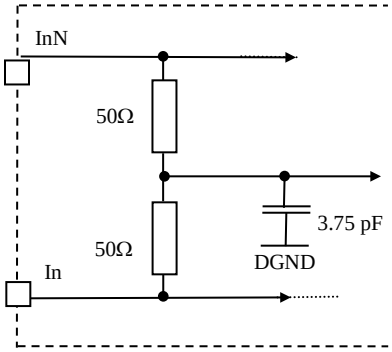
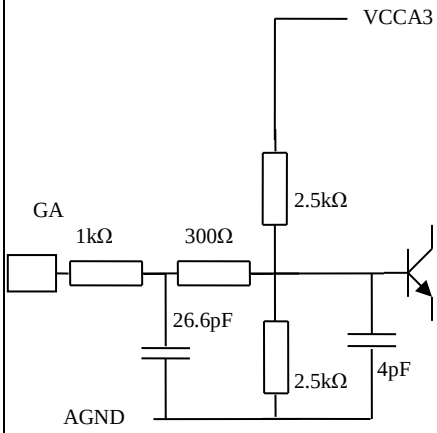
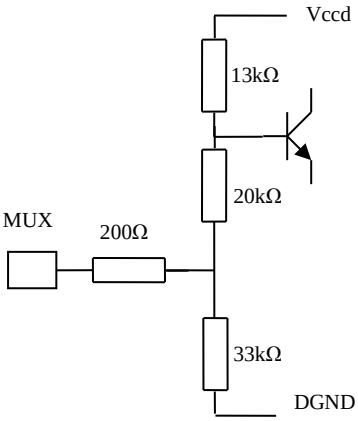
DSP, DSPN	P3, N3	Output clock (in-phase and inverted phase	O	

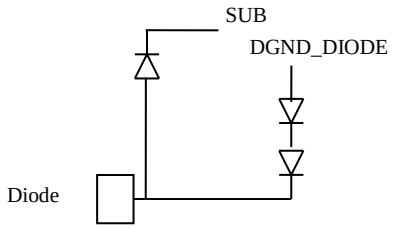
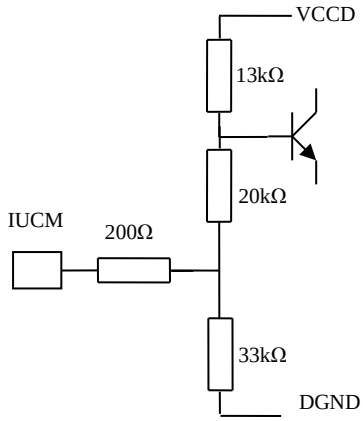
Analog output signal				
OUT, OUTN	T9, T10	In phase and inverted phase analogue output signal (differential termination required)	O	
Digital Input signals				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N	L3, M3 K1, K2 P1, P2 M1, M2 J1, J2 L1, L2 H1, H2 H3, G3 F1, F2 G1, G2	In-phase , inverted phase Digital input Port A Data A0, A0N is the LSB Data A9, A9N is the MSB	I	

B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N	D1, D2 C1, C2 A3, B3 A4, B4 C7, C8 C6, C5 A5, B5 A7, B7 A6, B6 A8, B8	In-phase , inverted phase Digital input Port B Data B0, B0N is the LSB Data B9, B9N is the MSB	I	
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N	D16, D15 C16, C15 A14, B14 A13, B13 C10, C9 C11, C12 A12, B12 A10, B10 A11, B11 A9, B9	In-phase , inverted phase Digital input Port C Data C0, C0N is the LSB Data C9, C9N is the MSB	I	
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N	L14, M14 K16, K15 P16, P15 M16, M15 J16, J15 L16, L15 H16, H15 H14, G14 F16, F15 G16, G15	In-phase , inverted phase Digital input Port D Data D0, D0N is the LSB Data D9, D9N is the MSB	I	

Control signals				
HTVF	N4	Set up time violation flag	O	
STVF	N6	Hold time violation flag	O	
IDC_P ICD_N	R4 T4	Input data check	I	

PSS0 PSS1 PSS2	T13 R13 R14	Phase Shift Select (PSS2 is the MSB)	I	
MODE0 MODE1	T12 R12	DAC Mode selection bits: - RTZ - NRZ - Narrow RTZ - RF	I	
OCDS0 OCDS1	N14 P14	Output Clock Division Select = these bits allow to select the clock division factor applied on the DSP, DSPN signal.	I	

SYNC, SYNCN	T5, R5	In phase and Inverted phase reset signal	I	
GA	P4	Gain adjust	I	
MUX	T14	MUX selection	I	

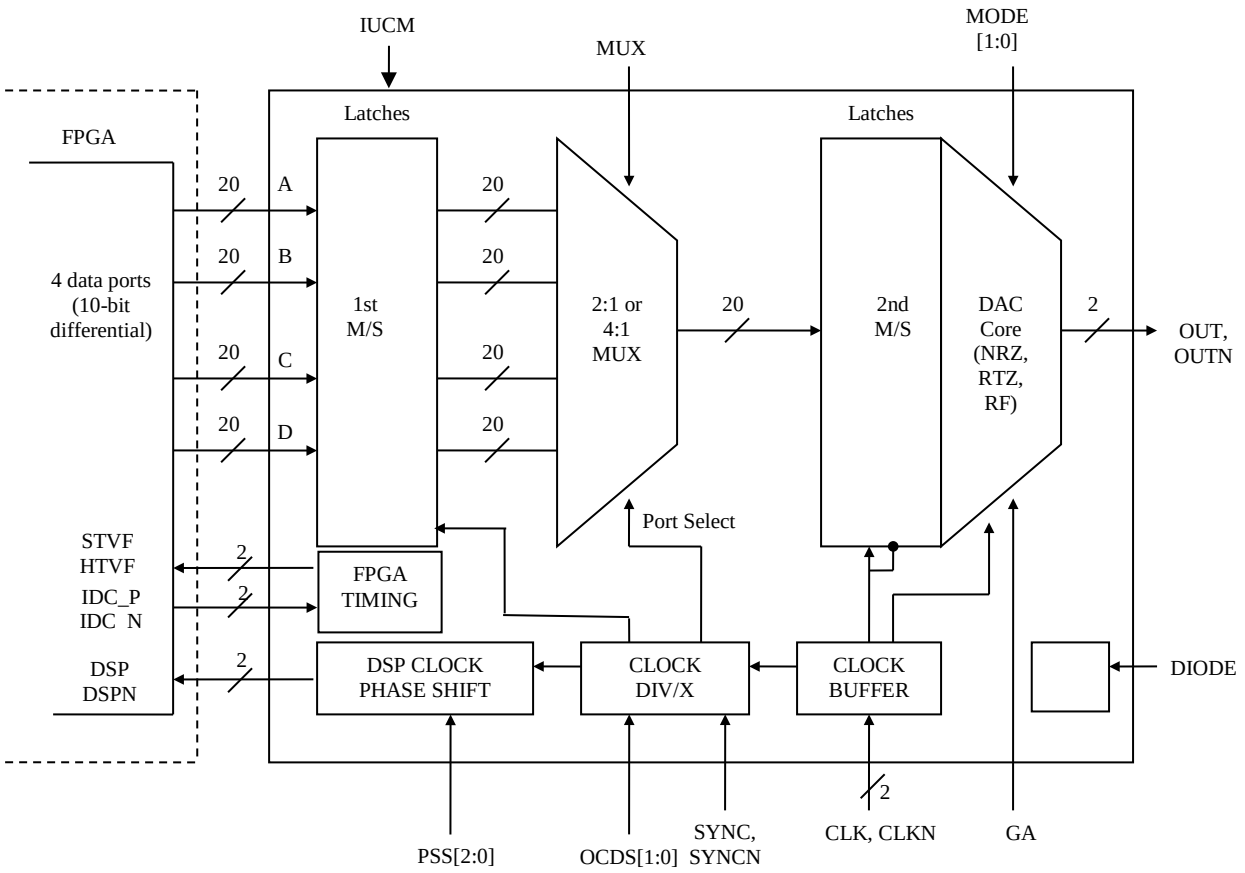
Diode	M6	Diode for die junction temperature monitoring function	I	
IUCM	M12	Input underclocking mode enable	I	
NC	E1, E2, E3, E14, E15,E16, F3, F14, J3, J14, K3, K14, M11, N1, N2, N15, N16	Reserved pin, NC, can be connected to DGND		

Functions Description

Name	Function	Name	Function
V_{CCD}	3.3V Digital Power Supply	CLK	In-phase Master clock
V_{CCA5}	5V Analog Power Supply	CLKN	Inverted phase Master clock
V_{CCA3}	3.3V Analog Power Supply	DSP_CK	In-phase Output clock
DGND	Digital Ground	DSP_CKN	Inverted phase Output clock
AGND	Analog ground (for analog supply reference)	PSS[0..2]	Phase shift select
A[9…0]	In-phase digital input Port A	GA	Gain Adjust
A[9..0]N	Inverted phase digital input Port A	MUX	MUX Selection
B[9…0]	In-phase digital input Port B	MODE[0..1]	DAC Mode: NRZ, RTZ, NRTZ, RF
B[9..0]N	Inverted phase digital input Port B	STVF	Setup time Violation flag
C[9…0]	In-phase digital input Port C	HTVF	Hold time Violation flag
C[9..0]N	Inverted phase digital input Port C	IDC_P, IDC_N	Input data check
D[9…0]	In-phase digital input Port D	OCDS[0..1]	Output Clock Division factor Selection (by 4 or 8)
D[9..0]N	Inverted phase digital input Port D	Diode	Diode for temperature monitoring
OUT	In-phase analog output	SYNC/ SYNCN	Synchronization signal (Active High)
OUTN	Inverted phase analog output	IUCM	input underclocking mode

Digital output MSB…….LSB	Differential Analogue Output
1111111111	+500mV
1100000000	+250mV
1010000000	+125mV
1000000000	0mV
0110000000	-125mV
0100000000	-250mV
0000000000	-500mV

FIGURE 3. Truth table.



NOTES:

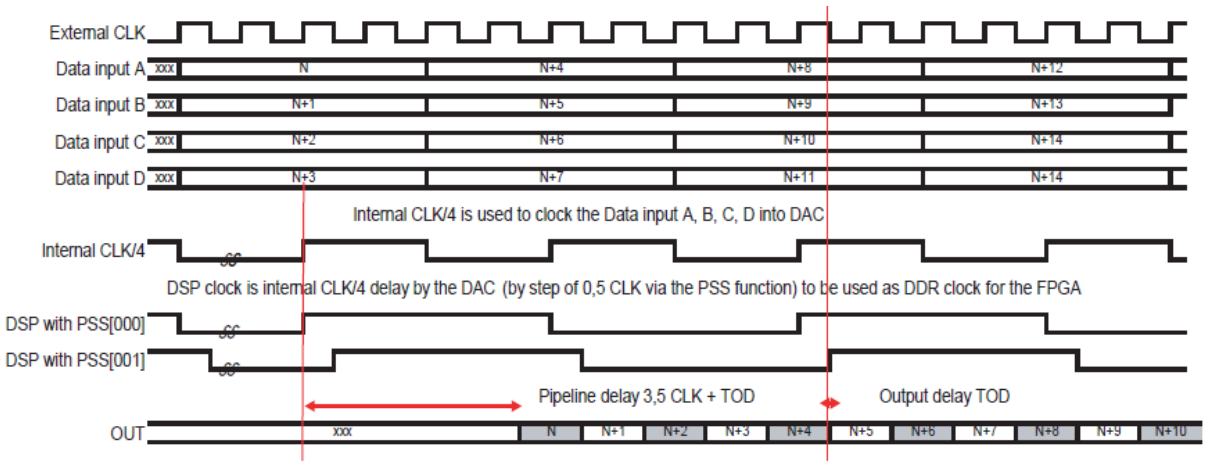
1. EV10DS130A die family is a 10-bit 3 GSps DAC with an integrated 4:1 or 2:1 multiplexer, allowing easy interface with standard LVDS FPGAs thanks to user friendly features as OCDS, PSS.

2. It embeds different output modes (RTZ, NRZ, narrow RTZ, RF) that allows performances optimizations depending on the working Nyquist zone.

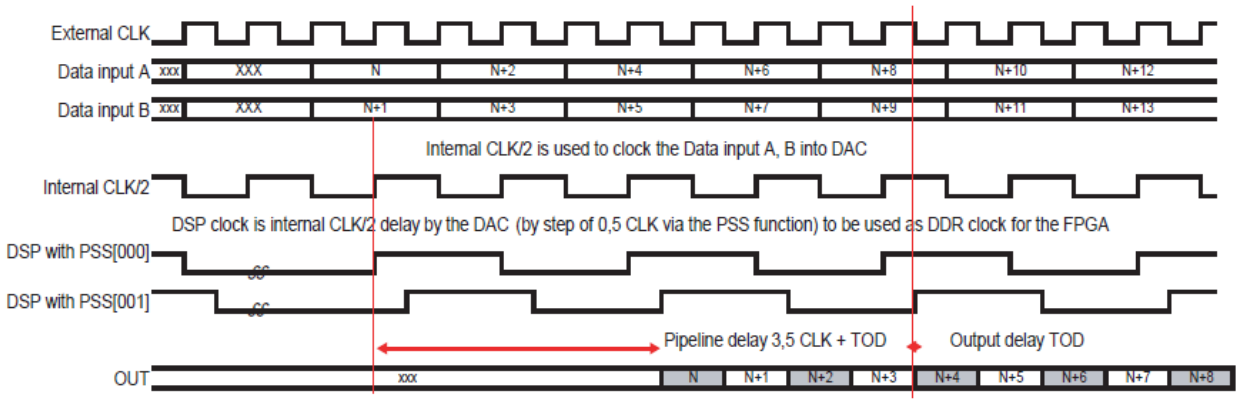
3. The Noise Power Ratio (NPR) performance, over more than 900 MHz instantaneous bandwidth, and the high linearity (SFDR, IMD) over full 1st Nyquist zone at 3 GSps (NRZ feature), make this product well suited for high-end applications such as arbitrary waveform generators and broadband DDS systems.

FIGURE 4. Block diagram.

5.1. Timing Diagram for 4:1 MUX principle of operation OCDS[00], IUCM disabled



5.2. Timing Diagram for 2:1 MUX principle of operation OCDS[00], IUCM disabled



5.3. SYNC Timing Diagram

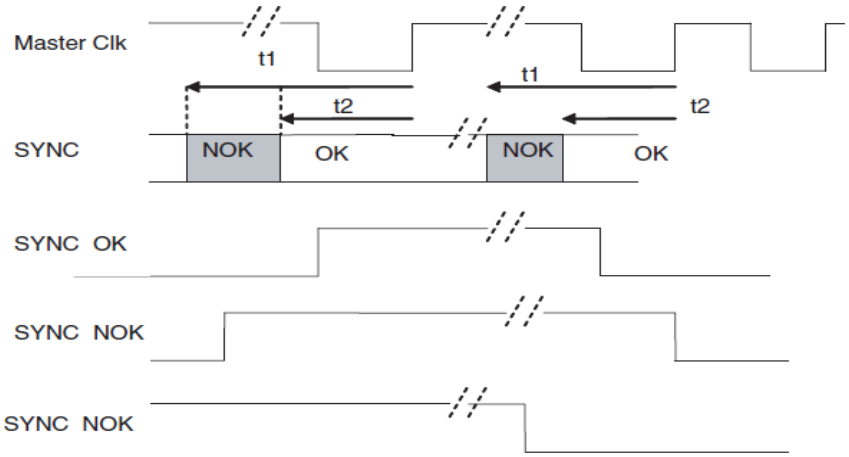
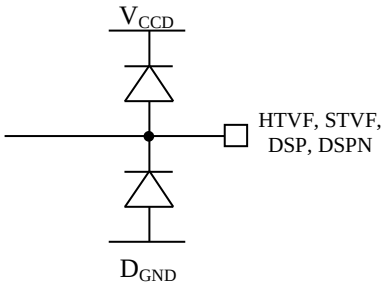
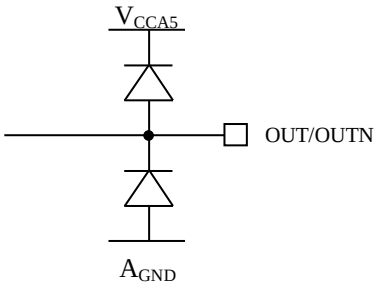


FIGURE 5. Timing waveforms.

Digital output ESD protections (HTVF, STVF, DSP, DSPN pins)



Analog output ESD protections (OUT/OUTN)



Static input buffer ESD protections (MODE, MUX, IUCM, OCDS, PSS, GA)

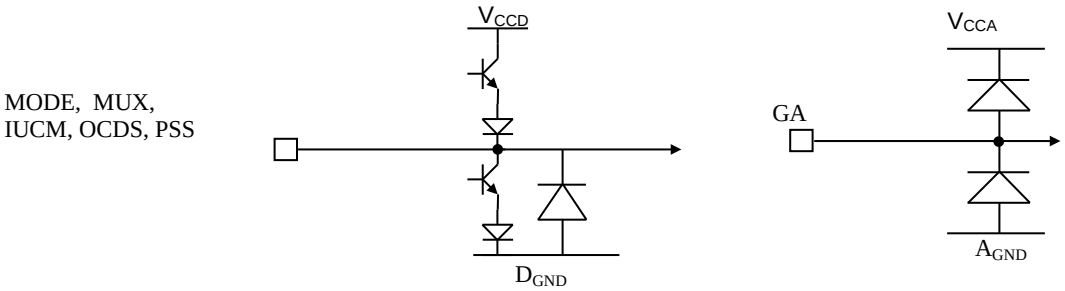
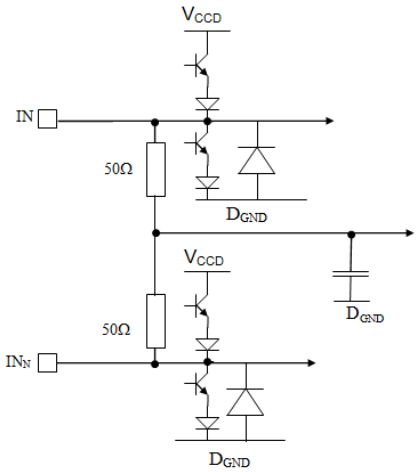


FIGURE 6. Input and output protection networks

LVDS input ESD protections (P0…P11N, CLKN, CLKN, SYNC, SYNCN, IDC, IDCP)
Port P – Port A, B, C, D



Power supplies ESD protections

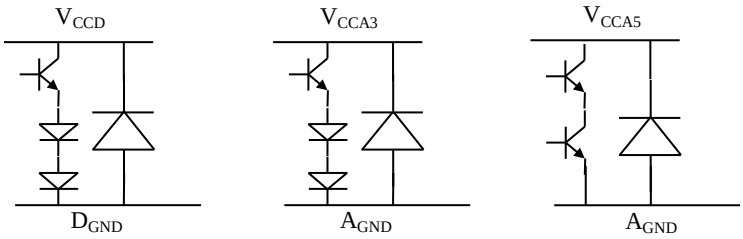


FIGURE 6. Input and output protection networks - continued.

For EV10DS130A the following instructions must be implemented:

Power-up sequence shall be implemented in order to obtain the guaranteed performances and functionality the following rules when powering the device:

It is necessary to raise V_{CCA5} power supply within the range 5.20V up to a recommended maximum of 5.60V during at least 1ms at power up. Then the supply voltage has to settle within 500 ms to a steady nominal supply voltage within a range of 4.75V up to 5.25V. A power-up sequence on V_{CCA5} that does not comply with the above recommendation will not compromise the functional operation of the device. Only the noise floor will be affected.

At power-up a SYNC pulse is internally and automatically generated when the following sequence is satisfied: V_{CCD}, V_{CCA3} and V_{CCA5}. To cancel the SYNC pulse at power-up, it is necessary to apply the sequence: V_{CCA5}, V_{CCA3}, V_{CCD}. (V_{CCA3} cannot reach 0.5V until V_{CCA5} is greater than 4.5V. V_{CCD} cannot reach 0.5V until VCCA3 is greater than 3.0V). Any other sequence may not have a deterministic SYNC behaviour.

Relationship between power supplies:

Within the applicable power supplies range, the following relationship shall always be satisfied $V_{CCA3} \geq V_{CCD}$, taking into account AGND and DGND planes are merged and power supplies accuracy.

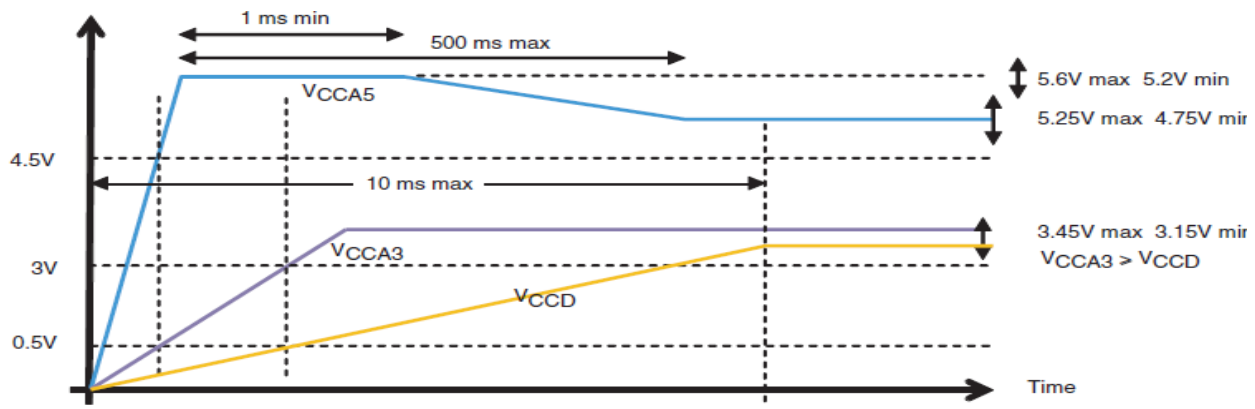


FIGURE 7. Power up sequence

Die thermal characteristics:

- Die thickness = 300µm
- No convection
- Pure conduction
- No radiation

Ci-CGA255 Package

- Rth Junction -bottom of columns (NTK SCI – 0.89 mm diameter) = 13.8°C/W
- Rthj-top of lid = 19.3°C/W
- Rthj-board (JEDEC JESD51-8) = 17°C/W (board size = 39 x 39 mm, 1.6 mm thickness)

- Assumptions:
- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
- Rth-j-a (JEDEC) = 29.5°C/W (board size 114.3 x 76.2 mm, 1.6 mm thickness)

CCGA255 Package

- Rth Junction -bottom of columns (Six Sigma Columns – 0.51 mm diameter) = 15.0°C/W
- Rthj-top of lid = 22.0°C/W
- Rthj-board (JEDEC JESD51-8) = 18.6°C/W (board size = 39 x 39 mm, 1.6 mm thickness)

- Assumptions:
- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
- Rth-j-a (JEDEC) = 29.4°C/W (board size 114.3 x 76.2 mm, 1.6 mm thickness)

FIGURE 8. Thermal characteristics

4. VERIFICATION

4.1 Sampling and inspection. For device class V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device class V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.2.2 Deviation/addition from MIL-PRF-38535.

a. “Nondestructive bond pull test” (TM 2023) is replaced by “Destructive bond pull test” (TM 2011) monitoring.

b. “Constant acceleration” (TM 2001) is deleted from screening. Group D4 shall be applied on each assembly lot.

c. “Reverse Bias Burn-in” is not applicable on technology use for EV10DS130A product (200GHz SiGe Bipolar). However,100% Static burn-in shall be performed in accordance with MIL-PRF-38535.

d. Burn-in is performed at T_A=105°C that gives a T_J= ~156°C in LGA packages and estimated case temperature during burn-in and HTOL is Tc = T_A burn-in (105°C) + 21°C => Tc = ~126°C

4.3 Qualification inspection for device class V. Qualification inspection for device class V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1, 2, 3, 7, 8A, 8B, 9, 10,1 1 1/	1,2,3,7,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Dynamic burn-in (method 1015)	Required	Required
4	Final electrical parameters	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1,2,3,7,8A,8B,9, 10,11 1/
5	Group A test requirements 3/	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8A, 8B, 9, 10, 11
6	Group C end-point electrical parameters 3/	1, 2, 3, 7, 8A, 8B, 9, 10, 11 2/	1,2,3,7,8A,8B, 9,10,11 2/
7	Group D end-point electrical parameters 4/	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B
8	Group E end-point electrical parameters 3/	-	-
9	Column attach 5/	1, 7, 9	1, 7, 9

1/ Indicates PDA applies to subgroup 1 and 7.
2/ For device class V, performance of delta limits shall be specified in table IIB.
3/ LGA packages only
4/ LGA package for all tests, plus CGA device for Column Pull and Salt Atmosphere.
5/ Solderability test shall be performed in accordance with TM 2003.

Table IIB. Burn-in delta drift limits at +25ºC. 1/ 2/

Test description	**Test Symbol**	**Test limits**		**Units**
		Low	High	
Full Scale Measurement with typical gain	Full-Scale_GA_Typ	-2	2	%
Power Consumption at Maximum Power Supplies	I_{VCCA5}_Mux4:1	-5	5	%
	I_{VCCA3}_Mux4:1	-5	5	%
	I_{VCCD}_Mux4:1	-5	5	%
Flags STVF and HTVF levels and functional verification	VOL_STVF	-5	5	%
	VOH_STVF	-5	5	%

1/ These parameters shall be recorded before and after the required burn-in to determine delta limits.

2/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall be as per the corresponding test defined in TABLE I. The drift value shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in Table IIA herein.

a. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM Standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0º ≤ angle ≤ 60º). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b.. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25ºC ±10ºC for single event upset testing and at the maximum rated operating temperature ±10ºC for single event upset testing.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device class V Packing is not individual: Devices are packed within trays.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device class V. Sources of supply for device class V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 CGA packages lead finish: Microcircuits devices for column grid array (CGA) packages are supplying to this drawing with terminal lead finish mark “F”. However, terminal lead finish F is tin (Sn) and lead (Pb) alloy with copper spiral column, and solder column material contains compositions of Sn= 20% and Pb=80% and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-08-20

Approved sources of supply for SMD 5962-15221 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1522101VXC	F8385	EV10DS130AMLG-V
5962-1522101VYF	F8385	EV10DS130AMGS-V
5962-1522101VZF	F8385	EV10DS130AMGC-V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8385	e2V Semiconductors Avenue De Rochepleine BP 123 Saint Egreve CEDEX 38521, France.

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.