REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02 with a temperature range of -55°C to +115°C. - ro	17-01-12	C. SAFFLE
B	Add "L" dimension limits to Figure 1. - ro	18-04-18	C. SAFFLE
C	Under paragraph 1.4, delete Ambient operating temperature range (T_A) and replace with Junction temperature range (T_J). Add last sentence to footnote 1/ as specified under Table I.- ro	19-05-08	C. SAFFLE
D	Make changes to case outline X inch conversion dimensions as specified under Figure 1. - ro	19-09-18	J. ESCHMEYER

REV																				
SHEET																				
REV	D	D	D																	
SHEET	15	16	17																	

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
16-04-12

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL-LINEAR, 32 BIT ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-14231**

SHEET 1 OF 17

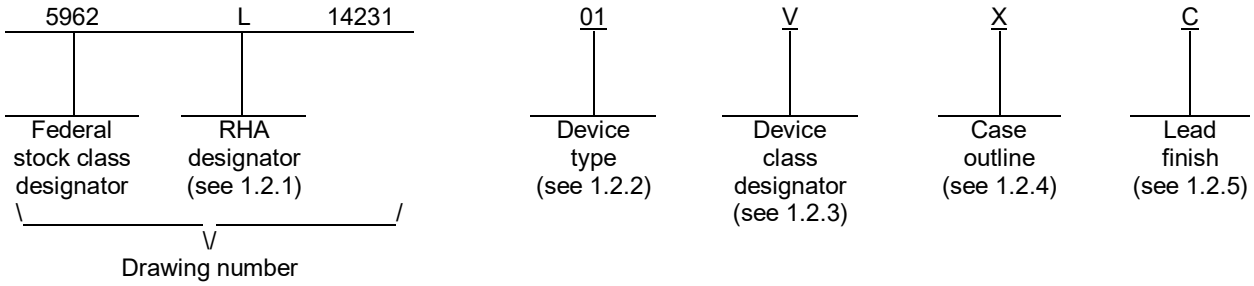
DSCC FORM 2233
APR 97

5962-E380-19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Temperature range	Circuit function
01	ADS1282-RHA	-55°C to +125°C	32 bit analog to digital converter
02	ADS1282-RHA	-55°C to +115°C	32 bit analog to digital converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	28	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Analog positive supply voltage (AVDD) to Analog negative supply voltage (AVSS) ..... -0.3 V to 5.5 V
AVSS to Digital ground (DGND) ..... -2.8 V to 0.3 V
Digital positive supply voltage (DVDD) to DGND ..... -0.3 V to 3.9 V
Input current :
  Momentary ..... 100 mA maximum
  Continuous ..... 10 mA maximum
Analog input voltage ..... AVSS – 0.3 V to AVDD + 0.3 V
Digital input voltage to DGND ..... -0.3 V to DVDD + 0.3 V
Power dissipation (P_D) ..... 41 mW
Maximum junction temperature (T_J) :
  Device type 01 ..... -55°C to +125°C
  Device type 02 ..... -55°C to +115°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Storage temperature range ..... -60°C to +150°C

1.4 Recommended operating conditions.

AVDD ..... 2.5 V
AVSS ..... -2.5 V
Junction temperature range (T_J) :
  Device type 01 ..... -55°C to +125°C
  Device type 02 ..... -55°C to +115°C

1.5 Radiation features.

Maximum total dose available (dose rate = 10 mrads(Si)/s) ..... 50 krads(Si) 2/

1.6 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(BOTTOM)}$	5.22	°C/W

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 50 krads(Si).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Analog inputs section.							
Absolute input range		AIMNP or AINN	1,2,3	01, 02	AVSS + 0.7	AVDD – 1.25	V
PGA output (CAPP, CAPN) section.							
Absolute output range			1,2,3	01, 02	AVSS + 0.4	AVDD – 0.4	V
External bypass capacitance			4,5,6	01, 02		100	nF
AC performance section.							
Signal to noise ratio 4/	SNR	High resolution mode	4,5,6	01, 02	112		dB
Total harmonic distortion	THD	High resolution, PGA = 1…16	4,5,6	01		-99	dB
				02		-101	
		High resolution, PGA = 32		01		-90	
				02		-92	
DC performance section.							
Resolution		No missing codes	4,5,6	01, 02	31		Bits
Data rate	fDATA	FIR filter mode	4,5,6	01, 02	250	4000	SPS
		Sinc filter mode			8000	128,000	
Integral nonlinearity 5/	INL	Differential input	4,5,6	01, 02		0.0090	%FSR
		M,D,P,L	4			0.0170	6/
Offset error		Shorted input	1,2,3	01, 02		200	µV
		M,D,P,L	1			750	
Gain error 7/		High resolution mode	4,5,6	01, 02	-1.5	-0.5	%
Gain matching 8/			4,5,6	01, 02		0.8	%
Common mode rejection	CMR	f_{CM} = 60 Hz 9/	4,5,6	01, 02	82		dB
Power supply rejection	PSR	AVDD, AVSS, f_{PS} = 60 Hz 9/	4,5,6	01, 02	80		dB
		M,D,P,L	4		64		
		DVDD, f_{PS} = 60 Hz 9/	4,5,6		90		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Voltage reference inputs.							
Reference input voltage		(V_{REF} = VREFP – VREFN)	1,2,3	01, 02	0.5	(AVDD – AVSS) + 0.2	V
Negative reference input	VREFN		1,2,3	01, 02	AVSS – 0.1	VREF – 0.5	V
Positive reference input	VREFP		1,2,3	01, 02	VREFN + 0.5	AVDD + 0.1	V
Digital filter response section.							
Passband ripple			4,5,6	01, 02		±0.003	dB
High pass filter corner			4,5,6	01, 02	0.1	10	Hz
Stop band attenuation 10/			4,5,6	01, 02	135		dB
Digital input/output section.							
High input voltage	V_{IH}		1,2,3	01, 02	0.8 x DVDD	DVDD	V
Low input voltage	V_{IL}		1,2,3	01, 02	DGND	0.2 x DVDD	V
High output voltage	V_{OH}	I_{OH} = 1 mA	1,2,3	01, 02	0.8 x DVDD		V
Low output voltage	V_{OL}	I_{OL} = 1 mA	1,2,3	01, 02		0.2 x DVDD	V
Input leakage current	I_{IL}, I_{IH}	$0 < V_{DIGITAL\ IN} <$ DVDD	1,2,3	01, 02		±10	µA
Clock input	f_{CLK}		4,5,6	01, 02	1	4.096	MHz
Serial clock rate	f_{SCLK}		4,5,6	01, 02		$f_{CLK}/2$	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply section.		See figure 5.					
Analog negative supply voltage	AVSS		1,2,3	01, 02	-2.6	0	V
Analog positive supply voltage	AVDD		1,2,3	01, 02	AVSS + 4.75	AVSS + 5.25	V
Digital positive supply voltage	DVDD		1,2,3	01, 02	1.75	3.6	V
Analog positive and negative supply current	AVDD, AVSS	High resolution mode	1,2,3	01		7.2	mA
				02		6.5	
		M,D,P,L	1	01, 02		11	
		Power down mode	1,2,3	01, 02		0.2	
		M,D,P,L	1			5	
		Standby mode	1,2,3	01, 02		0.2	
		M,D,P,L	1			5	
Digital positive and negative supply current	DVDD	High resolution mode	1,2,3	01		1.5	mA
				02		1.2	
		Standby mode		01, 02		0.175	
		Power down mode 11/		01, 02		0.120	
Power dissipation	P_D	High resolution mode	1,2,3	01, 02		41	mW
		M,D,P,L	1			60	
		Power down mode	1,2,3			1.4	
		M,D,P,L	1			25.4	
		Standby mode	1,2,3			1.6	
		M,D,P,L	1			25.5	
Timing requirements section.		See figure 6.					
SCLK period	t_{SCLK}		9,10,11	01, 02	2	16	$1/f_{CLK}$
SCLK pulse width, high 12/ and low	t_{SPWH}, t_{SPWL}		9,10,11	01, 02	0.8	10	$1/f_{CLK}$
DIN valid to SCLK rising edge: setup time	t_{DIST}		9,10,11	01, 02	50		ns
Valid DIN to SCLK rising edge: hold time	t_{DIHD}		9,10,11	01, 02	50		ns
SCLK falling edge to valid 13/ new DOUT: propagation delay	t_{DOPD}		9,10,11	01, 02		100	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing requirements section - continued.		See figure 6.					
SCLK falling edge to DOUT invalid: hold time	t_{DOHD}		9,10,11	01, 02	0		ns
Final SCLK rising edge of command to first SCLK rising edge for register read/write data	t_{SCDL}		9,10,11	01, 02	24		1/fCLK

1/ Unless otherwise specified, over operating temperature range, AVDD = 2.5 V, AVSS = -2.5 V, system clock (f_{CLK}) = 4.096 MHz, VREFP = 2.5 V, VREFN = -2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 samples per second (SPS). For production testing of these parameters to the limits in table I herein, Ambient temperature (T_A) = Junction temperature (T_J).

2/ Device types 01 and 02 supplied to this drawing have been characterized through all levels P and L of irradiation. However, this device is only tested at the "L" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see1.5 herein).

3/ The manufacturer supplying RHA device types 01 and 02 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1. The radiation end point limits for the conditions are as specified in MIL-STD-883, method 1019, condition D to a maximum total dose of 50 krad(Si).

4/ V_{IN} = 20 mVDC / PGA, see figure 4.

5/ Best fit method.

6/ FSR: full scale range = $\pm V_{REF}$ / (2 x PGA).

7/ The PGA output impedance and the modulator input impedance results in -1% systematic gain error (high resolution mode).

8/ Gain match relative to PGA = 1.

9/ f_{CM} is the input common mode frequency. f_{PS} is the power supply frequency.

10/ Input frequencies in the range of $Nf_{CLK}/512 \pm f_{DATA}/2$ (N = 1, 2, 3..) can mix with the modulator chopping clock. In these frequency ranges intermodulation = 120 dB nominal.

11/ CLK input stopped.

12/ Holding SCLK low for 64 $\overline{DRDY}$ falling edges resets the serial interface.

13/ Load on DOUT = 20 pF||100 kΩ.

Case X

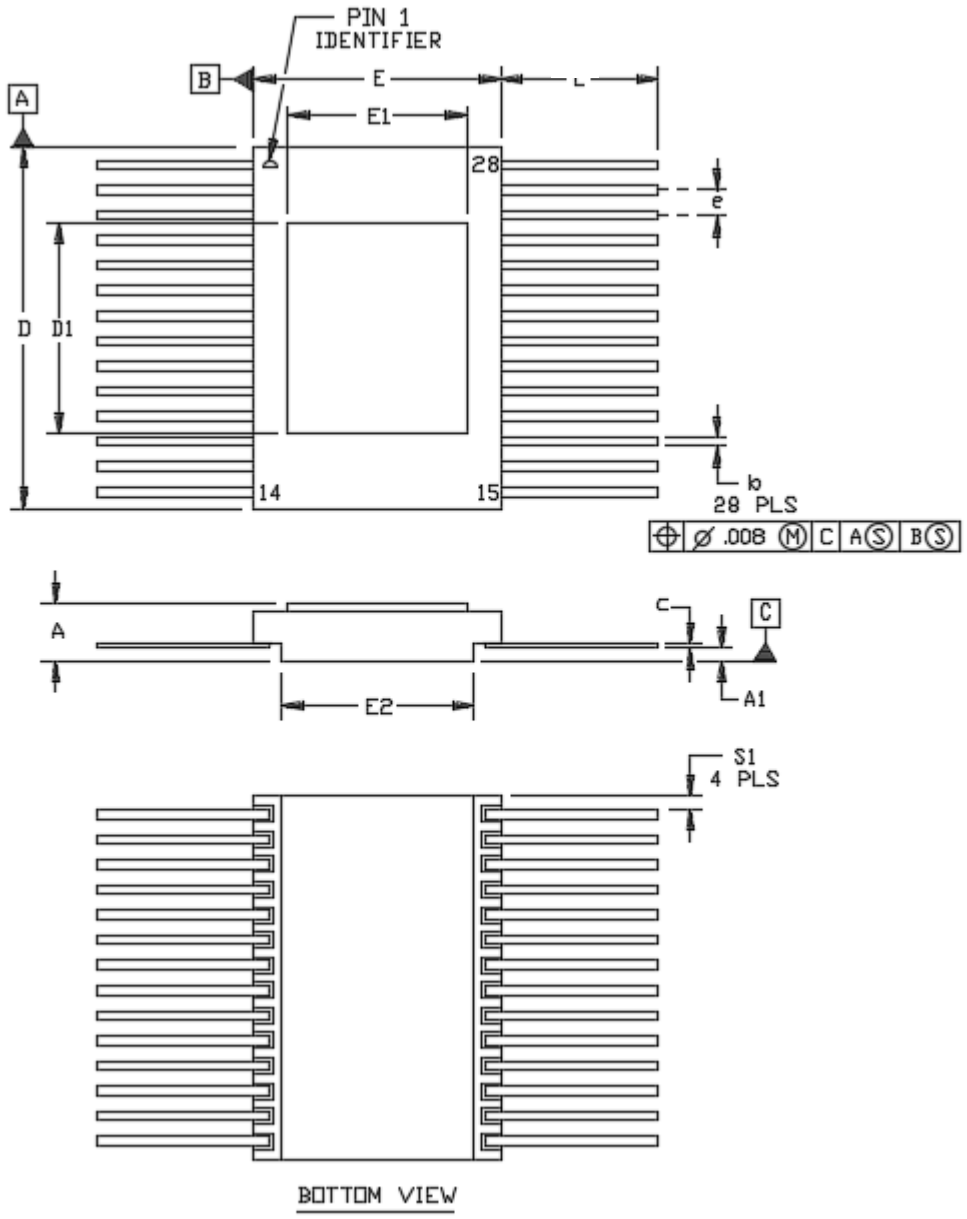


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.112	---	2.85
A1	.026	---	0.66	---
b	.015	.021	0.38	0.53
c	.004	.009	0.10	0.23
D	.712	.728	18.08	18.49
D1	.425 REF		10.795 REF	
E	.492	.508	12.5	12.9
E1	.355 REF		9.017 REF	
E2	.372	.388	9.45	9.86
e	.050 BSC		1.27 BSC	
L	.250	.370	6.35	9.40
S1	.010	---	0.25	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid.
3. The terminal are gold plated.

FIGURE 1. Case outline - continued.

Device types	01, 02	
Case outline	X	
Terminal number	Terminal symbol	Description
1	CLK	Master clock input.
2	SCLK	Serial clock input.
3	$\overline{\text{DRDY}}$	Data ready output: read data on falling edge.
4	DOUT	Serial data output.
5	DIN	Serial data input.
6	DGND	Digital ground, pin 12 is the key ground point.
7	MCLK	Modulator clock output, if in modulator mode: MCLK: modulator clock output. Otherwise, the pin is an unused input (must be tied).
8	M1	Modulator data output 1; if in modulator mode: M1: modulator data output 1. Otherwise, the pin is an unused input (must be tied)."
9	M0	Modulator data output 0; if in modulator mode: M0: modulator data output 0. Otherwise, the pin is an unused input (must be tied)."
10	SYNC	Synchronize input.
11	MFLAG	Modulator over range flag: 0 = normal, 1 = modulator over-range.
12	DGND	Digital ground, pin 12 is the key ground point.
13	CAPN	PGA outputs: Connect 10 nF capacitor from CAPP to CAPN.
14	CAPP	PGA outputs: Connect 10 nF capacitor from CAPP to CAPN.
15	AINP2	Positive analog input 2.
16	AINN2	Negative analog input 2.
17	AINP1	Positive analog input 1.
18	AINN1	Negative analog input 1.
19	AVDD	Positive analog power supply.
20	AVSS	Negative analog power supply.
21	VREFN	Negative reference input.
22	VREFP	Positive reference input.
23	$\overline{\text{PWDN}}$	Power-down input, active low.
24	$\overline{\text{RESET}}$	Reset input, active low.
25	DGND	Digital ground, pin 12 is the key ground point.
26	DVDD	Digital power supply: 1.8 V to 3.3 V.
27	DGND	Digital ground, pin 12 is the key ground point.
28	BYPASS	Sub regulator output: connect 1 μF capacitor to DGND.

FIGURE 2. Terminal connections.

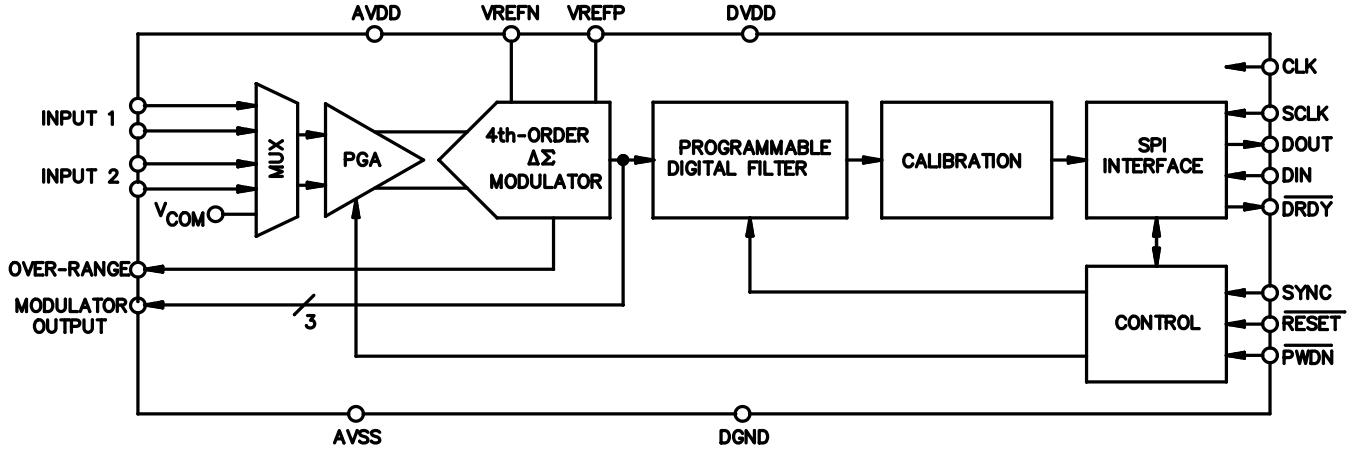
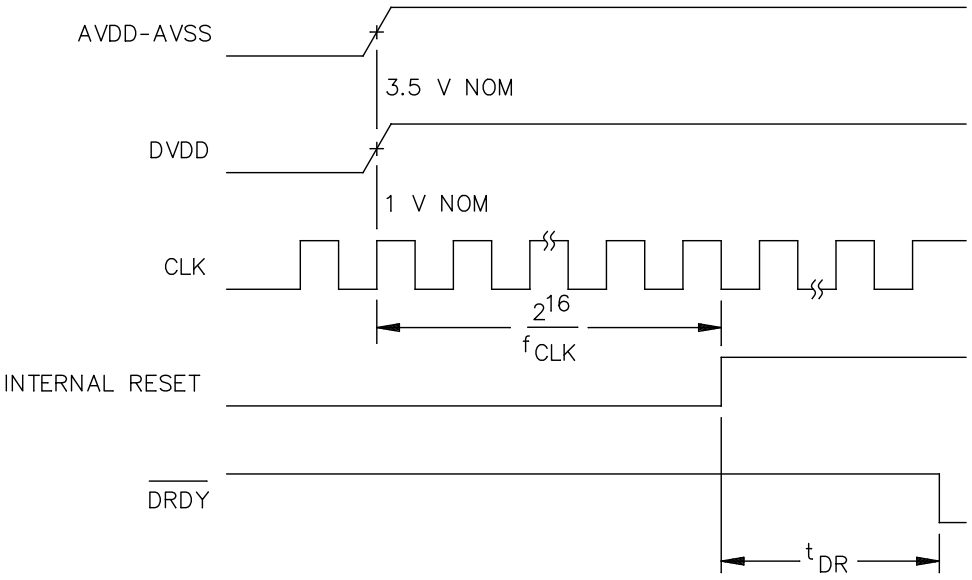


FIGURE 3. Block diagram.

Data rate	PGA (High resolution mode) 1/						
(SPS)	1	2	4	8	16	32	64
250	130	130	129	128	125	119	114
500	127	127	126	125	122	116	111
1000	124	124	123	122	119	113	108
2000	121	121	120	119	116	111	106
4000	118	118	117	116	113	108	103

1/ V_{IN} = 20 mV dc / PGA.

FIGUIRE 4. Signal to noise ratio (dB).



This device has three power supplies: AVDD, AVSS, and DVDD. Figure 5 shows the power on sequence of the device. The power supplies can be sequenced in any order. The supplies [the difference of (AVDD – AVSS) and DVDD] generate an internal reset whose outputs are summed to generate a global internal rest. After the supplies have crossed the minimum threshold, 2^{16} f_{CLK} cycles are counted before releasing the internal rest. After the internal reset is released, new conversion data are available, as shown in figure 5 and Table III.

FIGUIRE 5. Power on.

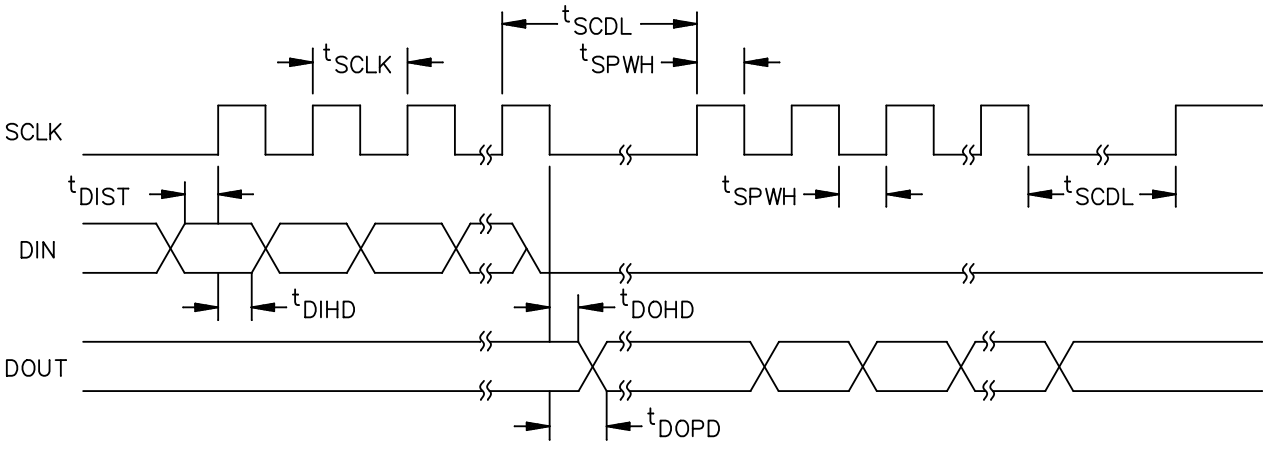


FIGURE 6. Timing diagram.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,9	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4,5,6, 1/ 2/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 2/ 9,10,11
Group D end-point electrical parameters (see 4.4)	1,4,9	1,4,9
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Conditions	Delta limits	Units
AVDD current	High resolution mode	±50	µA
AVSS current	High resolution mode	±50	µA
DVDD current	High resolution mode	±50	µA
AVDD current	Standby mode	±1	µA
AVSS current	Standby mode	±1	µA
DVDD current	Standby mode	±7.5	µA
AVDD current	Power down mode	±1	µA
AVSS current	Power down mode	±1	µA
DVDD current	Power down mode	±1	µA
I_{IL}, I_{IH} CLK	Input leakage	±0.2	µA
I_{IL}, I_{IH} SCLK	Input leakage	±0.2	µA
I_{IL}, I_{IH} PWDN	Input leakage	±0.2	µA

1/ These parameters shall be recorded before and after the required burn in and life test to determine delta limits.

TABLE III. Power on, power down input pin, and wake up command timing for new data.

Parameter	Description		Filter mode
Time for data ready (t_{DR})	Time for data ready 216 CLK cycles after power on; and new data ready after $\overline{PWDN}$	See Table IV.	SINC 1/
		62.98046875/f_{DATA} + 468/f_{CLK} 2/	FIR

1/ Supply power on and $\overline{PWDN}$ pin default is 1000 SPS FIR.

2/ Subtract two CLK cycles for the wake up command. The wake up command is timed from the next rising edge of CLK to after the eighth rising edge of $\overline{SCLK}$ during command to DRDY falling.

TABLE IV. Time for data ready (sinc filter).

f_{DATA}	f_{CLK} 1/
128 k	440
64 k	616
32 k	968
16 k	1672
8 k	2824

1/ For SYNC and wake up commands, f_{CLK} = number of CLK cycles from next rising CLK edge directly after eighth rising $\overline{SCLK}$ edge to DRDY falling edge. For wake up command only, subtract two f_{CLK} cycles.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-09-18

Approved sources of supply for SMD 5962-14231 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Temperature range	Vendor similar PIN 2/
5962L1423101VXC	01295	-55°C to +125°C	ADS1282-RHA
5962L1423102VXC	01295	-55°C to +115°C	ADS1282-RHA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243