REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add paragraphs 1.5, 4.4.4.1, and 4.4.4.2 for radiation hardened requirements. Make change to Input voltage Enable (EN) maximum limit as specified under paragraph 1.3 by deleting “6.5 V” and replacing with “3.6 V”. Delete Peak output current and Power good (PGOOD) pin sink current parameters as specified under paragraph 1.3. Delete footnote under paragraph 1.6. Make change to the Shutdown parameter unit symbol as specified under Table I by deleting “µA” and replacing with “mA”. Add note to AGND terminal description as specified under Figure 1. Add static burn-in to Table IIA. Add subgroup 1 to Group E endpoint parameters under Table IIA. - ro	16-06-21	C. SAFFLE
B	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	21-06-25	J. ESCHMEYER
C	Make change to the conditions column for “Shutdown current”, “VTTREF source current limit”, and “VTTREF sink current limit” tests as specified under Table I. Make change to symbol column to “Supply current VLDOIN”, “Shutdown current VLDOIN” tests as specified under Table I. Make change to “Output dc voltage, VO” test as specified under Table I. Make correction to the “Output DC voltage (VO)” limit under Table IIB. Make changes to dimension A and Q as specified under Figure 1. - ro	23-01-05	J. ESCHMEYER
D	Add device type 02, device class P requirements. Add case outline Y. Delete paragraph 1.6 and move the limits to paragraph 1.3. Add Glass transition temperature information to paragraph 1.4 - ro.	23-12-18	J. ESCHMEYER

Revision Status of Sheets

REV	D	D	D	D	D																	
SHEET	23	24	25	26	27																	
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
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DRAWING APPROVAL DATE
16-04-15

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, LINEAR, SINK/SOURCE DDR TERMINATION VOLTAGE REGULATOR, MONOLITHIC SILICON

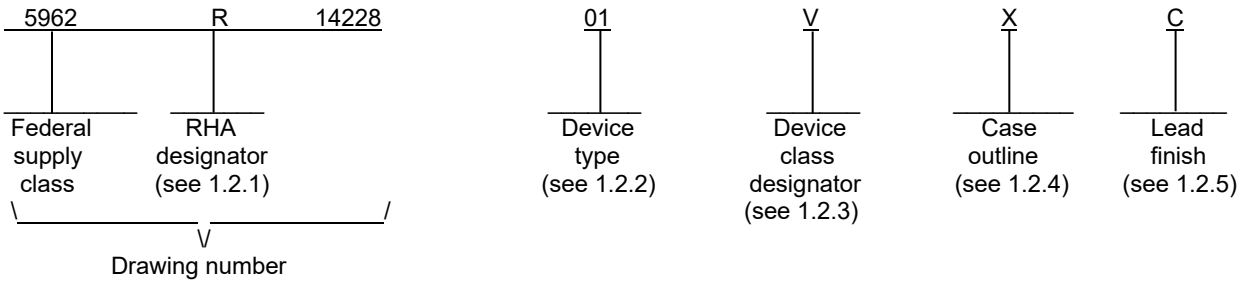
AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-14228**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing documents product assurance class levels consisting of high reliability (device class Q), space application (device class V or Y), and plastic encapsulated microcircuits (PEM) (device class N) for military, terrestrial and avionics application and device class P for space application. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device classes N and P, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. RHA marked devices classes are N, P, Q, Y, and V and meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TPS7H3301-SP	Sink/source double data rate (DDR) termination voltage regulator
02	TPS7H3302-SP (QMLP)	Sink/source double data rate (DDR) termination voltage regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N or P	Certification and qualification to MIL-PRF-38535 for PEM performance environments.
Q or V	Certification and qualification to MIL-PRF-38535
Y	Certification and qualification to MIL-PRF-38535. Non hermetic flip chip technology on a ceramic or organic substrate.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	16	Flat pack
Y	See figure 1	32	Thermally enhanced thin shrink small outline package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, P, Q, Y, and V.

1.3 Absolute maximum ratings. 1/

Input voltage: 2/	
Supply voltage (V_{DD}) /input voltage (V_{IN}), supply voltage for low dropout regulator (VLDOIN), remote sensing (VTTSNS), sense input (VDDQSNS)	-0.36 V to 3.6 V
Enable (EN)	-0.3 V to 3.6 V
Signal ground (PGND) to ground (AGND)	-0.3 V to 0.3 V
Output voltage: 2/	
Output voltage (VO/VTT), reference output (VTTREF)	-0.3 V to 3.6 V
Power good (PGOOD)	-0.3 V to 3.6 V
Maximum operating junction temperature (T_J)	-55°C to +150°C
Storage temperature range	-55°C to +150°C
Lead temperature (soldering, 10 seconds) for device type 01	+300°C
Thermal characteristics:	
Case X:	
Thermal resistance, junction to case (bottom) $\theta_{JC(BOT)}$	0.6°C/W 3/ 4/
Case Y:	
Junction to ambient thermal resistance (θ_{JA})	25.9°C/W
Junction to case (top) thermal resistance ($\theta_{JC(TOP)}$)	15.9°C/W
Junction to board thermal resistance (θ_{JB})	7.9°C/W
Junction to top characterization parameter (Ψ_{JT})	0.2°C/W
Junction to board characterization parameter (Ψ_{JB})	7.9°C/W
Junction to case (bottom) thermal resistance ($\theta_{JC(BOT)}$)	1.1°C/W
Electrostatic discharge (ESD) ratings:	
Human body model (HBM)	-4,000 V to +4, 000 V 5/
Charged device model (CDM)	-750 V to +750 V 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltage values are with respect to AGND.

3/ For device type 01, do not allow package body temperature to exceed 265°C at any time or permanent damage may result.

4/ Maximum power dissipation may be limited by overcurrent protection.

5/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6/ JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

1.4 Recommended operating conditions.

Input voltages :

V_{IN} / V_{DD}	2.375 V to 3.5 V
VDDQSNS	1.0 V to 3.5 V
VLDOIN	0.9 V to 3.5 V
EN, VTTSNS, PGOOD	-0.1 V to 3.5 V
PGND	-0.1 V to 0.1 V
Ouput voltages :	
VO/VTT	-0.1 V to 3.5 V
VTTREF	-0.1 V to 1.8 V
Device type 02 only:	
Input current:	
PGOOD	0 mA to 4 mA
Ouput current :	
VTT	-3 A to 3 A
VTTREF	-0.01 A to 0.01 A
Operating junction temperature (T_J)	-55°C to +125°C
Ambient operating temperature range (T_A)	-55°C to +125°C
Glass transition temperature:	
Mold compound (Tg)	+115°C 7/

1.5 Radiation features.

Maximum total ionizing dose available (dose rate = 50 – 300 rads(Si)/s)	100 krads(Si) 8/
Maximum total ionizing dose available (dose rate = 10 mrads(Si)/s)	100 krads(Si) 8/
Device type 02 only:	
Single event phenomenon (SEP):	
No SEL occurs at effective linear energy transfer (LET) (see 4.3)	≤ 70 MeV/(mg/cm^2) 9/
No SEB observe at effective LET (see 4.3)	≤ 70 MeV/(mg/cm^2) 9/
No SEGR observe at effective LET (see 4.3)	≤ 70 MeV/(mg/cm^2) 9/
Neutron/displacement irradiation damaged test (1 MeV equivalent)	= 1 x 10^{13} n/cm^2 10/

7/ Glass transition temperature (Tg) of mold compound measured specification value 115°C but, tested Tg is +135°C.

8/ The manufacturer supplying device types 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krads(Si). However device type 02 supplied to this drawing has been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019 to TID level 100 krads(Si). For more information on TID test please contact device manufacturer.

9/ The heavy-ion test performed at TAMU cyclotron radiation effects facility. Holmium (^{165}Ho) ion beam were used at an angle of incidence of 0° at flux of 10^5 ions/cm^2·s, fluences level of 10^7 ions/cm^2 and a temperature of 125°C and no single event latch-up (SEL) was observed at effective LET of 75 MeV/(mg/cm^2). Manufacturer also test Single event burnout (SEB) and Single event gate rupture (SEGR) test with (^{165}Ho) ion beam were used at angles of incidence of 0°. No SEB/SEGR observed up to effective LET of 75 MeV/(mg/cm^2). For more information on SEE/SEP test please contact device manufacturer.

10/ Neutron Displacement damaged dosimetry test was performed in Fast Neutron Irradiation (FNI) facility of The University of Massachusetts Lowell. The results show that all devices were fully functional and within production test limits after having been irradiated up to 1 x 10^{13} n/cm^2 (1-MeV equivalent). A sample size of nine units was exposed to radiation testing per MIL-STD-883, Method 1017 for Neutron Irradiation, and an additional one device was used as a control unit and was not irradiated.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at https://www.astm.org/.)

JEDEC Solid State Technology Association

JEDEC JESD57 – Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Radiation.
JEDEC JEP 155 - Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157 - Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https:/www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, P, Q, Y, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

Marking for case outline Y :
If any additional information is needed, contact the manufacturer.

\T/ YMLLLLSG4
R1422802PY
O Q MLA NNNN

O – PIN 1

\T/	TI Logo
YM	Year month date code
LLLL	Assembly lot code
S	Assembly site code per QSS 005-120
TAI	Country
Q	QML
MLA	Country
NNNN	Serial number, 4 digit

MAXIMUM CHARACTERS:
8 CHARACTERS – 1ST LINE
10 CHARACTERS – 2ND LINE

#Symbol device name:	R1422802PY
#Symbol ECAT: G4 must be symbolized with a solid line underscore	

3.5.1 Certification/compliance mark. The certification mark for device classes N, P, Q, Y, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current.							
Supply / quiescent current	$I_{VDD/VIN}$	EN = 3.3 V, no load	1,2,3	01, 02		30	mA
Shutdown current	$I_{VDD(SDN)}$	EN = 0 V, VDDQSNS = 0 V, no load	1,2,3	01		5	mA
		EN = 0 V, VDDQSNS > 0.78 V, no load				8	
	$I_{VDD(SHDN)}$	EN = 0 V, VDDQSNS = 0 V, no load		02		3	
		EN = 0 V, VDDQSNS > 0.78 V, no load				6	
Supply / quiescent current of VLDOIN	I_{VLDOIN}	EN = 3.3 V, no load	1,2,3	01		1200	µA
Shutdown current of VLDOIN	$I_{VLDOIN(SDN)}$	EN = 0 V, no load	1,2,3	01		100	µA
	$I_{VLDOIN(SHDN)}$	EN = 0 V, no load		02		1	
VDDQSNS input current	$I_{VDDQSNS}$	EN = 3.3 V	1,2,3	01, 02		6	µA
VO / VTT output.							
Output dc voltage, V_{TT}/V_O	VVTTSNS	V_{LDOIN} = 2.5 V, VVTTREF = 1.25 V (DDR1), $I_{VTT/VO}$ = 0 A	1,2,3	01	1.244	1.256	V
		V_{LDOIN} = 1.8 V, VVTTREF = 0.9 V (DDR2), $I_{VTT/VO}$ = 0 A			0.894	0.906	
		V_{LDOIN} = 1.5 V, VVTTREF = 0.75 V (DDR3), $I_{VTT/VO}$ = 0 A			0.744	0.756	
		V_{LDOIN} = 1.35 V, VVTTREF = 0.675 V (DDR3L), $I_{VTT/VO}$ = 0 A			0.669	0.681	
		V_{LDOIN} = 1.20 V, VVTTREF = 0.60 V (DDR4), $I_{VTT/VO}$ = 0 A			0.594	0.606	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VO / VTT output – continued.							
Output dc voltage, V_{TT}/V_O	V_{VTTSNS}	VDDQSNS = VLDOIN = 2.5 V (DDR1), I_{VTT} = 5 mA	1,2,3	02	1.24	1.26	mV
		VDDQSNS = VLDOIN = 1.8 V (DDR2), I_{VTT} = 5 mA			0.89	0.91	
		VDDQSNS = VLDOIN = 1.5 V (DDR3), I_{VTT} = 5 mA			0.745	0.759	
		VDDQSNS = VLDOIN = 1.35 V (DDR3L), I_{VTT} = 5 mA			0.67	0.684	
		VDDQSNS = VLDOIN = 1.2 V (DDR4), I_{VTT} = 5 mA			0.596	0.608	
		VDDQSNS = VLDOIN = 2.5 V (DDR1), I_{VTT} = -5 mA			1.25	1.27	
		VDDQSNS = VLDOIN = 1.8 V (DDR2), I_{VTT} = -5 mA			0.9	0.92	
		VDDQSNS = VLDOIN = 1.5 V (DDR3), I_{VTT} = -5 mA			0.752	0.768	
		VDDQSNS = VLDOIN = 1.35 V (DDR3L), I_{VTT} = -5 mA			0.675	0.692	
		VDDQSNS = VLDOIN = 1.2 V (DDR4), I_{VTT} = -5 mA			0.602	0.618	
		VDDQSNS = VLDOIN = 2.5 V (DDR1), $-1\ A \le I_{VTT} \le 1\ A$			1.24	1.28	
		VDDQSNS = VLDOIN = 1.8 V (DDR2), $-1\ A \le I_{VTT} \le 1\ A$			0.885	0.93	
		VDDQSNS = VLDOIN = 1.5 V (DDR3), $-1\ A \le I_{VTT} \le 1\ A$			0.735	0.78	
		VDDQSNS = VLDOIN = 1.35 V (DDR3L), $-1\ A \le I_{VTT} \le 1\ A$			0.66	0.72	
		VDDQSNS = VLDOIN = 1.2 V (DDR4), $-1\ A \le I_{VTT} \le 1\ A$			0.585	0.63	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VO / VTT output – continued .							
V_{LODIN} - $V_{TT/VO}$ 5/	V_{LODIN} > $V_{TT/VO}$	V_{IN}/V_{DD} = 2.95 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 2.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1)	1,2,3	01		230	mV
		V_{IN}/V_{DD} = 2.95 V, I_O = 1 A, $V_{VDDQSNS}$ = 2.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1)				300	
		V_{IN}/V_{DD} = 2.95 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 2.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1)				400	
		V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, 4/ $V_{VDDQSNS}$ = 1.80 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2)				230	
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, 4/ $V_{VDDQSNS}$ = 1.80 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.80 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2)				400	
		V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 1.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3)				230	
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, $V_{VDDQSNS}$ = 1.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3)				400	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VO / VTT output – continued.							
$V_{LODIN} > V_{TT/VO}$ 5/	$V_{LODIN} > V_{TT/VO}$	V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 1.35 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3L)	1,2,3	01		230	mV
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, $V_{VDDQSNS}$ = 1.35 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3L)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.35 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR3L)				400	
		V_{IN}/V_{DD} = 2.375 V, I_O = 0.5 A, $V_{VDDQSNS}$ = 1.20 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR4)				230	
		V_{IN}/V_{DD} = 2.375 V, I_O = 1 A, $V_{VDDQSNS}$ = 1.20 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR4)				300	
		V_{IN}/V_{DD} = 2.375 V, I_O = 2.0 A, 4/ $V_{VDDQSNS}$ = 1.20 V, $V_{TT} = V_{VTTREF}$ – 50 mV (DDR4)				400	
Output voltage tolerance to VTTREF	V_{VOTOL}/ V_{TTTOL}	I_{VO} = -3 A, 4/ across VDD / V_{IN} voltage range	1,2,3	01	12	34	mV
		I_{VO} = 3 A, 4/ across VDD / V_{IN} voltage range			-12	-34	
VO/VTT source current limit	I_{VOSRCL}	With reference to V_{VTTREF}, V_{VTTSNS} = 90% x V_{VTTREF}	1,2,3	01	3.25	8	A
VO/VTT sink current limit	I_{VOSNCL}	With reference to V_{VTTREF}, V_{VTTSNS} = 110% x V_{VTTREF}	1,2,3	01	3.5	5.5	A
Discharge impedance	RDSCHRG	V_{DDQSNS} = 0 V, V_{VO}= 0.3 V, V_{EN} = 0 V, T_A = +25C	1	01		25	Ω

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VO / VTT output – continued.							
Dropout voltage, V_{DO} = VLDOIN – VTTREF V_{DO} recorded when VTT – VTTREF = 50 mV	VDO	VDDQSNS = 2.5 V (DDR1), I_{VTT} = 0.5 A	1,2,3	02		60	mV
		VDDQSNS = 2.5 V (DDR1), I_{VTT} = 1 A				180	
		VDDQSNS = 2.5 V (DDR1), I_{VTT} = 2 A				465	
		VDDQSNS = 1.8 V (DDR2), I_{VTT} = 0.5 A				70	
		VDDQSNS = 1.8 V (DDR2), I_{VTT} = 1 A				200	
		VDDQSNS = 1.8 V (DDR2), I_{VTT} = 2 A				475	
		VDDQSNS = 1.5 V (DDR3), I_{VTT} = 0.5 A				65	
		VDDQSNS = 1.5 V (DDR3), I_{VTT} = 1 mA				180	
		VDDQSNS = 1.5 V (DDR3), I_{VTT} = 2 A				420	
		VDDQSNS = 1.35 V (DDR3L), I_{VTT} = 0.5 A				60	
		VDDQSNS = 1.35 V (DDR3L), I_{VTT} = 1 A				180	
		VDDQSNS = 1.35 V (DDR3L), I_{VTT} = 2 A				420	
		VDDQSNS = 1.2 V (DDR4), I_{VTT} = 0.5 A				60	
		VDDQSNS = 1.2 V (DDR4), I_{VTT} = 1 A				180	
		VDDQSNS = 1.2 V (DDR4), I_{VTT} = 2 A				420	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VO / VTT output – continued.							
VTT tolerance to VTTREF (VTT – VTTREF)	V_{TTTOL}	I_{VTT} = -3 A	1,2,3	02	1	30	mV
		I_{VTT} = 3 A			-30	-1	
VTT sourcing current limit	$I_{LIM\_SRC\_VTT}$	Ramp output 0 A to 10 A, record current when VTT reaches lowest value	1,2,3	02	5	9	A
VTT sinking current limit	$I_{LIM\_SNK\_VTT}$	Ramp output 0 A to -10 A, record current when VTT reaches highest value	1,2,3	02	5	10	A
VTT discharge resistance	R_{DSCHRG}	VDDQSNS = 0 V, VTT = 0.3 V, EN = 0 V	1,2,3	02		25	Ω
POWER-GOOD comparator.							
VO/VTT PGOOD threshold	VTH(PG)	PGOOD window lower threshold with respect to V_{VTTREF}	1,2,3	01	-23.5	-17.5	%
		PGOOD window upper threshold with respect to V_{VTTREF}			17.5	23.5	
VTT PGOOD threshold with respect to VTTREF	V_{PG} (LOW, Falling)	PGOOD window low falling threshold	1,2,3	02	-21%	-18%	
	V_{PG} (LOW, Rising)	PGOOD window low rising threshold	1,2,3	02	-17%	-13%	
VTT PGOOD threshold with respect to VTTREF	V_{PG} (HI, Falling)	PGOOD window high falling threshold	1,2,3	02	13%	17%	
	V_{PG} (HI, Rising)	PGOOD window high rising threshold	1,2,3	02	18%	21%	
Output low voltage	$V_{PGOODLOW}$	I_{SINK} = 4 mA	1,2,3	01		0.4	V
Power good output low	$V_{PG(OL)}$	$I_{PGOOD(SINK)}$ = 4 mA	1,2,3	02		0.4	V
Leakage current	IPGOODLK	VTTSNS = VREFIN (PGOOD high impedance), PGOOD = V_{IN} + 0.2 V	1,2,3	01		1	μA
Power good leakage	$I_{PG(LKG)}$	VTTSNS = VTTREF (PGOOD high impedance), PGOOD = VDD + 0.2 V	1,2,3	02		1	μA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V_{DDQSNS} and V_{VTTREF} output.							
V_{DDQSNS} voltage range	V_{DDQSNS_UVLO}		1,2,3	01	1.0	2.8	V
VDDQSNS UVLO turn-on threshold	$VDDQSNS_{UVLO}$	VDDQSNS rising	1,2,3	02		900	mV
VDDQSNS UVLO hysteresis	$VDDQSNS_{UVLO(HYST)}$		1,2,3	02		150	mV
VTTREF voltage tolerance to VDDQSNS	V_{VTTREF}	-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 2.5 V	1,2,3	01	-15	15	mV
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.8 V			-15	15	
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.5 V			-15	15	
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.35 V			-15	15	
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.2 V			-15	15	
VTTREF voltage tolerance to VDDQSNS	V_{VTTREF}	-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 2.5 V	1,2,3	02	49%	51%	mV
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.8 V			49%	51%	
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.5 V			49%	51.25%	
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.35 V			49%	51.5%	
		-10 mA < I_{VTTREF} < 10 mA, VDDQSNS = 1.2 V			49%	51.5%	
		-3 mA < I_{VTTREF} < 3 mA, VDDQSNS = 1.5 V			49%	51%	
		-3 mA < I_{VTTREF} < 3 mA, VDDQSNS = 1.35 V			49%	51%	
		-3 mA < I_{VTTREF} < 3 mA, VDDQSNS = 1.2 V			49%	51%	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V_{DDQSNS} and V_{VTTREF} output – continued.							
VTTREF source current limit	$I_{VTTREFSRCL}$	VTTREF = 0 V	1,2,3	01	10		mA
VTTREF sink current limit	$I_{VTTREFSRCCL}$	VTTREF = 0 V	1,2,3	01	6		mA
VTTREF sourcing current limit	$I_{LIM\_SRC\_VTTREF}$	Sourcing current ramped from 0 to 55 mA. Find when VTTREF drops to half its original value	1,2,3	02	35		mA
VTTREF sinking current limit	$I_{LIM\_SINK\_VTTREF}$	Sinking current ramped from 0 to 16.5 mA. Find when VTTREF hits peak value	1,2,3	02	12		mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
UVLO/EN logic threshold.							
UVLO threshold	$V_{VINUVVIN}$	Wake up, T_A = +25°C	1	01		2.25	V
VDD UVLO turn-on threshold	V_{DDUVLO}		1,2,3	02		2.3	V
High level input voltage	V_{ENIH}	Enable	1,2,3	01	1.7		V
Enable high-level input voltage (turn-on)	V_{IH_EN}		1,2,3	02		1.7	V
Low level input voltage	V_{ENIL}	Enable	1,2,3	01		0.3	V
Enable low-level input voltage (turn-off)	V_{IL_EN}		1,2,3	02	0.3		V
Logic input leakage current	I_{ENLEAK}	Enable, T_A = +25°C	1	01	-1	1	µA
Enable input leakage current	$I_{EN(LKG)}$		1,2,3	02	-1	1	µA

1/ Unless otherwise specified;
Device type 01. V_{DD}/V_{IN} = 3.3 V and 2.375 V, VLDOIN = 1.8 V, VDDQSNS = 1.8 V, VOSNS/VTTSNS = 0.9 V, EN = VDD/V_{IN}.
Device type 02. 2.375 V ≤ VDD ≤ 3.5 V, VLDOIN = 1.8 V, VDDQSNS = 1.8 V, VTTSNS = 0.9 V, EN = VDD/V_{IN}.

2/ The manufacturer supplying device types 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krads(Si). However device type 02 supplied to this drawing has been tested with total ionizing dose (TID) test at high dose rate (HDR) condition A per MIL-STD-883, method 1019 to TID level 100 krads(Si). For more information on TID test please contact device manufacturer.

3/ The manufacturer supplying RHA device types 01 and 02 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si).

4/ The parameter is guaranteed to the limits specified by characterization but, not production tested.

5/ Dropout and headroom information provided to help designer in optimizing system efficiency.

TABLE IB. SEP test limits. 1/ 2/ 3/ 4/

Device type	SEP/SEE	Temperature (T_A)	VIN	Effective Linear energy transfer (LET)
02	No SEL	125°C	3.5 V	LET ≤ 70 MeV/(mg/cm^2)
	No SEB/SEGR	25°C	3.5 V	LET ≤ 70 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.3 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ The heavy-ion test performed at TAMU cyclotron radiation effects facility. Holmium (^{165}Ho) ion beam were used at an angle of incidence of 0° at flux of 10^5 ions/cm^2·s, fluences level of 10^7 ions/cm^2 and a temperature of 125°C and no single event latch-up (SEL) was observed at effective LET of 75 MeV/(mg/cm^2). Manufacturer also test Single event burnout (SEB) and Single event gate rupture (SEGR) test with (^{165}Ho) ion beam were used at angles of incidence of 0°. No SEB/SEGR observed up to effective LET of 75 MeV/(mg/cm^2). For more information on SEE/SEP test please contact device manufacturer.

4/ For SEL test temperature T_A = +125°C ±10°C.

Case outline X

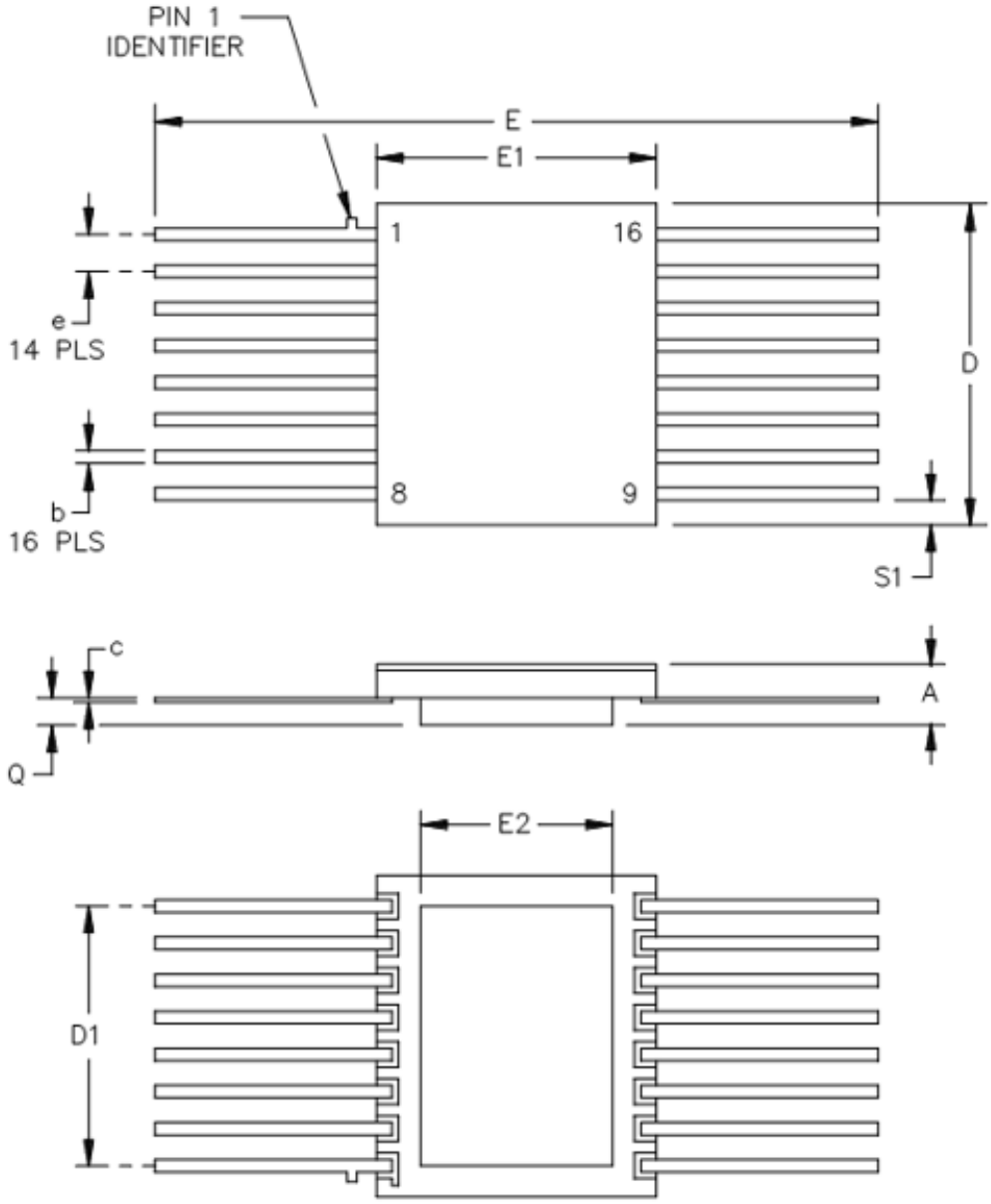


FIGURE 1. Case outline.

Case outline X – continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.850	2.416	.073	.095
b	0.382	0.482	0.015	0.019
c	0.097	0.177	0.004	0.007
D	10.760	11.260	0.424	0.443
D1	8.550	9.050	0.337	0.356
E	24.642	25.142	0.970	0.990
E1	9.380	9.880	0.369	0.389
E2	6.340	6.840	0.250	0.269
e	1.190	1.350	0.047	0.053
Q	0.84	1.04	0.033	0.041
S1	0.844 REF		0.033 REF	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid. Lid and heat sink are connected to pin 8 (GND).
3. The leads are gold plated.
4. Bottom side has a thermal pad.

FIGURE 1. Case outline - continued.

Case Y

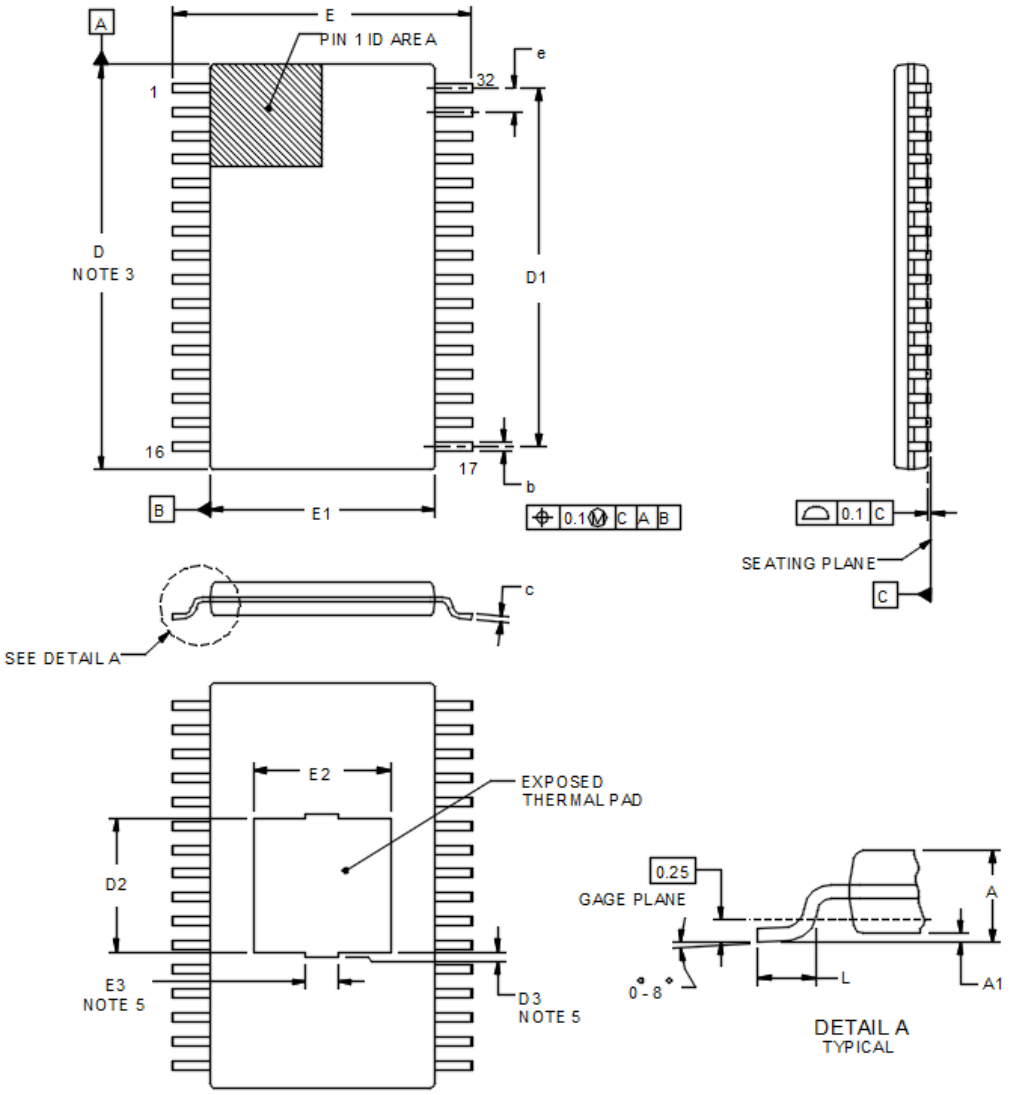


FIGURE 1. Case outline - continued.

Case Y – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.047	---	1.2
A1	.002	.006	0.05	0.15
b	.007	.012	0.19	0.30
c	.006 TYP		0.15 TYP	
D	.429	.437	10.9	11.1
D1	.384 BSC		9.75 BSC	
D2	.124	.160	3.16	4.06
D3	.006 REF		0.15 REF	
e	.026 BSC		0.65 BSC	
E	.311	.327	7.9	8.3
E1	.236	.244	6.0	6.2
E2	.129	.162	3.29	4.11
E3	.035 REF		0.9 REF	
L	.020	.029	0.50	0.75

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

FIGURE 1. Case outline - continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Input / Output	Description
1	VTTREF	O	Reference output. Connect to GND through 0.1 μF ceramic capacitor.
2	VDDQSNS	I	VDDQ sense input. Reference input for VTTREF.
3	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
4	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
5	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
6	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
7	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
8	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
9	EN	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.
10	VDD / V_{IN}	I	2.5 V or 3.3 V power supply. A ceramic decoupling capacitor with a value between 1 μF and 10 μF is required.
11	PGOOD	O	PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.
12	VTT / VO	O	Power output for VTT low drop out voltage regulator.
13	VTT / VO	O	Power output for VTT low drop out voltage regulator.
14	VTT / VO	O	Power output for VTT low drop out voltage regulator.
15	AGND	---	Signal ground. Connect to negative pin of output capacitors. See note.
16	VTTSNS	I	VDDQ sense input, reference input for VTTREF. Voltage sense for VTT/VO. Connect to positive pin of the output capacitor or the load.

NOTE: Thermal pad and package lid are internally connected to ground.

FIGURE 2. Terminal connections.

Device type	02		
Case outline	Y		
Terminal number	Terminal symbol	Input / Output 1/	Description
1	NC 3/	---	No connection.
2	NC 3/	---	No connection.
3	NC 3/	---	No connection.
4	VTTREF	O	Reference output. Connect to GND through 0.1 μF ceramic capacitor.
5	VDDQSNS	I	VDDQ sense input. Reference input for VTTREF. 2/
6	NC	---	No connection.
7	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
8	VLDOIN	I	Supply voltage for the low dropout (LDO) voltage regulator. Connect to VDDQ voltage or an alternate voltage source.
9	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
10	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
11	PGND	---	Power ground. Connect output for the VTT / V_O low dropout voltage regulator to negative pin of the output capacitor.
12	NC 3/	---	No connection.
13	NC 3/	---	No connection.
14	NC 3/	---	No connection.
15	NC 3/	---	No connection.
16	NC 3/	---	No connection.

FIGURE 2. Terminal connections - continued.

Device type	02		
Case outline	Y		
Terminal number	Terminal symbol	Input / Output 1/	Description
17	NC 3/	---	No connection.
18	NC 3/	---	No connection.
19	NC 3/	---	No connection.
20	EN	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.
21	VDD	I	2.5 V or 3.3 V power supply. A ceramic decoupling capacitor with a value between 1 μF and 10 μF is required.
22	PGOOD	O	PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.
23	VTT	O	Power output for VTT low drop out voltage regulator.
24	VTT	O	Power output for VTT low drop out voltage regulator.
25	VTT	O	Power output for VTT low drop out voltage regulator.
26	VTT	O	Power output for VTT low drop out voltage regulator.
27	NC	---	No connection.
28	AGND	---	Signal ground. Connect to negative pin of output capacitors. See note.
29	VTTSNS	I	VDDQ sense input, reference input for VTTREF. Voltage sense for VTT/VO. Connect to positive pin of the output capacitor or the load.
30	NC 3/	---	No connection.
31	NC 3/	---	No connection.
32	NC 3/	---	No connection.

1/ I = Input, O = Output, — = Other

2/ VDDQSNS shall be connected to the regulated voltage supplying VDDQ. If the VDDQ supply is also used for VLDOIN, an RC filter is recommended to isolate transients from VLDOIN to VDDQ.

3/ No connect. These pins are not internally connected. It is recommended to connect these pins to ground to prevent charge buildup; however, these pins can also be left open or tied to any voltage between ground and V_{DD}.

FIGURE 2. Terminal connections - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, P, Q, Y, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, P, Q, Y, and V, screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, P, Q Y, and V.

a. Test condition A, B, C and D. Burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Unless otherwise specified in the QM plan, for devices class N, P, Q, Y, and V, dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

c. For devices class P, Y, and V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

4.3 Qualification inspection. Qualification inspection for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. Preconditioning shall be performed on non hermetic device classes N, P, and Y surface mount devices as specified in the manufacturer's QM plan. Thermal shock is not applicable to class N, P, and organic class Y.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, tableIII)				
	Device class N	Device class P	Device class Q	Device class V	Device class Y
Interim (pre burn-in) electrical parameters, (see 4.2)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Post burn-in electrical parameters (see 4.2.1)	1,2,3 1/	1,2,3 1/ 2/	1,2,3, 1/	1,2,3 1/ 2/	1,2,3 1/
Group A (Final electrical) test requirements (see 4.4.1)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Group C end-point electrical parameters (see 4.4.2)	1,2,3	1,2,3 2/	1,2,3	1,2,3 2/	1,2,3
Group D end-point electrical parameters (see 4.4.3)	1	1	1	1	1
Group E end-point electrical parameters (see 4.4.4)	1	1	1	1	1

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous endpoint electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Conditions	Device type	Limit	Unit
Supply / quiescent current	I_{VIN}/I_{VDD}	V_{EN} = 3.3 V, no load	01, 02	±1	mA
Shutdown current	$I_{VDD(SDN)}$	V_{EN} = 0 V, no load, VDDQSNS > 0.78 V	01, 02	±0.24	mA
Supply / quiescent current of VLDOIN	I_{VLDOIN}	V_{EN} = 3.3 V, no load	01, 02	±60	µA
Shutdown current of VLDOIN	$I_{LDOIN(SDN)}$	V_{EN} = 0 V, no load, VDDQSNS > 0.78 V	01	±8.5	µA
Output DC voltage, VO	V_{VOSNS}/V_{TTSNS}	V_{LDOIN} = 1.8 V, I_O = 0 A, V_{VTTREF} = 0.9 V (DDR2)	01	±1	mV
Output DC voltage, VTT	VTTSNS	I_{VTT} = 5 mA	02	±1	mV
Output DC voltage, VTT	VTTSNS	I_{VTT} = - 5 mA	02	±1	mV

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. RHA levels for device classes N, P, Q, Y, and V, shall be as specified in MIL-PRF-38535 and the end-point electrical parameters subgroups shall be as specified in table IIA herein.

b. For device classes N, P, Q, Y, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total irradiation dose testing. Total irradiation dose testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and condition D for device type 01 and condition A for device type 02 as specified herein.

4.4.4.2 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.3 Single event phenomena (SEP). SEP testing was performed on two units per the conditions in table IB. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60˚ to the normal, inclusive (i.e., 0°≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ± 10% for SEL.

f. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, P, Q, Y, and V shall be in accordance with MIL-PRF-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply. Sources of supply for device classes N, P, Q, Y, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-12-18

Approved sources of supply for SMD 5962-14228 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1422801VXC	01295	TPS7H3301-SP
5962R1422801VXC	01295	TPS7H3301-RHA
5962R1422802PYE	01295	TPS7H3302-QMLP

1/ The lead finish shown for each PIN is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243