REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	23-12-18	James R. Eschmeyer

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
18-07-02

DLA LAND AND MARITIME
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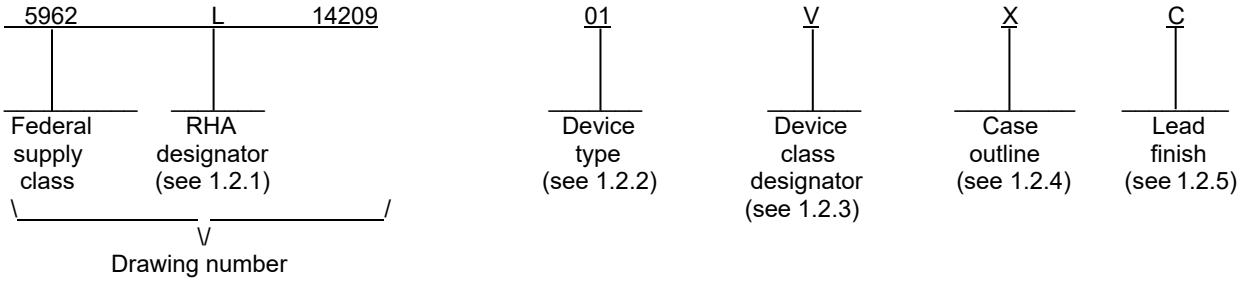
MICROCIRCUIT, LINEAR, CONTROLLER AREA NETWORK (CAN) TRANSCEIVER, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL A	SIZE A	CAGE CODE **67268**	**5962-14209**
		SHEET	1 OF 20	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	SN55HVD233-SP	Radiation hardened CAN transceiver, 3.3 V

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	8	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.3 V to +7 V
Voltage range at any bus terminal (CANH or CANL)	-16 V to +16 V
Voltage input range, transient pulse, CANH and CANL, through 100 Ω	-100 V to +100 V
Input voltage range (V_I)	-0.5 V to +7 V
Output voltage range (V_O)	-0.5 V to +7 V
Receiver output current (I_O)	-10 mA to +10 mA
Storage temperature (Tstg)	-65°C to +150°C
Thermal resistance, junction-to-case (bottom) (θ_{JCbot})	7.0°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	97.1°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+3 V to +3.6 V
Voltage range at any bus terminal (separately or common mode)	-7 V to +12 V
High-level input voltage range (V_{IH})	+2 V to +5.5 V
Low-level input voltage range (V_{IL})	0 V to +0.8 V
Differential input voltage range (V_{ID})	-6 V to +6 V
Resistance from R_S to ground	0 Ω to 50 kΩ
Input voltage range at R_S for standby ($V_{I(RS)}$)	+0.75 V_{CC} to +5.5 V
High-level output current:	
Driver	-50 mA
Receiver	-10 mA
Low-level output current:	
Driver	+50 mA
Receiver	+10 mA
Operating junction temperature (T_J)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (low dose rate = 1 mrad(Si)/s)	50 krad(Si) 3/
Maximum total dose available (effective dose rate = 41.33 mrad(Si)/s	50 krad(Si) 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

3/ The manufacturer supplying device type 01 has performed low dose rate test in accordance with MIL-STD-883 method 1019, condition D. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D.

4/ Device type 01 is irradiated at dose rate = 50 - 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 41.33 mrad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test		Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
							Min	Max	
DRIVER ELECTRICAL CHARACTERISTICS									
Bus output voltage (Dominant)		$V_{O(D)}$	D = 0 V, R_S = 0 V, see figures 5 and 6	CANH	1, 2, 3	01	2.25	V_{CC}	V
				CANL			0.5	1.25	
Differential output voltage (Dominant)		$V_{OD(D)}$	D = 0 V, R_S = 0 V, see figures 5 and 6		1, 2, 3	01	1.5	3	V
				L			1.2	3	
			D = 0 V, R_S = 0 V, see figures 6 and 7				1.2	3	
Differential output voltage (Recessive)		V_{OD}	D = 3 V, R_S = 0 V, see figures 5 and 6		1, 2, 3	01	-120	12	mV
			D = 3 V, R_S = 0 V, no load				-0.5	0.05	V
High-level input current		I_{IH}	D, LBK pins = 2 V		1, 2, 3	01	-30	30	µA
Low-level input current		I_{IL}	D, LBK pins = 0.8 V		1, 2, 3	01	-30	30	µA
Short circuit output current		I_{OS}	V_{CANH} = -7 V, CANL open, see figure 8		1, 2, 3	01	-250		mA
			V_{CANH} = 12 V, CANL open, see figure 8					1	
			V_{CANL} = -7 V, CANH open, see figure 8				-1		
			V_{CANL} = 12 V, CANH open, see figure 8					250	
R_S input current for standby		$I_{IRS(S)}$	R_S = 0.75 V_{CC}		1, 2, 3	01	-10		µA
Supply current:	Standby	I_{CC}	D = V_{CC}, no load, LBK = 0 V, R_S = 0 V		1, 2, 3	01		850	µA
	Dominant		V(D) = 0 V, no load, V(LBK) = 0 V, R_S = 0 V					6	mA
	Recessive		V(D) = V_{CC}, no load, V(LBK) = 0 V, V(RS) = 0 V					6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DRIVER SWITCHING CHARACTERISTICS							
Propagation delay time, low-to-high level output	t_{PLH}	R_S = 0 V, see figure 9	9, 10, 11	01		85	ns
		R_S with 10 kΩ to ground, see figure 9				125	
		R_S with 50 kΩ to ground, see figure 9				870	
Propagation delay time, high-to-low level output	t_{PHL}	R_S = 0 V, See figure 9	9, 10, 11	01		120	ns
		R_S with 10 kΩ to ground, see figure 9				180	
		R_S with50 kΩ to ground, see figure 9				1200	
Differential output signal rise time	t_r	R_S = 0 V, see figure 9	9, 10, 11	01	20	70	ns
		R_S with 10 kΩ to ground, see figure 9			30	135	
		R_S with 50 kΩ to ground, see figure 9			350	1400	
Differential output signal fall time	t_f	R_S = 0 V, see figure 9	9, 10, 11	01	20	70	ns
		R_S with 10 kΩ to ground, see figure 9			30	135	
		R_S with 50 kΩ to ground, see figure 9			350	1400	
Enable time from standby to dominant	$t_{EN(S)}$	See figure 10	9, 10, 11	01		1.5	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
							Min	Max	
RECEIVER ELECTRICAL CHARACTERISTICS									
Positive-going input threshold voltage		V_{IT+}	LBK = 0 V, see figure 11		1, 2, 3	01		900	mV
Negative-going input threshold voltage		V_{IT-}	LBK = 0 V, see figure 11		1, 2, 3	01	500		mV
High-level output voltage		V_{OH}	I_O = -4 mA		1, 2, 3	01	2.4		V
Low-level output voltage		V_{OL}	I_O = 4 mA		1, 2, 3	01		0.4	V
Bus input current		I_I	CANH or CANL = 12 V	Other bus pin = 0 V, D = 3 V, LBK = 0 V, R_S = 0 V	1, 2, 3	01	150	500	µA
			CANH or CANL = 12 V, V_{CC} = 0 V				150	600	
			CANH or CANL = -7 V				-610	-100	
			CANH or CANL = -7 V, V_{CC} = 0 V				-450	-100	
Differential input resistance		R_{ID}	D = 3 V, LBK = 0 V		1, 2, 3	01	40	105	kΩ
Input resistance (CANH or CANL)		R_{IN}	D = 3 V, LBK = 0 V		1, 2, 3	01	20	55	kΩ
Supply current:	Standby	I_{CC}	$R_S = V_{CC}$, D = V_{CC}, LBK = 0 V		1, 2, 3	01		850	µA
	Dominant		D = 0 V, no load, R_S = 0 V, LBK = 0 V					6	mA
	Recessive		D = V_{CC}, no load, R_S = 0 V, LBK = 0 V					6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RECEIVER SWITCHING CHARACTERISTICS							
Propagation delay time, low-to-high level output	t_{PLH}	see figure 12	9, 10, 11	01		105	ns
Propagation delay time, high-to-high level output	t_{PHL}	see figure 12	9, 10, 11	01		105	ns
DEVICE SWITCHING CHARACTERISTICS							
Total loop delay, driver input to receiver output, recessive to dominant	t_{LOOP1}	R_S = 0 V, see figure 13	9, 10, 11	01		150	ns
		R_S with 10 kΩ, see figure 13				225	
		R_S with 50 kΩ, see figure 13				600	
Total loop delay, driver input to receiver output, dominant to recessive	t_{LOOP2}	R_S = 0 V, see figure 13	9, 10, 11	01		150	ns
		R_S with 10 kΩ, see figure 13				225	
		R_S with 50 kΩ, see figure 13				600	

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, and L of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

The manufacturer supplying device type 01 has performed low dose rate test in accordance with MIL-STD-883 method 1019, condition D. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D.

Device type 01 is irradiated at dose rate = 50 - 300 rad(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 41.33 mrad(Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for this device only applies to the specified effective dose rate, or lower, environment.

2/ For production testing of these parameters to the limits in table I herein, ambient temperature (T_A) = junction temperature (T_J).

Case X

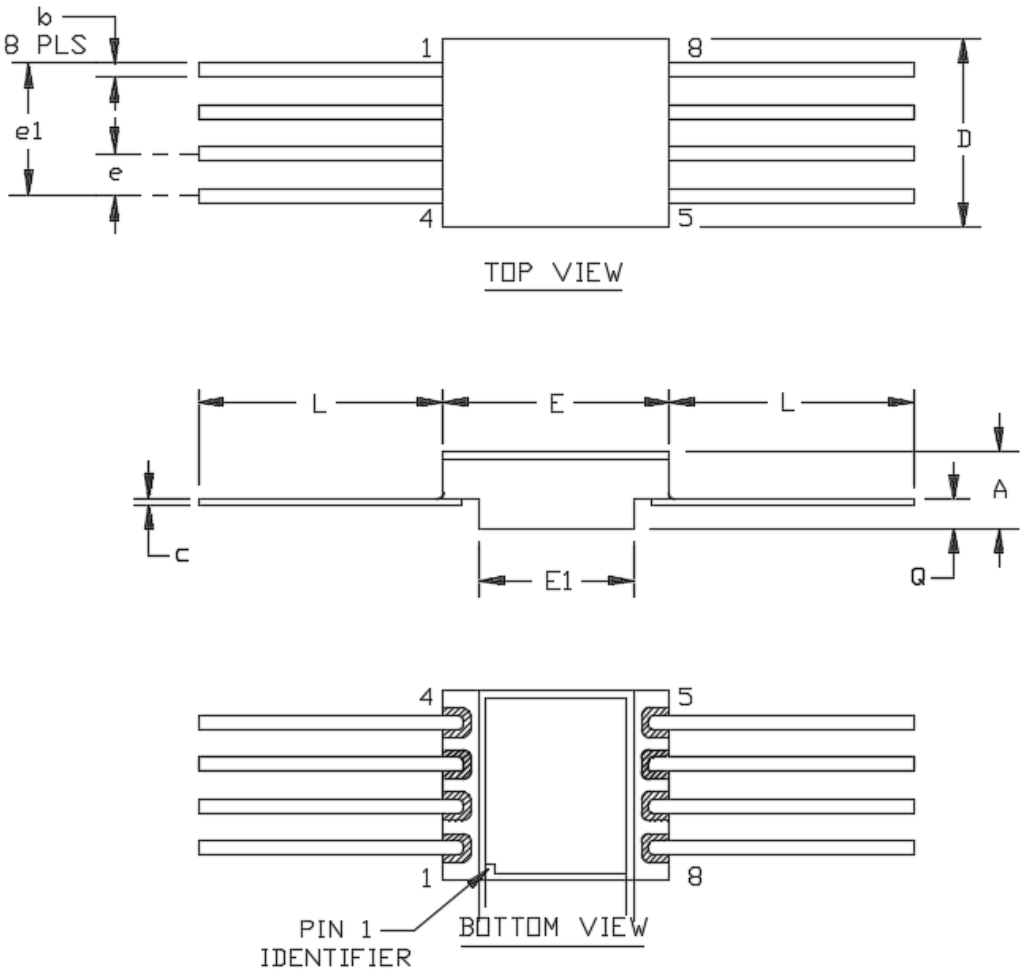


FIGURE 1. Case outline.

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.1096	---	2.785
b	.0165	.0204	0.42	0.52
c	.0047	.0078	0.12	0.20
D	.2450	.2647	6.225	6.725
E	.2454	.2651	6.235	6.735
E1	.1749 NOM		4.445 NOM	
e	.0499 BSC		1.27 BSC	
e1	.1499 BSC		3.81 BSC	
L	.6797	.6994	17.265	17.765
Q	---	.0374	---	0.95

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535. Lead finishes are in accordance with MIL-PRF-38535.

FIGURE 1. Case outline - Continued.

Terminal number	Terminal symbol	Type	Description
1	D	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
2	GND	Ground	Ground connection
3	V_{CC}	Supply	Transceiver 3.3 V supply voltage
4	R	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
5	LBK	I	Loopback mode input pin.
6	CANL	I/O	Low-level CAN bus line.
7	CANH	I/O	high level CAN bus line
8	R_S	I	Mode select pin: strong pull down to GND = high speed mode, strong pull up to V_{CC} = low power mode, 10 kΩ to 50 kΩ pull down to GND = slope control mode

FIGURE 2. Terminal connections.

DRIVER I/O					
INPUTS			OUTPUTS		
D	LBK	R_S	CANH	CANL	BUS STATE
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

RECEIVER I/O			
INPUTS			OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} – V_{(CANL)}$	D	R
Dominant	$V_{ID} \geq 0.9$ V	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	H or open	H
?	0.5 V < V_{ID} < 0.9 V	H or open	?
Dominant	$V_{ID} \geq 0.9$ V	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	H	H
Recessive	$V_{ID} \leq 0.5$ V or open	L	L
?	0.5 V < V_{ID} < 0.9 V	L	L

Notes: H = high level
L = low level
Z = high impedance
X = irrelevant
? = indeterminate

FIGURE 3. Truth tables

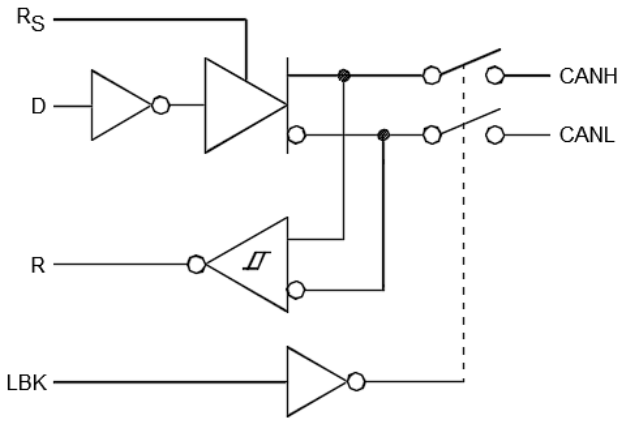


FIGURE 4. Block diagram.

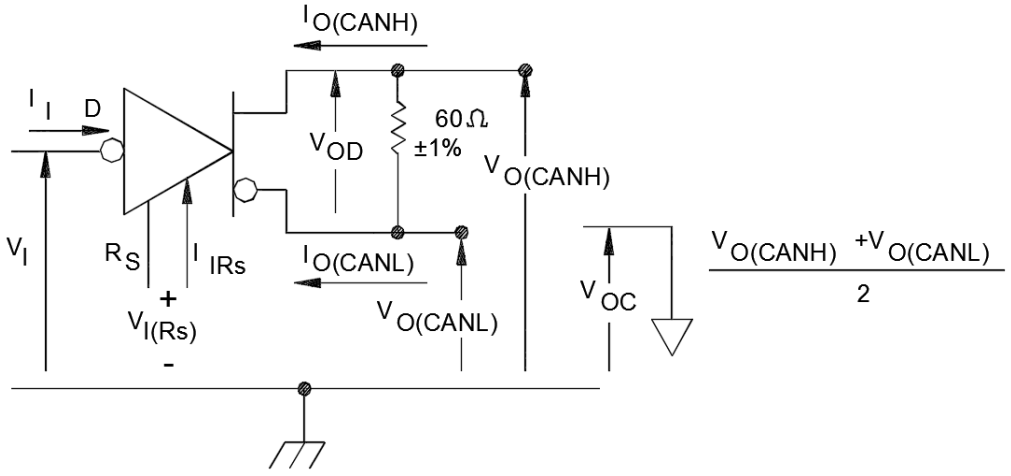


FIGURE 5. Driver voltage, current, and test definition.

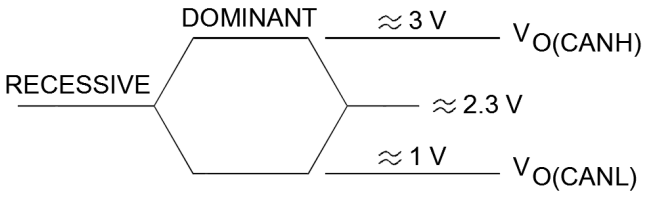


FIGURE 6. Bus logic state voltage defininitions.

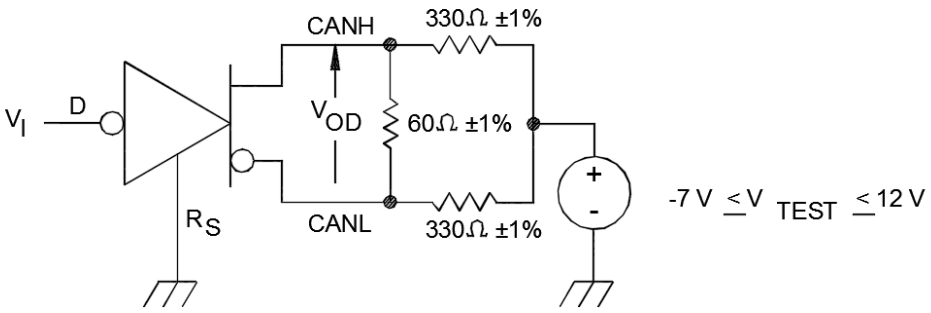


FIGURE 7. Driver V_{OD}.

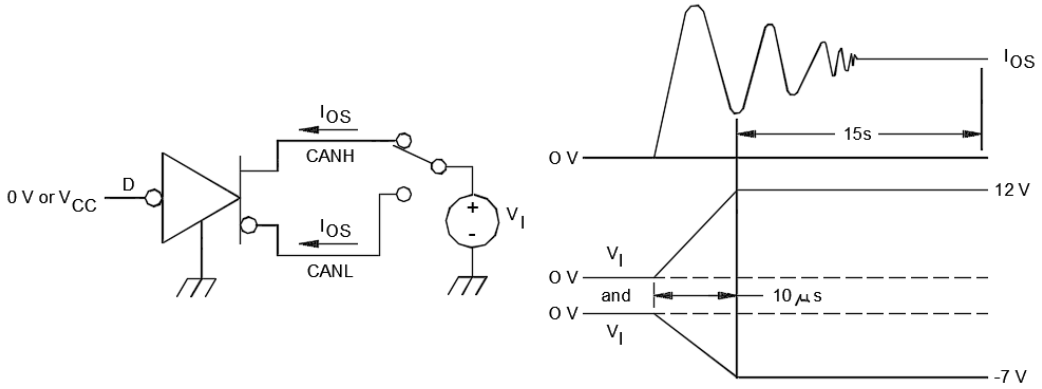
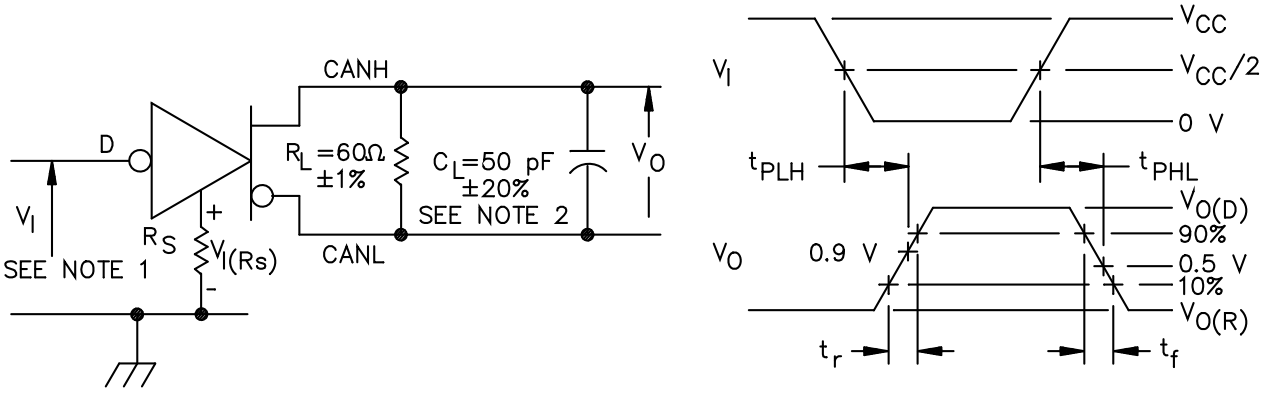


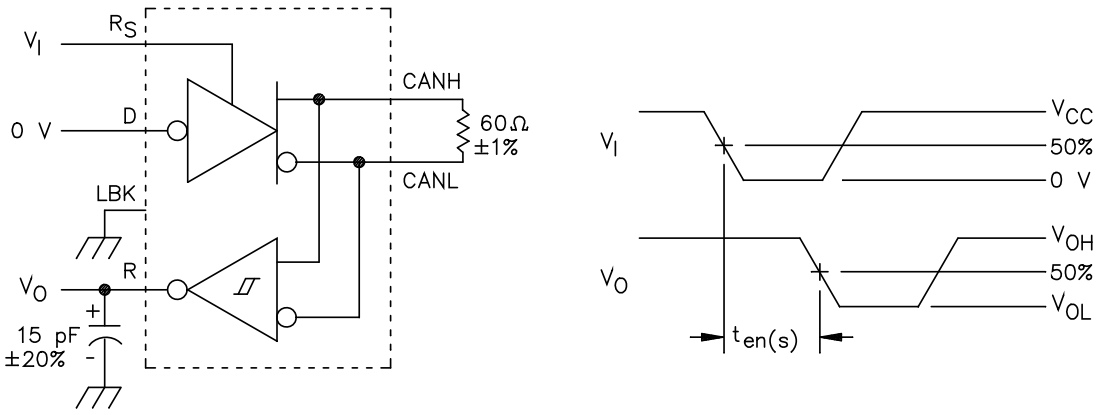
FIGURE 8. I_{OS} test cicuit and waveforms.



NOTES: 1. The input pulse is supplied by generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

2. C_L includes fixture and instrumentation capacitance.

FIGURE 9. Driver test circuit and timing waveforms.

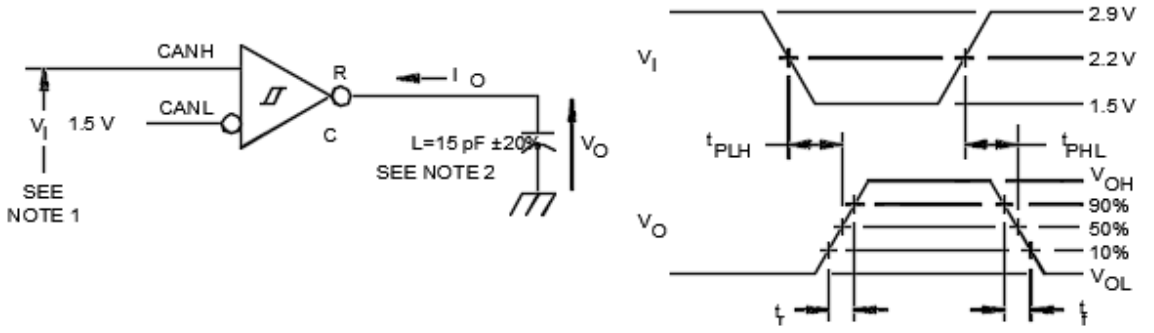


NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, Pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

FIGURE 10. Enable time test circuit and timing waveforms.

Input		Output		Measured
V_{CANH}	V_{CANL}	R		$\|V_{ID}\|$
-6.1 V	-7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
-1 V	-7 V	L		6 V
12 V	6 V	L		6 V
-6.5 V	-7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
-7 V	-1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X

FIGURE 11 Differential input voltage threshold test.



NOTES: 1. The input pulse is supplied by generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
2. C_L includes fixture and instrumentation capacitance.

FIGURE 12. Receiver test circuit and timing waveforms.

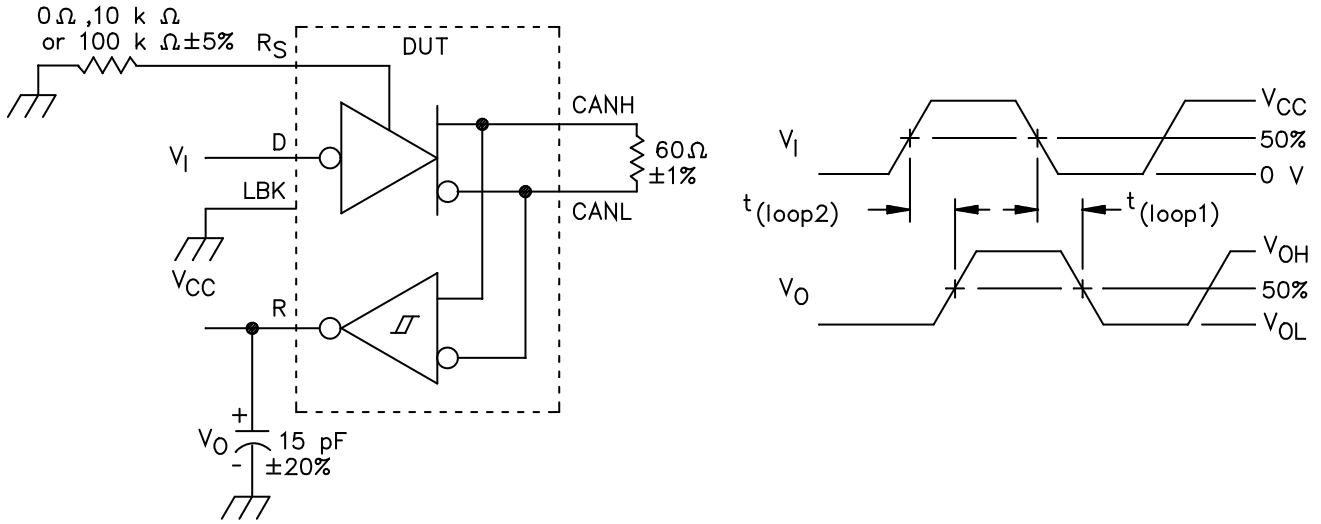


FIGURE 13. Loop delay test circuit and timing waveforms.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 9, 1/ 10, 11	1, 2, 3, 1/ 2/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 9	1, 2, 3 2/
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A and D and as specified herein section 1.5.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table A herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C.

Parameters	Symbol	Conditions	Min	Max	Delta limit	Units
Bus output voltage (Dominant)	$V_{O(D)}$	V_{CC} = 3 V	2.4	3.6	±0.192	V
Differential output voltage (Dominant)	$V_{OD(D)}$	V_{CC} = 3 V	1.4	3	±0.112	V
Bus output voltage (Dominant)	$V_{O(D)}$	V_{CC} = 36 V	2.4	3.6	±0.192	V
Differential output voltage (Dominant)	$V_{OD(D)}$	V_{CC} = 36 V	1.4	3	±0.112	V
Supply current: (Standby)	I_{CC}	V_{CC} = 3 V		600	±50	µA
Supply current: (Dominant)	I_{CC}	V_{CC} = 3 V		6	±0.48	mA
Supply current: (Recessive)	I_{CC}	V_{CC} = 3 V		6	±0.48	mA
Supply current: (Standby)	I_{CC}	V_{CC} = 36 V		600	±50	µA
Supply current: (Dominant)	I_{CC}	V_{CC} = 36 V		6	±0.48	mA
Supply current: (Recessive)	I_{CC}	V_{CC} = 36 V		6	±0.48	mA
Low level output voltage	V_{OL}	V_{CC} = 3 V		0.4	±0.008	V
High level output voltage	V_{OH}	V_{CC} = 3 V	2.4		±0.12	V
High level output voltage	V_{OH}	V_{CC} = 3 V	2.4		±0.12	V
High level output voltage	V_{OH}	V_{CC} = 3 V	2.4		±0.12	V
Low level output voltage	V_{OL}	V_{CC} = 3 V		0.4	±0.008	V
Low level output voltage	V_{OL}	V_{CC} = 36 V		0.4	±0.008	V
High level output voltage	V_{OH}	V_{CC} = 36 V	2.4		±0.12	V
High level output voltage	V_{OH}	V_{CC} = 36 V	2.4		±0.12	V

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-12-18

Approved sources of supply for SMD 5962-14209 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L1420901VXC	01295	SN55HVD233-RHA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243