REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add RHA device type 02. Add single event phenomenon (SEP) information in section 1.5 and SEP table IB. - ro	16-07-06	C. SAFFLE
B	Drawing updated to reflect current MIL-PRF-38535 requirements. -rrp	21-09-17	J. ESCHMEYER

REV																				
SHEET																				
REV	B	B	B	B	B															
SHEET	15	16	17	18	19															

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
15-08-20

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, LOW NOISE, PRECISION, RAIL TO RAIL OUTPUT, JFET DUAL OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-14207**

SHEET 1 OF 19

DSCC FORM 2233
APR 97

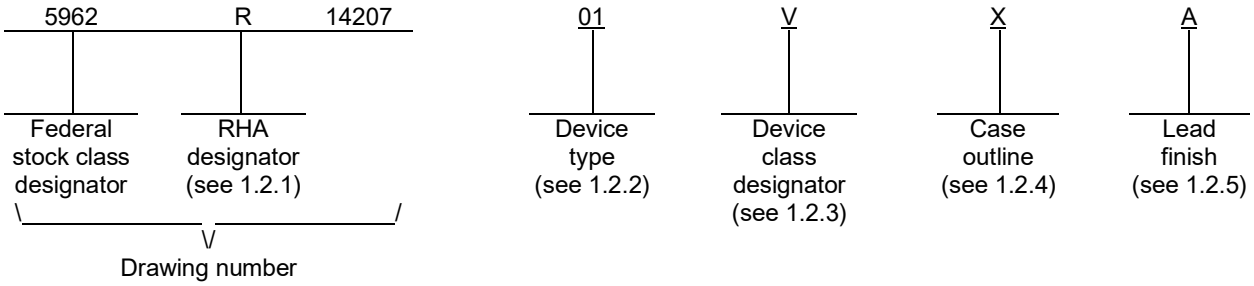
5962-E529-21

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADA4610-2	Radiation hardened, low noise, precision, rail to rail output, junction field effect transistor (JFET) dual operational amplifier
02	ADA4610-2	Radiation hardened, low noise, precision, rail to rail output, junction field effect transistor (JFET) dual operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F10	10	Bottom brazed flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage ($+V_S$ to $-V_S$)	36 V
Input voltage (V_{IN})	$-V_S$ to $+V_S$
Differential input voltage	$\pm V_S$
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C 2/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	23°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA})	39°C/W 3/

1.4 Recommended operating conditions.

Dual supply voltage ($\pm V_S$)	$\pm$5.0 V to $\pm$15.0 V
Single supply voltage ($+V_S$ / 0 V)	+10.0 V to +30.0 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Nominal operating performance characteristics. 4/

Input capacitance (C_{IN}):	
Differential (C_{DM})	3.1 pF
Common mode (C_{CM})	4.8 pF
Input resistance (R_{IN})	$> 1 \times 10^{13}\ \Omega$
Unity gain crossover: (V_{IN} = 5 mV_{PP}, R_L = 2 kΩ, A_V = -10)	
$\pm V_S$ = $\pm$5 V and $\pm$15 V	9.3 MHz
Phase margin:	
$\pm V_S$ = $\pm$5 V	61°
$\pm V_S$ = $\pm$15 V	66°
-3 dB closed loop bandwidth: (V_{IN} = 5 mV_{PP}, A_V = 1)	
$\pm V_S$ = $\pm$5 V	10.6 MHz
$\pm V_S$ = $\pm$15 V	9.5 MHz
Total harmonic distortion (THD) + noise:	
$\pm V_S$ = $\pm$15 V, 1 kHz, G = +1, R_L = 2 kΩ, V_{IN} = 6 Vrms	0.00006%

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ While the device is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. Do not exceed maximum T_J in application with output current load.

3/ Measurement taken under absolute worst case condition and represents data taken with thermal camera for highest power density location. See MIL-STD-1835 for average θ_{JC} number.

4/ Unless otherwise specified, T_A = +25°C, $\pm V_S$ = $\pm$5 V, $\pm V_S$ = $\pm$15 V, and V_{CM} = 0 V.

1.6 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device type 01 ..... 100 krads(Si) 5/
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s):
Device type 02 ..... 50 krads(Si) 6/
Single event phenomenon (SEP):
No single event latchup (SEL) occurs at effective linear energy transfer (LET) (see 4.4.4.2):
Device types 01 and 02 ..... ≤ 80 MeV cm^2/mg 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org).

5/ Device type 01 may exhibit enhanced low dose rate sensitivity (ELDRS) effects. The manufacturer supplying device type 01 has performed high dose rate testing in accordance with MIL-STD-883 method 1019 condition A. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A for a total dose of 100 krads (Si).

6/ The manufacturer supplying device type 02 has performed low dose rate (LDR) testing in accordance with MIL-STD-883 method 1019 condition D. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D for a total dose of 50 krads (Si).

7/ Limits are characterized at initial qualification and after any design or process changes that may affect the SEP characteristics, but are not production lot tested unless specified by the customer through the purchase order or contract. For more information on single event effect (SEE) test results, customers are requested to contact the manufacturer.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 5$ V, $V_{CM} = 0$ V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input characteristics.								
Offset voltage	V_{OS}			1, 3	01, 02	-0.4	0.4	mV
				2		-0.8	0.8	
			P, L, R	1	01	-0.4	+0.4	
			P, L	1	02	-0.4	+0.4	
Offset voltage drift	$\Delta V_{OS}/\Delta T$	3/ 4/		2, 3	01, 02	-8	8	µV/°C
Input bias current 5/	I_B			1, 3	01, 02	-25	25	pA
				2		-1.5	1.5	nA
			P, L, R	1	01	-25	25	pA
			P, L	1	02	-25	25	pA
Input offset current 5/	I_{OS}			1, 3	01, 02	-20	20	pA
				2		-0.4	0.4	nA
			P, L, R	1	01	-20	20	pA
			P, L	1	02	-20	20	pA
Input voltage range	IVR			1, 2, 3	01, 02	-2.5	2.5	V
			P, L, R	1	01	-2.5	2.5	
			P, L	1	02	-2.5	2.5	
Common mode rejection ratio	CMRR	V_{CM} = -2.5 V to +2.5 V		1	01, 02	94		dB
				2, 3		86		
			P, L, R	1	01	94		
			P, L	1	02	94		
Large signal voltage gain	A_{VO}	R_L = 2 kΩ,		1, 3	01, 02	98		dB
		V_O = -3.5 to +3.5 V		2		86		
			P, L, R	1	01	98		
			P, L	1	02	98		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 5$ V, $V_{CM} = 0$ V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output characteristics.								
Output voltage high	V_{OH}	R_L = 2 kΩ to GND		1, 3	01, 02	4.85		V
				2		4.6		
			P, L, R	1	01	4.85		
			P, L	1	02	4.85		
		R_L = 600 Ω to GND		1, 3	01, 02	4.6		
				2		4.05		
			P, L, R	1	01	4.6		
			P, L	1	02	4.6		
Output voltage low	V_{OL}	R_L = 2 kΩ to GND		1, 3	01, 02		-4.9	V
				2			-4.75	
			P, L, R	1	01		-4.9	
			P, L	1	02		-4.9	
		R_L = 600 Ω to GND		1, 3	01, 02		-4.8	
				2			-4.4	
			P, L, R	1	01		-4.8	
			P, L	1	02		-4.8	
Short circuit limit 6/	$+I_{SC}$	Source		1, 2	01, 02	-65		mA
				3		-70		
			P, L, R	1	01	-65		
			P, L	1	02	-65		
	$-I_{SC}$	Sink		1, 2	01, 02		+65	
				3			+70	
			P, L, R	1	01		+65	
			P, L	1	02		+65	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 5$ V, $V_{CM} = 0$ V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power supply								
Power supply rejection ratio	PSRR	$\pm V_S = \pm 4.5$ V to ± 18 V		1	01, 02	106		dB
				2, 3		103		
			P, L, R	1	01	106		
			P, L	1	02	106		
Total supply current (both amplifiers)	I_S	$I_O = 0$ mA		1	01, 02		± 3.4	mA
				2, 3			± 3.7	
			P, L, R	1	01		± 3.4	
			P, L	1	02		± 3.4	
Transient response.								
Rise time	t_R	$V_{IN} = 5$ mV_{PP}, 3/ 7/ 8/ $R_L = 2$ kΩ, $C_L = 100$ pF, $A_V = -1$		9	01, 02		31	ns
				10			57	
				11			26	
Fall time	t_F	$V_{IN} = 5$ mV_{PP}, 3/ 7/ 8/ $R_L = 2$ kΩ, $C_L = 100$ pF, $A_V = -1$		9	01, 02		51	ns
				10			70	
				11			41	
Settling time	$+t_S$	0.1% error, $A_V = -1$ 3/ 7/		9	01, 02		430	ns
				10			540	
				11			410	
	$-t_S$			9			450	
				10			670	
				11			650	
Overshoot	+OVR	$V_{IN} = 5$ mV_{PP}, $A_V = -1$, 3/ 7/ $R_L = 2$ kΩ, $C_L = 100$ pF		9	01, 02		12	ns
				10, 11			14	
	-OVR			9, 10, 11			20	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 5$ V, $V_{CM} = 0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
Gain bandwidth product	GBP	V_{IN} = 5 mV_{PP}, 3/ 7/ A_V = -100, R_L = 2 kΩ	4	01, 02	17		MHz
			5		9		
			6		24		
Slew rate	+SR	R_L = 2 kΩ, 3/ 7/ 8/ C_L = 100 pF	4	01, 02	25		V/μs
			5		13		
			6		33		
	-SR		4		17		
			5		11		
			6		19		
Noise performance.							
Peak to peak voltage noise	en_{PP}	0.1 Hz to 10 Hz bandwidth 3/ 7/	4	01, 02		1.7	μV_{PP}
			5			4	
			6			3.2	
Voltage noise density	en	f = 10 kHz 3/ 7/	4	01, 02		7.3	nV/ $\sqrt{Hz}$
			5			10.5	
			6			5.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 15$ V, $V_{CM} = 0$ V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input characteristics.								
Offset voltage	V_{OS}			1, 3	01, 02	-0.4	0.4	mV
				2		-0.8	0.8	
			P, L, R	1	01	-0.4	+0.4	
			P, L	1	02	-0.4	+0.4	
Offset voltage drift	$\Delta V_{OS}/\Delta T$	3/ 4/		2, 3	01, 02	-8	8	µV/°C
Input bias current 5/	I_B			1, 3	01, 02	-25	25	pA
				2		-1.5	1.5	nA
			P, L, R	1	01	-25	25	pA
			P, L	1	02	-25	25	pA
Input offset current 5/	I_{OS}			1, 3	01, 02	-20	20	pA
				2		-0.4	0.4	nA
			P, L, R	1	01	-20	20	pA
			P, L	1	02	-20	20	pA
Input voltage range	IVR			1, 2, 3	01, 02	-12.6	12.6	V
			P, L, R	1	01	-12.6	12.6	
			P, L	1	02	-12.6	12.6	
Common mode rejection ratio	CMRR	V_{CM} = -12.6 V to +12.6 V		1	01, 02	100		dB
				2, 3		96		
			P, L, R	1	01	100		
			P, L	1	02	100		
Large signal voltage gain	A_{VO}	R_L = 2 kΩ,		1, 3	01, 02	104		dB
		V_O = -13.5 to +13.5 V		2		91		
			P, L, R	1	01	104		
			P, L	1	02	104		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 15$ V, $V_{CM} = 0$ V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output characteristics.								
Output voltage high	VOH	RL = 2 kΩ to GND		1, 3	01, 02	14.80		V
				2		14.65		
			P, L, R	1	01	14.80		
			P, L	1	02	14.80		
		R_L = 600 Ω to GND		1, 3	01, 02	14.25		
				2		13.35		
			P, L, R	1	01	14.25		
			P, L	1	02	14.25		
Output voltage low	V_{OL}	R_L = 2 kΩ to GND		1, 3	01, 02		-14.85	V
				2			-14.75	
			P, L, R	1	01		-14.85	
			P, L	1	02		-14.85	
		R_L = 600 Ω to GND		1, 3	01, 02		-14.60	
				2			-14.30	
			P, L, R	1	01		-14.60	
			P, L	1	02		-14.60	
Short circuit limit 6/	$+I_{SC}$	Source		1, 2	01, 02	-85		mA
				3		-95		
			P, L, R	1	01	-85		
			P, L	1	02	-85		
	$-I_{SC}$	Sink		1, 2	01, 02		+85	
				3			+95	
			P, L, R	1	01		+85	
			P, L	1	02		+85	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 15$ V, $V_{CM} = 0$ V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power supply.								
Power supply rejection ratio	PSRR	$\pm V_S = \pm 4.5$ V to ± 18 V		1	01, 02	106		dB
				2, 3		103		
			P, L, R	1	01	106		
			P, L	1	02	106		
Total supply current (both amplifiers)	I_{SY}	$I_O = 0$ mA		1	01, 02		± 3.7	mA
				2, 3			± 4	
			P, L, R	1	01		± 3.7	
			P, L	1	02		± 3.7	
Transient response.								
Rise time	t_R	$V_{IN} = 5$ mV_{PP}, 3/ 7/ 8/ $R_L = 2$ kΩ, $C_L = 100$ pF, $A_V = -1$		9	01, 02		31	ns
				10			57	
				11			24	
Fall time	t_F	$V_{IN} = 5$ mV_{PP}, 3/ 7/ 8/ $R_L = 2$ kΩ, $C_L = 100$ pF, $A_V = -1$		9	01, 02		51	ns
				10			69	
				11			39	
Settling time	$+t_S$	0.1% error, $A_V = -1$ 3/ 7/		9	01, 02		430	ns
				10			540	
				11			410	
	$-t_S$			9			450	
				10			670	
				11			650	
Overshoot	+OVR	$V_{IN} = 5$ mV_{PP}, AV = -1, 3/ 7/ $R_L = 2$ kΩ, $C_L = 100$ pF		9	01, 02		12	ns
				10, 11			14	
	-OVR			9, 10, 11			20	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ $\pm V_S = \pm 15$ V, $V_{CM} = 0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance							
Gain bandwidth product	GBP	$V_{IN} = 5\ mV_{PP}$, 3/ 7/ $A_V = -100$, $R_L = 2\ k\Omega$	4	01, 02	17		MHz
			5		9		
			6		24		
Slew rate	+SR	$R_L = 2\ k\Omega$, 3/ 7/ 8/ $C_L = 100$ pF	4	01, 02	25		V/μs
			5		13		
			6		33		
	-SR		4		17		
			5		11		
			6		19		
Noise performance.							
Peak to peak voltage noise	en_{PP}	0.1 Hz to 10 Hz bandwidth 3/ 7/	4	01, 02		1.7	μV_{PP}
			5			4	
			6			3.2	
Voltage noise density	en	f = 10 kHz 3/ 7/	4	01, 02		7.3	nV/ $\sqrt{Hz}$
			5			10.5	
			6			5.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

1/ Device type 01 supplied to this drawing has been characterized through all levels P, L, and R of irradiation. However, device type 01 is only tested at the "R" level. Device type 02 supplied to this drawing has been characterized through all levels P and L of irradiation. However, device type 02 is only tested at the "L" level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, TA = +25°C.

2/ Device type 01 may exhibit enhanced low dose rate sensitivity (ELDRS) effects. The manufacturer supplying device type 01 has performed high dose rate testing in accordance with MIL-STD-883 method 1019 condition A. The manufacturer supplying device type 02 has performed irradiation testing at low dose rate in accordance with MIL-STD-883, method 1019, condition D. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a total dose of 100 krads (Si) for device type 01, and only for the conditions as specified in MIL-STD-883, method 1019, condition D to a total dose of 50 krads (Si) for device type 02.

3/ Parameter is not tested post irradiation.

4/ Calculated from 25°C to -55°C, 25°C to +125°C and -55°C to +125°C.

5/ Input bias current increase exponentially as $T_A >$ +45°C. Refer to the input bias current versus temperature graphs in the manufacturer's datasheet.

6/ While the device is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. Do not exceed maximum T_J in application with output current load.

7/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

8/ Measured from 10% to 90% and 90% to 10% of output swing.

TABLE IB. SEP test limits. 1/

Device types	SEP	Temperature (T_C)	Bias	Linear energy transfer (LET)
01, 02	No SEL	125°C	V_S = ± 18 V	Effective LET ≤ 80 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.2 herein.

Device types	01, 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal type	Description
1	NC/GND	N/A	No connection or ground for this terminal.
2	OUT A	Analog output	Operational amplifier output, Amplifier A.
3	-IN A	Analog input	Operational amplifier negative input, Amplifier A.
4	+IN A	Analog input	Operational amplifier positive input, Amplifier A.
5	$-V_S$	Power	Negative power supply.
6	NC/GND	N/A	No connection or ground for this terminal.
7	+IN B	Analog input	Operational amplifier positive input, Amplifier B.
8	-IN B	Analog input	Operational amplifier negative input, Amplifier B.
9	OUT B	Analog output	Operational amplifier output, Amplifier B.
10	$+V_S$	Power	Positive power supply.

FIGURE 1. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3,4, 1/ 3/ 5,6,9,10,11	1,2,3,4, 1/ 2/ 3/ 5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 3/ 9,10,11	1,2,3,4,5,6, 3/ 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3,4,5, 2/ 3/ 6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters (see Table IA).
3/ See Table IA for parameters characterized for subgroups 4, 5, 6, 9, 10, and 11.

TABLE IIB. Burn-in and operating life test delta parameters. 1/ 2/

Parameters	Symbol	Conditions	Delta limits	Units
Offset voltage	V_{OS}		±120	μV
Input bias current	I_B	V_{CM} = 0 V	±9.4	pA
Supply current	I_S		±0.07	mA

1/ Deltas are performed at room temperature T_A = +25°C.
2/ 240 hour burn-in and 1,000 hour operating group C life test.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and D as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq \text{angle} \leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C and the maximum rated operating temperature $\pm 10°$C for single event latchup. testing.

f. Bias conditions shall be $V_S = \pm 18$ V for the latchup measurements.

g. For SEP limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Application notes.

6.7.1 General Description. The device is a dual precision JFET amplifier that features low offset voltage, low input bias current, low input voltage noise, low input current noise, and rail-to-rail output. The device maintains fast settling performance even with substantial capacitive loads. The device does not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range. See manufacturer's datasheet for more application information regarding these specifications.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-09-17

Approved sources of supply for SMD 5962-14207 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1420701VXA	24355	ADA4610-2BF/QMLR
5962L1420702VXA	24355	ADA4610-2BF/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.