REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22											
REV STATUS				REV															
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Raj Pithadia

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raj Pithadia

APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
14-08-12

REVISION LEVEL

MICROCIRCUIT, LINEAR, PHASE LOCKED LOOP FREQUENCY SYNTHESIZER, MONOLITHIC SILICON

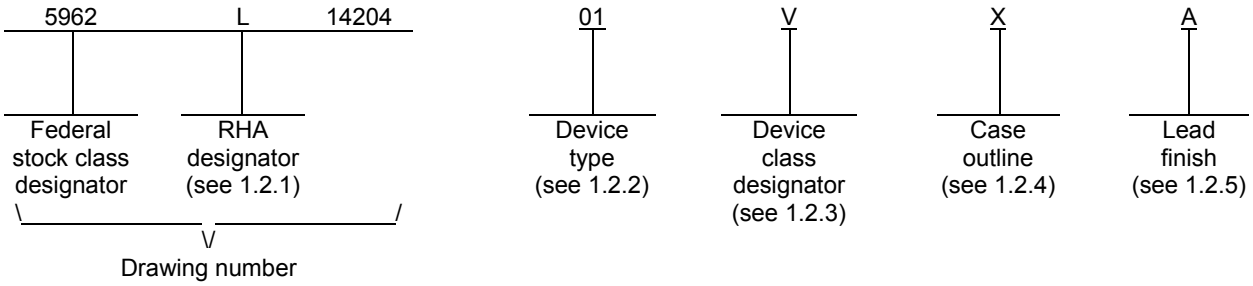
SIZE	CAGE CODE	
A	**67268**	**5962-14204**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADF4108S	Radiation hardened, 1 to 7 GHz phase locked loop frequency synthesizer
02	ADF4108S	Radiation hardened, 1 to 7 GHz phase locked loop frequency synthesizer

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F16	16	Bottom brazed flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

AV_{DD} to GND	-0.3 V to +3.9 V
AV_{DD} to DV_{DD}	-0.3 V to +0.3 V
V_P to GND	-0.3 V to +5.8 V
V_P to AV_{DD}	-0.3 V to +5.8 V
Digital I/O voltage to GND	-0.3 V to V_{DD} + 0.3 V
Analog I/O voltage to GND	-0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	-0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±600 mV
Operating temperature range (T_A)	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Lead temperature (soldering, 60 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	31°C/W 2/
Thermal resistance, junction-to-ambient (θ_{JA})	36°C/W 2/

1.4 Recommended operating conditions.

AV_{DD} = DV_{DD}	+3.2 V to +3.6 V
Charge pump power supply voltage (V_P)	V_{DD} to +5.5 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.4.1 Operating performance characteristics. 3/

RF frequency	1.0 GHz to 7.0 GHz
REF frequency	20 MHz to 250 MHz
Phase detector:	
Maximum sampling frequency	104 MHz
Logic input:	
Maximum input capacitance	10 pF
REF_{IN}:	
Maximum input capacitance	10 pF
Noise characteristics:	
Normalized phase noise floor (PN_{SYNTH})	-223 dBc/Hz 4/
Normalized 1/f noise (PN1_f)	-122 dBc/Hz 5/
Phase noise performance, 6835 MHz output	-81 dBc/Hz 6/
Spurious signals, 6835 MHz output	-82 dBc 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Measurement taken under absolute worst case conditions and represents data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package θ_{JC} numbers.

3/ Unless otherwise specified, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V, GND = AGND = DGND = CPGND = 0 V, V_{CP} = 5 V, R_{SET} = 5.1 kΩ, $RF_{IN}B$ capacitor coupled to ground.

4/ Phase lock loop (PLL) bandwidth = 500 kHz, measured at 100 kHz offset. The synthesizers phase noise is estimated by measuring the in-band phase noise at the output of the voltage controlled oscillator (VCO) and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. Therefore, $PN_{SYNTH} = PN_{TOT}$ - 10 log F_{PFD} – 20 log N.

5/ 10 kHz offset, normalized to 1 GHz. The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at a RF frequency, f_{RF}, and at a frequency f is given by PN = PN1_f + 10 log(10 kHz/f) – 10 log (f_{RF} / 1 GHZ).

6/ At VCO output and 1 kHz offset, f_{REFIN} = 10 MHz, f_{PFD} = 1 MHz, f_{RF} = 6835 MHz, N = 6835 ; Loop bandwidth = 30 kHz, VCO with +10 dB RF amplifier so that the PLL RF_{IN} = +5 dBm.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) :
Device type 01: ..... 50 krads(Si) 7/
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s) :
Device type 02 ..... 50 krads(Si) 8/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

7/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A for device type 01.
8/ For device type 02, radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply							
AV_{DD}, DV_{DD} supply voltage	V_{DD}	Pin AV_{DD}, DV_{DD}, with $AV_{DD} = DV_{DD}$	1, 2, 3	01, 02	3.2	3.6	V
		M, D, P, L	1		3.2	3.6	
V_{CP} supply voltage	V_{CP}	Pin V_P	1, 2, 3	01, 02	V_{DD}	5.5	V
		M, D, P, L	1		V_{DD}	5.5	
I_{DD} supply current	I_{DD}	Pin AV_{DD}, DV_{DD}, 4/ tested over supply range, $I_{DD} = AI_{DD} + DI_{DD}$, RF = 5 GHz	1, 2, 3	01, 02		17	mA
		M, D, P, L	1			17	
I_P supply current	I_{CP}	Pin V_P, 4/ tested over supply range,	1, 2, 3	01, 02		0.4	mA
		M, D, P, L	1			0.4	
I_{DD} power down current	I_{DIS}	$A_{IDD} + D_{IDD}$ power down, 4/ 5/ V_{CP} power down	1, 2, 3	01, 02		10	µA
		M, D, P, L	1			15	
Charge Pump, pin CP							
I_{CP} source high value	$I_{CP}8up$	With R_{SET} = 5.1 kΩ	1, 2, 3	01, 02	2.5	7.5	mA
		M, D, P, L	1		2.5	7.5	
I_{CP} sink high value	$I_{CP}8dwn$	With R_{SET} = 5.1 kΩ	1, 2, 3	01, 02	-7.5	-2.5	mA
		M, D, P, L	1		-7.5	-2.5	
I_{CP} source low value	$I_{CP}1up$	With R_{SET} = 5.1 kΩ	1, 2, 3	01, 02	0.125	1.250	mA
		M, D, P, L	1		0.125	1.250	
I_{CP} sink low value	$I_{CP}1dwn$	With R_{SET} = 5.1 kΩ	1, 2, 3	01, 02	-1.25	-0.125	mA
		M, D, P, L	1		-1.25	-0.125	
I_{CP} sink/source absolute accuracy	$I_{CP}8_{AbsAcc}$		1, 2, 3	01, 02	-10	10	%
		M, D, P, L	1		-10	10	
I_{CP} sink/source R_{SET} range	R_{SETRng}	6/	1, 2, 3	01, 02	3.0	11.0	kΩ
I_{CP} three-state leakage	I_{CP}_lkg		1, 2, 3	01, 02	-15	15	nA
		M, D, P, L	1		-20	20	
I_{CP} sink/source current matching	I_{CP}_m	$I_{CP}1 - I_{CP}8$, With R_{SET} = 5.1 kΩ	1, 2, 3	01, 02	-10	10	%
		M, D, P, L	1		-10	10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Charge Pump, pin CP – continued.							
I_{CP} versus V_{CP}	$I_{CP}\_V_{CP}$	With R_{SET} = 5.1 kΩ, $0.5\ V \le V_{CP} \le V_P - 0.5\ V$	1, 2, 3	01, 02	-8	8	%
		M, D, P, L	1		-8	8	
I_{CP} versus temperature	I_{CP}_T	With R_{SET} = 5.1 kΩ, 6/ $V_{CP} = V_P/2$	1, 2, 3	01, 02	-5	5	%
R_{SET} output voltage	V_{RSET}	With R_{SET} = 5.1 kΩ,	1, 2, 3	01, 02	0.5	0.7	V
		M, D, P, L	1		0.5	0.7	
Logic inputs, pins CE, LE, CLK, DATA							
Input high voltage	V_{IH}		1, 2, 3	01, 02	1.4	V_{DD}	V
		M, D, P, L	1		1.4	V_{DD}	
Input low voltage	V_{IL}		1, 2, 3	01, 02	0	0.6	V
		M, D, P, L	1		0	0.6	
Input high/low leakage current	I_{INH}, I_{INL}	Voltage of I_{NH} = 3.2 V, Voltage of I_{NL} = 0.1 V	1, 2, 3	01, 02	-1	1	µA
		M, D, P, L	1		-1	1	
Logic outputs, pin MUXOUT							
N-channel output high voltage	V_{OH}	1 kΩ pull-up resistor to 1.8 V	1, 2, 3	01, 02	1.4		V
		M, D, P, L	1		1.4		
CMOS output high voltage	V_{OH}	I_{OH} = 500 µA 7/	1, 2, 3	01, 02	2.9		V
		M, D, P, L	1		2.9		
Output low voltage	V_{OL}	I_{OL} = 500 µA	1, 2, 3	01, 02		0.4	V
		M, D, P, L	1			0.4	
Output high/low leakage current	I_{OH}, I_{OL}	Voltage of IOH = 3.2 V, Voltage of IOL = 0.1 V, MUXOUT tri-stated	1, 2, 3	01, 02	-100	100	µA
		M, D, P, L	1		-100	100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device Type	Limits		Unit
						Min	Max	
RF_{IN} characteristics, pin $RF_{IN}A$, $RF_{IN}B$								
RF_{IN} input frequency	RF_{FREQ}	Tested at V_{DD}/V_{CP} = 3.6/3.6; 3.6/5.5; 3.2/3.2		4, 5, 6	01, 02	1	5	GHz
			M, D, P, L	4		1	5	
RF_{IN} input frequency	RF_{FREQ}	6/		4, 5, 6	01, 02		7	GHz
RF_{IN} input sensitivity	RF|v|			4, 5, 6	01, 02	-5	5	dBm
			M, D, P, L	4		-5	5	
Maximum allowable prescaler output frequency	F_{PRESC}	Prescaler = 8, tested at V_{DD}/V_{CP} = 3.6/5.5; 3.2/3.2		4, 5, 6	01, 02		300	MHz
		8/	M, D, P, L	4			300	
REF_{IN} characteristics, pin REF_{IN}								
REF_{IN} input frequency	REF_{FREQ}			4, 5, 6	01, 02	20	250	MHz
			M, D, P, L	4		20	250	
REF_{IN} input sensitivity	REF|v|	AC coupling ensures bias = $AV_{DD/2}$		4, 5, 6	01, 02	0.8	V_{DD}	V_{P-P}
			M, D, P, L	4		0.8	V_{DD}	
REF_{IN} input high/low current	REF_LIN			4, 5, 6	01, 02	-100	100	µA
			M, D, P, L	4		-100	100	
Timing								
Data to clock setup time	t_1	See figure 3		9, 10, 11	01, 02	10		ns
			M, D, P, L	9		10		
Data to clock hold time	t_2	See figure 3		9, 10, 11	01, 02	10		ns
			M, D, P, L	9		10		
Clock high time	t_3	See figure 3		9, 10, 11	01, 02	25		ns
			M, D, P, L	9		25		
Clock low time	t_4	See figure 3		9, 10, 11	01, 02	25		ns
			M, D, P, L	9		25		
Data to LE setup time	t_5	See figure 3		9, 10, 11	01, 02	10		ns
			M, D, P, L	9		10		
LE pulse width	t_6	See figure 3		9, 10, 11	01, 02	20		ns
			M, D, P, L	9		20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Device types 01 and 02 supplied to this drawing has been characterized through all levels M, D, P, L of irradiation. However, device type 01 and 02 are only tested at the "L" level. Pre and post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurement for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A for device type 01 and condition D for device type 02. Device type 02 has been tested at low dose rate condition D.

3/ AV_{DD} = DV_{DD} = 3.3 V, GND = AGND = DGND = CPGND = 0 V, V_{CP} = 5 V, R_{SET} = 5.1 kΩ, RF level = 0 dBm, REF level = 0.8 V_{P-P}, $RF_{IN}B$ capacitor coupled to ground unless otherwise specified. Values are relative to 50 Ω.

4/ P = 64/65, R = 50, A = 468, f_{PFD} = 200 kHz, REF = 10 MHz.

5/ I_{DIS} tested under four conditions:
1. Initial power reset.
2. CE = 0.2 V
3. CE = 3.0 V and function latch bit DB21/DB3 = 01.
4. CE = 3.0 V and function latch bit DB21/DB3 = 11.

6/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots. Parameter is not tested post radiation.

7/ V_{OH} minimum limit is dependent on V_{DD} chosen by the formula : V_{IH} min = V_{DD} – 0.4 V. Table I limits for default test condition of V_{DD} = 3.3 V.

8/ This parameter is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/ompliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

Device type	01, 02
Case outline	X
Terminal number	Terminal symbol
1	R_{SET}
2	CP
3	CPGND
4	AGND
5	$RF_{IN}B$
6	$RF_{IN}A$
7	AV_{DD}
8	REF_{IN}
9	DGND
10	CE
11	CLK
12	DATA
13	LE
14	MUXOUT
15	DV_{DD}
16	V_P

FIGURE 1. Terminal connections.

Terminal symbol	Type	Description
R_{SET}	Analog input	Bias for charge pump. Connecting a resistor between this pin and CPGND sets the maximum charge pump current to: I_{CP} max = 25.5 V/ R_{SET}. The nominal output voltage is 0.66 V.
CP	Analog output	Charge pump output. When enabled, this pin provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
CPGND	Ground	Charge pump ground. Connect to low impedance ground.
AGND	Ground	Analog ground. Connect to low impedance ground.
$RF_{IN}B$	Analog input	Complementary input to the RF prescaler. This pin must be decoupled to ground plane with a small bypass capacitor, typically 100 pF.
$RF_{IN}A$	Analog input	Input to the RF prescaler. This pin must be ac coupled to external VCO.
AV_{DD}	Power	Analog supply voltage. 3.2 V to 3.6 V. AV_{DD} and DV_{DD} should be tied together externally and properly bypassed.
REF_{IN}	Analog input	Reference input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ.
DGND	Ground	Digital ground. Connect to low impedance ground.
CE	Digital input	Chip enable. High impedance CMOS input. A logic low on this pin powers down the part and puts the charge pump output into three-state mode.
CLK	Digital input	Serial clock input. High impedance CMOS input. Used to clock in serial data to registers.
DATA	Digital input	Serial data input. High impedance CMOS input. Data loaded most significant bit (MSB) first with the 2 LSBs being the control bits.
LE	Digital input	Load enable. High impedance CMOS input. When LE rises, shift register data is loaded into one of four latches selected using the control bits.
MUXOUT	Digital input	Multiplexer output. Allows either the SD Out, the Analog or Digital lock detect lock detect, the scaled RF, or the scaled REF frequency to be accessed externally.
DV_{DD}	Power	Digital supply voltage. 3.2 V to 3.6 V. AV_{DD} and DV_{DD} should be tied together externally and properly bypassed.
V_P	Power	Charge pump power supply. Must be greater than or equal to V_{DD} and less than 5.5 V.

FIGURE 1. Terminal connections – continued.

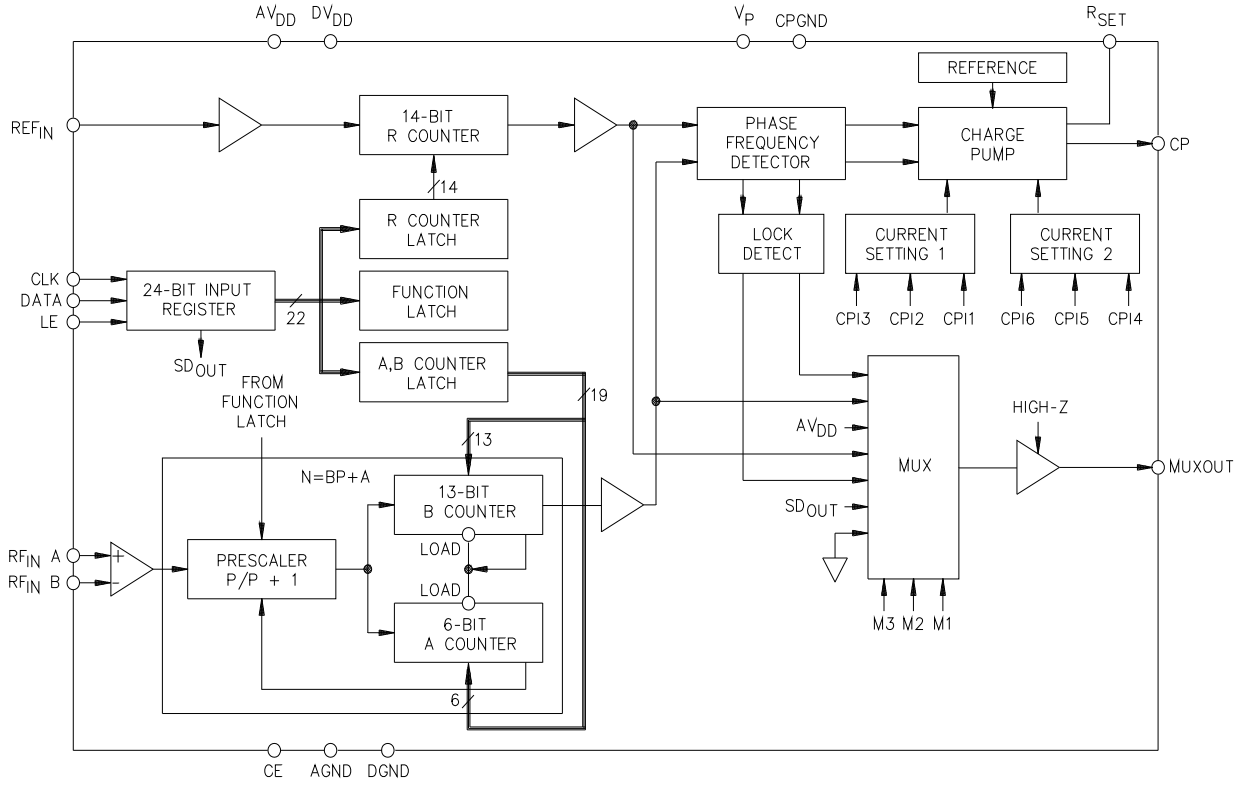


FIGURE 2. Block diagram.

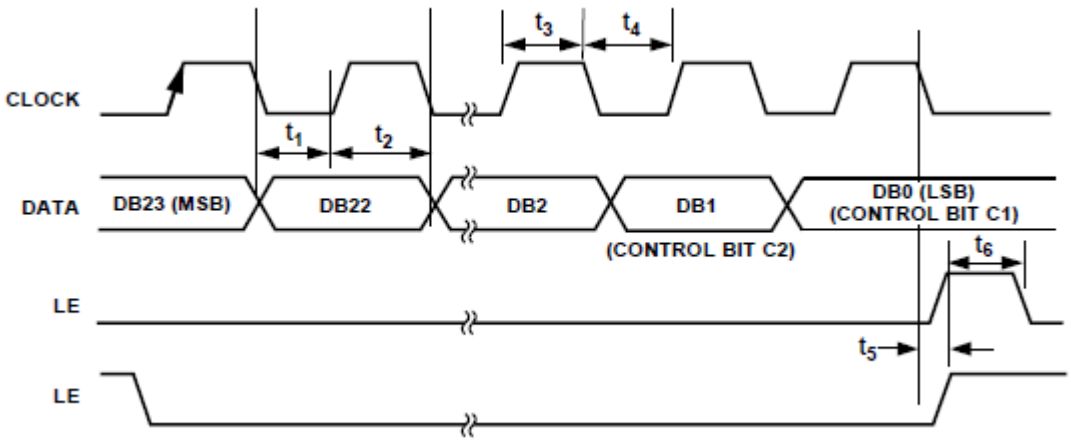


FIGURE 3. Timing waveform.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 9,10,11 1/ 2/	1,2,3,4,5,6 9,10,11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 9,10,11 3/
Group D end-point electrical parameters (see 4.4)	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 9,10,11
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9

1/ PDA applies to subgroup 1 only. Deltas are not excluded from PDA
2/ Parameters marked with footnote 6/ in Table I are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Delta limits as specified in Table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. 1/

Parameter	Device types	Symbol	Condition	Limits		Units
				Min	Max	
I_{DD} Supply current	01, 02	I_{DD}	V_{DD} = 3.6 V, V_{CP} = 5.5 V	-0.4	+0.4	mA
I_{CP} Supply current	01, 02	I_{CP}	V_{DD} = 3.6 V, V_{CP} = 5.5 V	-0.05	+0.05	mA
R_{SET} output voltage	01, 02	V_{RSET}	V_{DD} = 3.2 V, V_{CP} = 5.5 V	-0.06	+0.06	V
I_{CP} sink/source current high value	01, 02	I_{CP8}	V_{DD} = 3.3 V, V_{CP} = 5.5 V	-0.35	+0.35	mA
I_{CP} sink/source current low value	01, 02	I_{CP1}	V_{DD} = 3.3 V, V_{CP} = 5.5 V	-0.08	+0.08	mA
Input high/low leakage current	01, 02	I_{IH}/I_{IL}	V_{DD} = 3.3 V, V_{CP} = 5 V	-50	+50	nA

1/ 240 hour burn-in and group C end point electrical parameters. Deltas are performed at T_A = +25°C.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and condition D for device type 02, and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Application notes.

6.7.1 REFERENCE INPUT STAGE. The reference input stage is shown in Figure 4. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

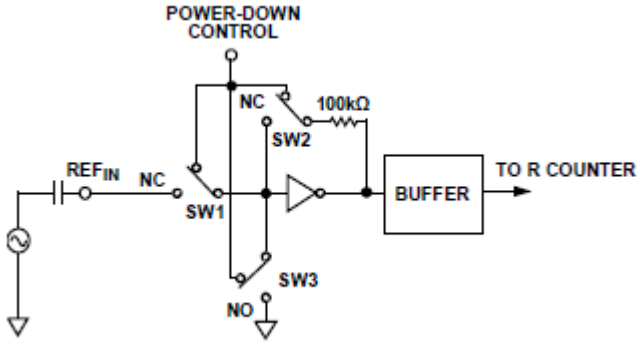


Figure 4. Reference Input Stage

6.7.2 RF INPUT STAGE. The RF input stage is shown in Figure 5. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

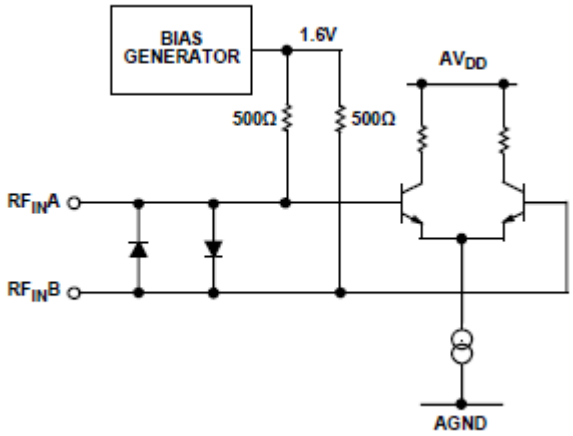


Figure 5. Reference Input Stage

6.7.3 PRESCALER (P/P + 1). The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. A minimum divide ratio is possible for contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by $(P^2 - P)$.

6.7.4 A AND B COUNTERS. The A and B CMOS counters shown in Figure 6 combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

6.7.4.1 Pulse Swallow Function. The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN} / R$$

Where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO), P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, and so on), B is the preset divide ratio of binary 13-bit counter (3 to 8191). *A* is the preset divide ratio of binary 6-bit swallow counter (0 to 63). f_{REFIN} is the external reference frequency oscillator.

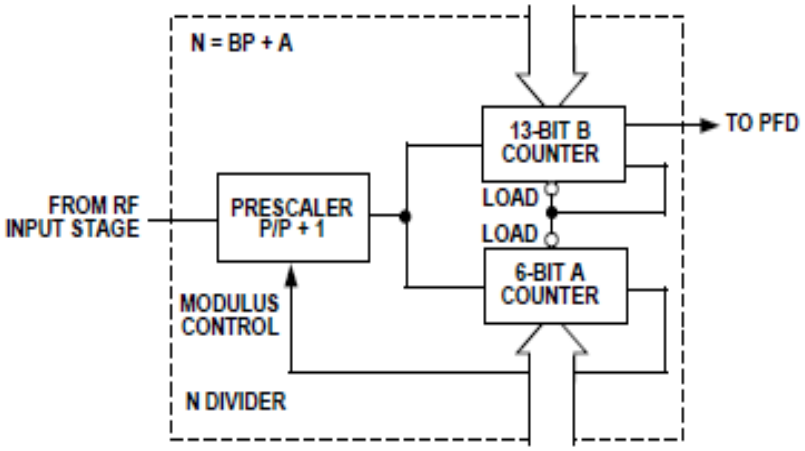


Figure 6. A and B Counters.

6.7.5 R COUNTER. The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

6.7.6 PHASE FREQUENCY DETECTOR AND CHARGE PUMP. The phase frequency detector (PFD) takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 7 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse (contact the manufacturer for further details on Reference Counter Latch Map). Use of the minimum antibacklash pulse width is not recommended.

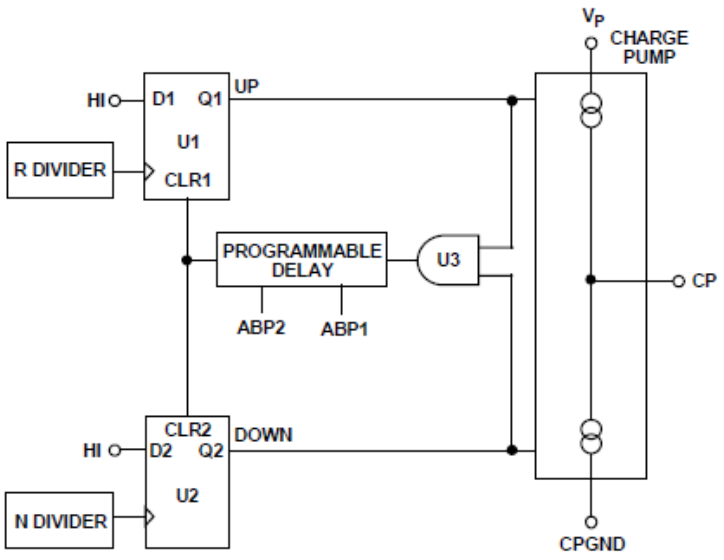


Figure 7. PFD Simplified Schematic and Timing (in Lock).

6.7.7 MUXOUT AND LOCK DETECT. The output multiplexer on the device allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Contact the manufacturer for information regarding the truth table in the AB Counter Latch Map. Figure 9 shows the MUXOUT section in block diagram form.

6.7.7.1 Lock Detect. MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect. Digital lock detect is active high. When the lock detect precision (LDP) bit in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output is high with narrow, low going pulses.

6.7.8 INPUT SHIFT REGISTER. The devices digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the 2 LSBs, DB1 and DB0, as shown in the timing diagram of Figure 3. The truth table for these bits is shown in Table III. Contact the manufacturer for a summary of how the latches are programmed in the Latch Summary.

Table III. C2 and C1 truth table.

Control bits		Data latch
C2	C1	
0	0	R counter
0	1	N counter (A and B)
1	0	Function latch (including prescaler)
1	1	Initialization latch

6.7.9 FUNCTION LATCH. The on-chip function latch is programmed with C2 and C1 set to 1 and 0, respectively. Contact the manufacturer for the Function Latch Map for the input data format for programming the function latch.

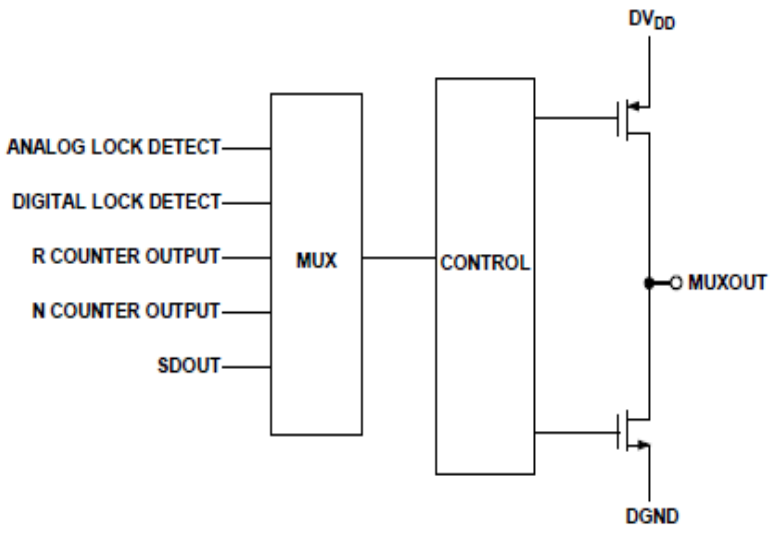


Figure 9. MUXOUT Circuit.

6.7.9.1 Counter Reset. DB2 (F1) is the counter reset bit. When this bit is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit needs to be disabled (set to 0). Then, the N counter resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle.)

6.7.9.2 Power-Down. DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin. When the CE pin is low, the device is immediately disabled regardless of the states of PD2 and PD1. In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into the PD1 bit, with the condition that PD2 has been loaded with a 0. In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into PD1 (on condition that a 1 has also been loaded to PD2), the device goes into power-down on the occurrence of the next charge pump event. When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

6.7.9.3 MUXOUT Control. The on-chip multiplexer is controlled by M3, M2, and M1 on the device. Contact the manufacturer for the Function Latch Map for the truth table.

6.7.9.4 Fastlock Enable Bit. DB9 of the function latch is the fastlock enable bit. Fastlock is enabled only when this bit is 1.

6.7.9.5 Fastlock Mode Bit. DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1. The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2. The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4:TC1, the CP gain bit in the AB counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. Contact the manufacturer for the Function Latch Map for the timeout periods.

6.7.9.6 Timer Counter Control. The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed).
The normal sequence of events is as follows:
The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2. At the same time, it must be decided how long the secondary current is to stay active before reverting to the primary current. This is controlled by the timer counter control bits, DB14:DB11 (TC4:TC1) in the function latch. Contact the manufacturer for the Function Latch Map for the truth table. Now, to program a new output frequency, the user simply programs the AB counter latch with new values for A and B. At the same time, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6:CPI4 for a period of time determined by TC4:TC1. When this time is up, the charge pump current reverts to the value set by CPI3:CPI1. At the same time, the CP gain bit in the AB counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency. Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

6.7.9.7 Charge Pump Currents. CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. Contact the manufacturer for the truth table in the Function Latch Map.

6.7.9.8 Prescaler Value. P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 300 MHz. Thus, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

6.7.9.9 PD Polarity. This bit sets the phase detector polarity bit. Contact the manufacturer for further details in the Function Latch Map.

6.7.9.10 CP Three-State. This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

6.7.10 INITIALIZATION LATCH. The initialization latch is programmed when C2 and C1 are set to 1 and 1. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0). Contact the manufacturer for further details in the initialization Latch Map. However, when the initialization latch is programmed, an additional internal reset pulse is applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched and the device will begin counting in close phase alignment. If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse and so close phase alignment is maintained when counting resumes. When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB counter loads after this do not trigger the internal reset pulse.

6.7.10.1 Device Programming After Initial Power-Up. After initially powering up the device, there are three ways to program the device.

Initialization Latch Method
1. Apply V_{DD}.
2. Program the initialization latch (11 in 2 LSBs of input word). Make sure that the F1 bit is programmed to 0.
3. Next, do a function latch load (10 in 2 LSBs of the control word), making sure that the F1 bit is programmed to a 0.
4. Then do an R load (00 in 2 LSBs).
5. Then do an AB load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:
1. The function latch contents are loaded.
2. An internal pulse resets the R, AB, and timeout counters to load state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first AB counter data after the initialization word activates the same internal reset pulse. Successive AB loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method
1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the AB counter latch (01).
6. Bring CE high to take the device out of power-down. The R and AB counters will now resume counting in close alignment.

Note that after CE goes high, a duration of 1 µs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state. CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after VDD was initially applied.

Counter Reset Method
1. Apply V_{DD}.
2. Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in 2 LSBs).
4. Do an AB counter load (01 in 2 LSBs).
5. Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

6.7.11 INTERFACING. This device has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 3 for the timing diagram and Table III for the latch truth table. The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-08-12

Approved sources of supply for SMD 5962-14204 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962L1420401VXA	24355	ADF4108L703F
5962L1420402VXA	24355	ADF4108L803F

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605