REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make correction to group A subgroups 2 and 3 for output voltage high (V_{OH}), test with conditions V_S = ±15.0 V and R_L = 2 kΩ in table I. - rrp	15-12-01	C. SAFFLE
B	Add RHA device type 02. Add footnote 3/ to all three Offset voltage drift tests as specified under table I. – ro	17-01-26	C. SAFFLE
C	Make correction to the power dissipation limit from 32 mW to 288 mW as specified under paragraph 1.3. - ro	20-06-25	J. ESCHMEYER
D	Change descriptor 'Power dissipation (P_D)' in section 1.3 to 'Continuous power dissipation (P_D)' and add corresponding technical guidance and new footnote 4/ guidance, per request from vendor CAGE 24355, and then change footnote 4/ and 5/ in previous revision, to footnotes 5/ and 6/. In table I, add new footnote 6/ to 'Short circuit current' test per request from vendor CAGE 24355. Deleted section 6.7 (pg 20-29 of rev C) per request from vendor CAGE 24355; was commercial datasheet information not meant for inclusion in the original drawing - cgh.	26-02-24	J. ESCHMEYER

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV																						
SHEET																						
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
RICK OFFICER

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
15-01-15

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

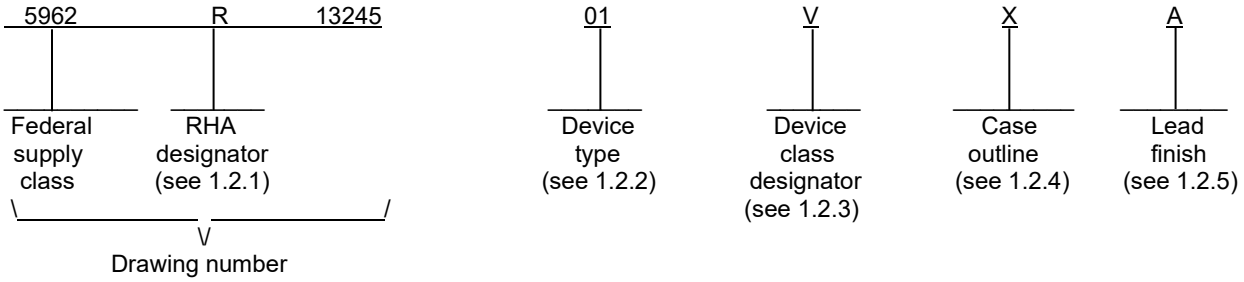
MICROCIRCUIT, LINEAR, 30 V, LOW NOISE, LOW POWER DUAL, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-13245**
		SHEET	1 OF 19	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADA4084-2	Radiation hardened 30 V low noise, low power dual operational amplifier
02	ADA4084-2	Radiation hardened 30 V low noise, low power dual operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F10	10	Bottom brazed flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage ($+V_S$ to $-V_S$)	36 V
Input voltage (V_{IN})	$-V_S$ to $+V_S$
Differential input voltage	±0.6 V 2/
Output short circuit duration to GND	Indefinite
Continuous power dissipation (P_D):	
T_A = +125°C	288 mW 4/
T_A > +125°C, derate P_D for each °C above +125°C	P_D – [(Δ°C) * 19.2 mW/°C] 4/
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+140°C
Lead temperature (soldering, 60 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	40°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	52°C/W

1.4 Recommended operating conditions.

Supply voltage ($+V_S$ to $-V_S$)	±1.5 V to ±15 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.4.1 Operating performance characteristics.

V_S = ±1.5 V

Differential input resistance	100 kΩ 3/
Differential input capacitance	1.1 pF 3/
Common mode input resistance	80 MΩ 3/
Common mode input capacitance	2.9 pF 3/
Unity gain crossover, V_{IN} = 5 V_{PP}, R_L = 10 kΩ, A_V = 1	8.08 MHz
Phase margin	86 Degrees
Current noise density, f = 1 kHz	0.55 pA / $\sqrt{Hz}$

V_S = ±5.0 V

Differential input resistance	100 kΩ 3/
Differential input capacitance	1.1 pF 3/
Common mode input resistance	200 MΩ 3/
Common mode input capacitance	2.5 pF 3/
Unity gain crossover, V_{IN} = 5 V_{PP}, R_L = 10 kΩ, A_V = 1	9.6 MHz
Phase margin	85 Degrees
Current noise density	0.55 pA / $\sqrt{Hz}$

V_S = ±15.0 V

Differential input resistance	100 kΩ 3/
Differential input capacitance	1.1 pF 3/
Common mode input resistance	200 MΩ 3/
Common mode input capacitance	2.5 pF 3/
Unity gain crossover, V_{IN} = 5 V_{PP}, R_L = 10 kΩ, A_V = 1	9.9 MHz
Phase margin	86 Degrees
Current noise density	0.55 pA / $\sqrt{Hz}$

See footnotes on next page.

1.5 Radiation features.

Device type 01:
Maximum total dose available (dose rate = 50 – 300 rad(Si)/s)..... 100 krad(Si) 5/
Device type 02:
Maximum total dose available (dose rate ≤ 10 mrad(Si)/s)..... 50 krad(Si) 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ For input differential voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.
3/ Measurement taken under absolute worst case condition of still air and represent data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package θ_{JC} thermal numbers with smaller die size.
4/ While device types 01 and 02 are capable of short-term operation at junction temperatures (T_J) exceeding +140°C up to +175°C, operating these device types with a junction temperature exceeding +140°F will degrade the device Mean Time To Failure (MTTF). The extent of the MTTF reduction is dependent on the duration of exposure to a junction temperature exceeding +140°F.
5/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate sensitivity (ELDRS) effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.
6/ For device type 02, radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ V_S = ±1.5 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
INPUT CHARACTERISTICS.								
Offset voltage	V_{OS}			1	01, 02	-100	100	µV
				2, 3		-200	200	
			P, L, R	1	01	-100	100	
			P, L	1	02	-100	100	
Offset voltage drift 3/	$\Delta V_{OS}/\Delta T$			2, 3	01, 02	---	1.75	µV/°C
Offset voltage matching		Channel A versus Channel B		1, 2, 3	01, 02	---	150	µV
			P, L, R	1	01	---	150	
			P, L	1	02	---	150	
Input bias current	I_B			1	01, 02	-300	300	nA
				2, 3		-450	450	
			P, L, R	1	01	-300	300	
			P, L	1	02	-300	300	
Input offset current	I_{OS}			1	01, 02	-25	25	nA
				2, 3		-50	50	
			P, L, R	1	01	-25	25	
			P, L	1	02	-25	25	
Input voltage range	V_{IN}			1, 2, 3	01, 02	-1.5	+1.5	V
			P, L, R	1	01	-1.5	+1.5	
			P, L	1	02	-1.5	+1.5	
Common mode rejection ratio	CMRR	V_{CM} = ±1.5 V		1	01, 02	64	---	dB
				2, 3		60	---	
			P, L, R	1	01	64	---	
			P, L	1	02	64	---	
Large signal voltage gain	A_{VO}	R_L = 2 kΩ, 1.3 V ≤ V_O ≤ +1.3 V		1	01, 02	100	---	dB
				2		96	---	
				3		94	---	
			P, L R	1	01	100	---	
			P, L	1	02	100	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±1.5 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
OUTPUT CHARACTERISTICS.								
Output voltage high	V_{OH}	R_L = 10 kΩ to V_{CM}		1, 2, 3	01, 02	1.4	---	V
			P, L, R	1	01	1.4	---	
			P, L	1	02	1.4	---	
		R_L = 2 kΩ to V_{CM}		1, 2, 3	01, 02	1.35	---	
			P, L, R	1	01	1.35	---	
			P, L	1	02	1.35	---	
Output voltage low	V_{OL}	R_L = 10 kΩ to V_{CM}		1, 2, 3	01, 02	---	-1.45	V
			P, L, R	1	01	---	-1.45	
			P, L	1	02	---	-1.45	
		R_L = 2 kΩ to V_{CM}		1	01, 02	---	-1.4	
				2, 3		---	-1.35	
			P, L, R	1	01	---	-1.4	
			P, L	1	02	---	-1.4	
Short circuit current 6/	I_{SC} source	Source		1, 2, 3	01, 02	-19	---	mA
			P, L, R	1	01	-19	---	
			P, L	1	02	-19	---	
	I_{SC} sink	Sink		1, 2, 3	01, 02	---	+20	
			P, L, R	1	01	---	+20	
			P, L	1	02	---	+20	
POWER SUPPLY.								
Power supply rejection ratio	PSRR	V_S = ±1.25 V to ±1.75 V		1	01, 02	100	---	dB
				2		90	---	
				3		80	---	
			P, L, R	1	01	100	---	
			P, L	1	02	100	---	
Supply current both amplifiers	I_S	I_O = 0 mA		1	01, 02	---	±1350	µA
				2, 3		---	±1900	
			P, L, R	1	01	---	±1350	
			P, L	1	02	---	±1350	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±1.5 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DYNAMIC PERFORMANCE.							
Slew rate 4/	SR	R_L = 2 kΩ	4	01, 02	1.7	---	V/µs
			5		2	---	
			6		1.3	---	
Gain bandwidth product 4/	GBP	V_{IN} = 5mV_{PP}, R_L = 10 kΩ, A_V = 100	4, 5, 6	01, 02	14.4	---	MHz
-3 dB closed loop bandwidth 4/	-3 dB	A_V = 1, V_{IN} = 5 mV_{PP}	4, 5	01, 02	11.3	---	MHz
			6		4.8	---	
NOISE PERFORMANCE.							
Voltage noise 4/	en_{pp}	0.1 Hz to 10 Hz	4	01, 02	---	0.2	µV_{PP}
			5, 6		---	0.22	
Voltage noise density 4/	e_n	f = 10 kHz	4	01, 02	---	3.7	nV/√Hz
			5		---	4.4	
			6		---	2.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±5.0 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
INPUT CHARACTERISTICS.								
Offset voltage	V_{OS}			1	01, 02	-100	100	µV
				2, 3		-200	200	
			P, L, R	1	01	-100	100	
			P, L	1	02	-100	100	
Offset voltage drift 3/	$\Delta V_{OS}/\Delta T$			2, 3	01, 02	---	1.75	µV/°C
Offset voltage matching		Channel A versus Channel B		1, 2, 3	01, 02	---	150	µV
			P, L, R	1	01	---	150	
			P, L	1	02	---	150	
Input bias current	I_B			1	01, 02	-300	300	nA
				2, 3		-450	450	
			P, L, R	1	01	-300	300	
			P, L	1	02	-300	300	
Input offset current	I_{OS}			1	01,02	-25	25	nA
				2, 3		-50	50	
			P, L, R	1	01	-25	25	
			P, L	1	02	-25	25	
Input voltage range	V_{IN}			1, 2, 3	01, 02	-5	+5	V
			P, L, R	1	01	-5	+5	
			P, L	1	02	-5	+5	
Common mode rejection ratio	CMRR	V_{CM} = ±4 V		1, 2, 3	01, 02	106	---	dB
			P, L, R	1	01	106	---	
			P, L	1	02	106	---	
		V_{CM} = ±5 V		1, 2, 3	01, 02	76	---	
			P, L, R	1	01	76	---	
			P, L	1	02	76	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±5.0 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
INPUT CHARACTERISTICS – continued.								
Large signal voltage gain	A_{VO}	R_L = 2 kΩ, -4 V ≤ V_O ≤ 4 V		1	01, 02	108	---	dB
				2		103	---	
				3		96	---	
			P, L, R	1	01	108	---	
			P, L	1	02	108	---	
OUTPUT CHARACTERISTICS.								
Output voltage high	V_{OH}	R_L = 10 kΩ to V_{CM}		1	01, 02	4.9	---	V
				2, 3		4.8	---	
			P, L, R	1	01	4.9	---	
			P, L	1	02	4.9	---	
		R_L = 2 kΩ to V_{CM}		1	01, 02	4.8	---	
				2, 3		4.7	---	
			P, L, R	1	01	4.8	---	
			P, L	1	02	4.8	---	
Output voltage low	V_{OL}	R_L = 10 kΩ to V_{CM}		1	01, 02	---	-4.9	V
				2, 3		---	-4.8	
			P, L, R	1	01	---	-4.9	
			P, L	1	02	---	-4.9	
		R_L = 2 kΩ to V_{CM}		1	01, 02	---	-4.8	
				2, 3		---	-4.7	
			P, L, R	1	01	---	-4.8	
			P, L	1	02	---	-4.8	
Short circuit current 6/	I_{SC} source	Source		1, 2, 3	01, 02	-36	---	mA
			P, L, R	1	01	-36	---	
			P, L	1	02	-36	---	
	I_{SC} sink	Sink		1, 2, 3	01, 02	---	+35	
			P, L, R	1	01	---	+35	
			P, L	1	02	---	+35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±5.0 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
POWER SUPPLY.								
Power supply rejection ratio	PSRR	V_S = ±2 V to ±18 V		1	01, 02	110	---	dB
				2, 3		105	---	
			P, L, R	1	01	110	---	
			P, L	1	02	110	---	
Supply current both amplifiers	I_S	I_O = 0 mA		1	01, 02	---	±1400	µA
				2, 3		---	±2000	
			P, L, R	1	01	---	±1400	
			P, L	1	02	---	±1400	
DYNAMIC PERFORMANCE.								
Slew rate 4/	SR	R_L = 2 kΩ to V_{CM}		4	01, 02	1.8	---	V/µs
				5		2.4	---	
				6		1.4	---	
Gain bandwidth product 4/	GBP	V_{IN} = 5 mV_{PP}, R_L = 10 kΩ, A_V = 100		4, 5, 6	01, 02	14.9	---	MHz
-3 dB closed loop bandwidth 4/	-3 dB	A_V = 1, V_{IN} = 5 mV_{PP}		4, 5	01, 02	12.9	---	MHz
				6		5.2	---	
NOISE PERFORMANCE.								
Voltage noise 4/	e_{nPP}	0.1 Hz to 10 Hz		4	01, 02	---	0.2	$µV_{PP}$
				5, 6		---	0.22	
Voltage noise density 4/	e_n	f = 10 kHz		4	01, 02	---	3.8	$nV/\sqrt{Hz}$
				5		---	4.5	
				6		---	2.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±15.0 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
INPUT CHARACTERISTICS.								
Offset voltage	V_{OS}			1	01, 02	-100	100	µV
				2, 3		-200	200	
			P, L, R	1	01	-100	100	
			P, L	1	02	-100	100	
Offset voltage drift 3/	$\Delta V_{OS}/\Delta T$			2, 3	01, 02	---	1.75	µV/°C
Offset voltage matching		Channel A versus Channel B		1	01, 02	---	150	µV
			P, L, R	1	01	---	150	
			P, L	1	02	---	150	
Input bias current	I_B			1	01, 02	-300	300	nA
				2, 3		-450	450	
			P, L, R	1	01	-300	300	
			P, L	1	02	-300	300	
Input offset current	I_{OS}			1	01, 02	-25	25	nA
				2, 3		-50	50	
			P, L, R	1	01	-25	25	
			P, L	1	02	-25	25	
Input voltage range	V_{IN}			1, 2, 3	01, 02	-15	+15	V
			P, L, R	1	01	-15	+15	
			P, L	1	02	-15	+15	
Common mode rejection ratio	CMRR	V_{CM} = ±14 V		1, 2, 3	01, 02	106	---	dB
			P, L, R	1	01	106	---	
			P, L	1	02	106	---	
		V_{CM} = ±15 V		1, 2, 3	01, 02	85	---	
			P, L, R	1	01	85	---	
			P, L	1	02	85	---	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±15.0 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
INPUT CHARACTERISTICS - continued.								
Large signal voltage gain	A_{VO}	R_L = 2 kΩ, -13.V ≤ V_O ≤ +13.5 V		1	01, 02	110	---	dB
				2		105	---	
				3		100	---	
			P, L, R	1	01	110	---	
			P, L	1	02	110	---	
OUTPUT CHARACTERISTICS.								
Output voltage high	V_{OH}	R_L = 10 kΩ to V_{CM}		1, 2, 3	01, 02	14.8	---	V
			P, L, R	1	01	14.8	---	
			P, L	1	02	14.8	---	
		R_L = 2 kΩ to V_{CM}		1, 2	01, 02	14.5	---	
				3		13.0	---	
			P, L, R	1	01	14.5	---	
			P, L	1	02	14.5	---	
Output voltage low	V_{OL}	R_L = 10 kΩ to V_{CM}		1	01, 02	---	-14.9	V
				2, 3		---	-14.8	
			P, L, R	1	01	---	-14.9	
			P, L	1	02	---	-14.9	
		R_L = 2 kΩ to V_{CM}		1	01, 02	---	-14.8	
				2, 3		---	-14.7	
			P, L, R	1	01	---	-14.8	
			P, L	1	02	---	-14.8	
Short circuit current 6/	I_{SC} source	Source		1, 2, 3	01, 02	-71	---	mA
			P, L, R	1	01	-71	---	
			P, L	1	02	-71	---	
	I_{SC} sink	Sink		1, 2, 3	01, 02	---	+35	
			P, L, R	1	01	---	+35	
			P, L	1	02	---	+35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ 2/ V_S = ±15.0 V, V_{CM} = 0 V, -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
POWER SUPPLY.								
Power supply rejection ratio	PSRR	V_S = ±2 V to ±18 V		1	01, 02	110	---	dB
				2, 3		105	---	
			P, L, R	1	01	110	---	
			P, L	1	02	110	---	
Supply current both amplifiers	I_S	I_O = 0 mA		1	01, 02	---	±1500	µA
				2, 3		---	±2100	
			P, L, R	1	01	---	±1500	
			P, L	1	02	---	±1500	
DYNAMIC PERFORMANCE.								
Slew rate 4/	SR	R_L = 2 kΩ		4	01, 02	1.9	---	V/µs
				5		2.4	---	
				6		1.5	---	
Gain bandwidth product 4/	GBP	V_{IN} = 5mV_{PP}, R_L = 10 kΩ, A_V = 100		4, 5, 6	01, 02	14.9	---	MHz
-3 dB closed loop bandwidth 4/	-3 dB	A_V = 1, V_{IN} = 5 mV_{PP}		4, 5	01, 02	12.9	---	MHz
				6		6	---	
NOISE PERFORMANCE.								
Voltage noise 3/ 5/	e_{nPP}	0.1 Hz to 10 Hz		4	01, 02	---	0.2	µV_{PP}
				5, 6		---	0.22	
Voltage noise density 4/	e_n	f = 1 kHz		4	01, 02	---	3.9	nV/√Hz
				5		---	4.6	
				6		---	3.1	

1/ Device type 01 supplied to this drawing has been characterized through all levels P, L, R of irradiation. Device type 02 supplied to this drawing has been characterized through all levels P, L, of irradiation. Pre and Post irradiation values are identical unless specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate sensitivity (ELDRS) effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A for device type 01 and condition D for device type 02. Device type 02 has been tested at low dose rate condition D.

3/ Not tested post irradiation.

4/ Parameter is part of device initial characterization which is only repeated after major design and process changes or with subsequent wafer lots. Not tested post irradiation.

5/ The test parameter e_{nPP} is 100% production tested at V_S = ±15 V, T_A = ambient temperature.

6/ Parameters are part of the initial characterization and qualification. Exposure to conditions above absolute maximum ratings for extended periods may affect device reliability.

Device types	01, 02	
Case outline	X	
Terminal number	Terminal symbol	Description
1	NC/GND	No connect or ground. No internal circuitry connected so user may ground pin if desired.
2	OUTA	Operational amplifier output, amplifier A.
3	-INA	Operational amplifier negative input, amplifier A.
4	+INA	Operational amplifier positive input, amplifier A.
5	$-V_S$	Negative power supply.
6	NC/GND	No connect or ground. No internal circuitry connected so user may ground pin if desired.
7	+INB	Operational amplifier positive input, amplifier B.
8	-INB	Operational amplifier negative input, amplifier B.
9	OUTB	Operational amplifier output, amplifier B.
10	$+V_S$	Positive power supply.

FIGURE 1. Terminal connections.

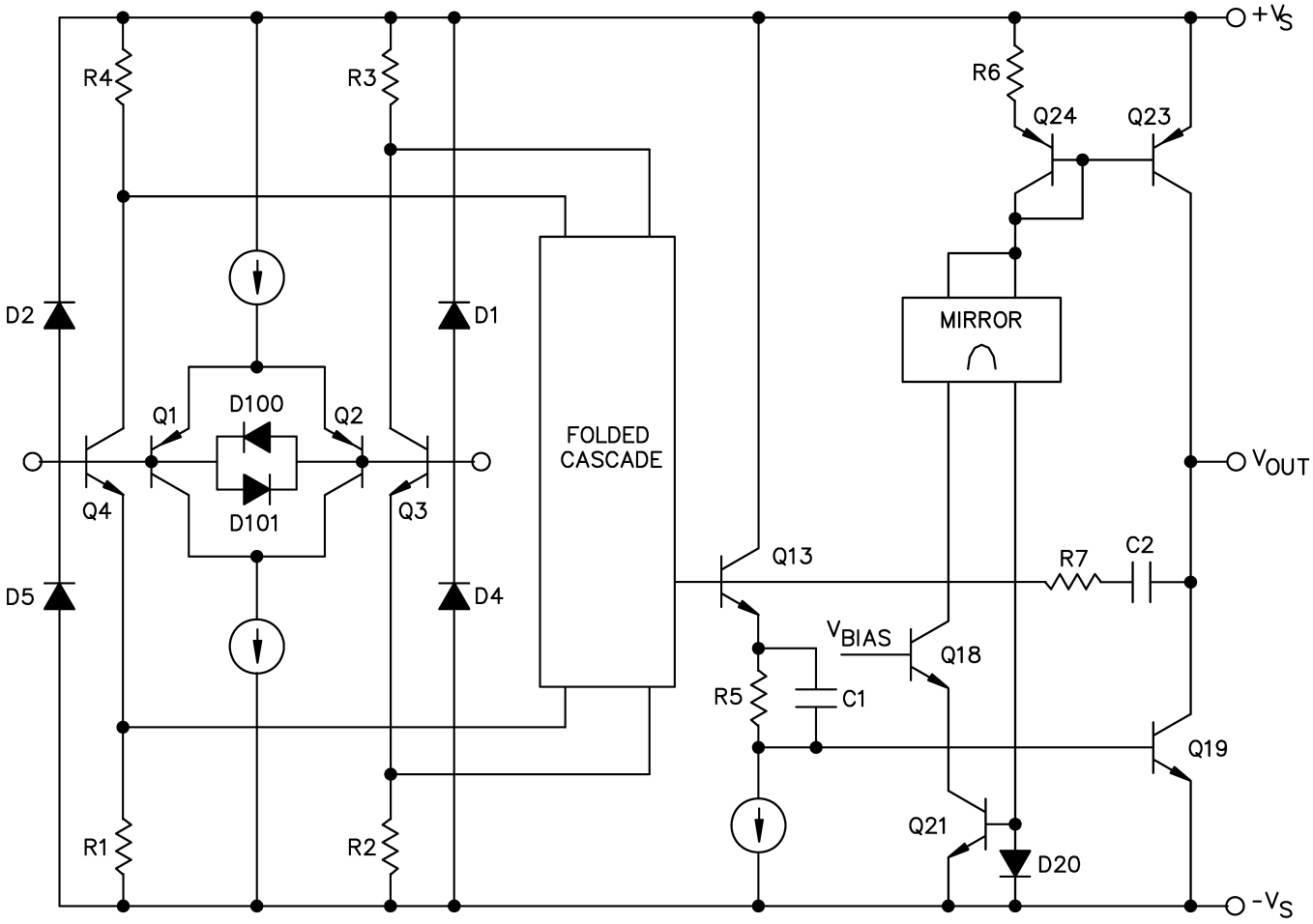


FIGURE 2. Block diagram.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 5, and 6 are tested as part of device initial characterization and after design and process changes or with subsequent wafer lots as indicated in table I.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6 1/	1, 2, 3, 4, 5, 6 1/ 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4 2/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. 1/

Parameters	Symbol	Delta limits	Units
Supply current at V_S = ±1.5 V	I_S	±33	µA
Supply current at V_S = ±5 V	I_S	±21	µA
Supply current at V_S = ±15 V	I_S	±12	µA
Offset voltage at V_S = ±1.5 V	V_{OS}	±36	µV
Offset voltage at V_S = ±5 V	V_{OS}	±35	µV
Offset voltage at V_S = ±15 V	V_{OS}	±35	µV
Input bias current at V_S = ±1.5 V	I_B	±7	nA
Input bias current at V_S = ±5 V	I_B	±10	nA
Input bias current at V_S = ±15 V	I_B	±6	nA

1/ 240 hour burn in and group C end point electrical parameters. Deltas are performed at T_A = +25°C.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 693-9032.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 693-0178.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 26-02-24

Approved sources of supply for SMD 5962-13245 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1324501VXA	24355	ADA4084-2AF/QMLR
5962L1324502VXA	24355	ADA4084-2AF/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices, Inc. 1 Analog Way Wilmington, MA 01887