REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make correction to die size mils conversion measurements as specified under figure A-1. - ro	14-10-22	C. SAFFLE
B	Make correction to I_{OS} test descriptions by deleting the word “voltage” and replacing with the word “current” as specified under Table IA for both ±2.5 V and ±1.5 V sections. - ro	16-11-29	C. SAFFLE
C	Add device type 02. - ro	17-05-09	C. SAFFLE
D	Make change to Offset voltage tests and Input offset current tests as specified under Table IA and Table IIB for device type 01 only. Make change to Power supply rejection ratio tests as specified under Table IA for device type 01 only- ro	17-06-06	C. SAFFLE
E	Add device type 03. - ro	19-01-23	C. SAFFLE
F	Make correction to PSRR test condition column within V_S = ±2.5 V section as specified under Table IA. - ro	22-06-13	J. ESCHMEYER

Revision Status of Sheets

REV	F	F	F	F	F																	
SHEET	23	24	25	26	27																	
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	PREPARED BY RICK OFFICER CHECKED BY RAJESH PITHADIA	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**		
	APPROVED BY CHARLES F. SAFFLE DRAWING APPROVAL DATE 13-07-25	MICROCIRCUIT, LINEAR, 19 MHz, 40 V, LOW POWER, QUAD OPERATIONAL AMPLIFIER, MONOLITHIC SILICON		
AMSC N/A	REVISION LEVEL F	SIZE A	CAGE CODE **67268**	**5962-13214**
		SHEET 1 OF 27		

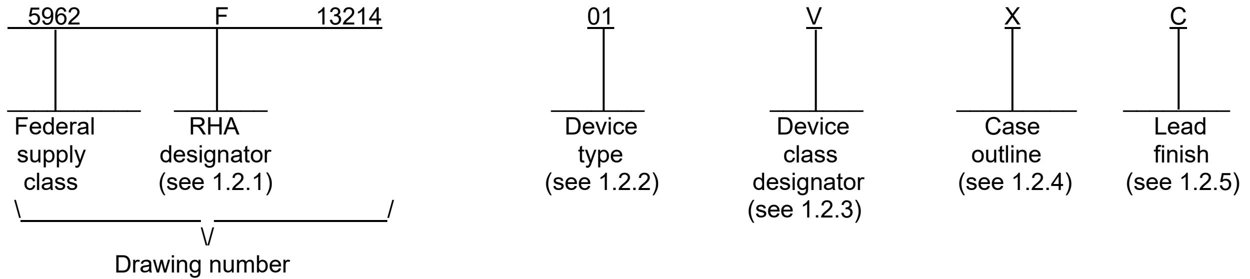
DSCC FORM 2233
APR 97 5962-E322-22

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70444SEH	Radiation hardened, 19 MHz, 40 V, low power, quad operational amplifier
02	ISL70444ASEH	Radiation hardened, 19 MHz, 40 V, low power, quad operational amplifier
03	ISL73444SEH	Radiation hardened, 19 MHz, 40 V, low power, quad operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Maximum supply voltage .... 42 V
Maximum differential input current .... 20 mA
Maximum differential input voltage .... 42 V or $-V_S - 0.5$ V to $+V_S + 0.5$ V
Minimum/maximum input voltage .... 42 V or $-V_S - 0.5$ V to $+V_S + 0.5$ V
Maximum/minimum current for input voltage $> +V_S$ or $< -V_S$ .... ±20 mA
Electrostatic discharge (ESD) ratings:
Human body model (HBM) .... 2 kV
Machine model (MM) .... 200 V
Charged device model (CDM) .... 750 V
Maximum junction temperature range (T_J) .... +150°C
Storage temperature range (T_{STG}) .... -65°C to +150°C
Thermal resistance, junction to case (θ_{JC}) .... 9°C/W 2/
Thermal resistance, junction to ambient (θ_{JA}) .... 35°C/W 3/

1.4 Recommended operating conditions.

Single supply voltage (V_S) .... 3 V ± 10% to 36 V ± 10%
Split rail supply voltage (V_S) .... ±1.5 V ± 10% to ±18 V ± 10%
Ambient operating temperature range (T_A) .... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s) :
Device types 01 and 02 .... 300 krad(Si) 4/
Maximum total dose available (low dose rate ≤ 10 mrad(Si)/s) :
Device types 01, 02 and 03 .... 50 krad(Si) 4/ 5/
Single event phenomena (SEP):
No SEL occurs at effective LET (see 4.4.4) .... ≤ 86 MeV/(mg/cm^2) 6/ 7/
No SEB occurs at surface LET (see 4.4.4) .... ≤ 86 MeV/(mg/cm^2) 6/ 7/
Single event transients (SET) observed at an effective LET (see 4.4.4)
(SET magnitude of ±10 mV with recovery time 2 μs at
cross section 1.58×10^{-5}cm^2) .... = 2.7 MeV/(mg/cm^2) 7/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For θ_{JC}, the “case temperature” location is the center of the package underside.

3/ θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air.

4/ Device types 01 and 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krad(Si), and condition D to a maximum total dose of 50 krad(Si). Manufacturer has performed ELDRS characterization to a level of 100 krad(si) and accelerated anneal testing to 1.5X over test (450 krad(Si)) and observed no time dependent effects. However, device types 01 and 02 may be ELDRS susceptible to low dose rate space environment at TID level above 100 krad(si).

5/ Device type 03 has been tested at low dose rate only. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total ionizing dose (TID) level of 50 krad(Si).

6/ Device types 01, 02 and 03 use silicon on insulator (SOI) technology. No single-event burnout (SEB) or single-event latchup (SEL) was observed when irradiated with gold (Au) ions at normal incidence, corresponding to a surface LET of 86 MeV/(mg/cm^2). The normal particle range into silicon for Au ions after 30 mm of air is about 118 μm and the Bragg peak range is 53 μm, resulting Au ion penetrate well beyond the sensitive volume of the devices.

7/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacture.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C V_S = ±18 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage	V_{OS}	V_{CM} = 0 V	1	01, 02, 03		400	µV
		V_{CM} = +V_S to -V_S	1,2,3,			500	
		V_{CM} = +V_S to -V_S , M,D,P,L,R,F 2/	1				
Input offset channel to channel match	ΔV_{OS}	V_{CM} = +V_S	1,2,3	01, 02, 03		800	µV
		V_{CM} = +V_S , M,D,P,L,R,F 2/	1				
		V_{CM} = -V_S	1,2,3			800	
		V_{CM} = -V_S , M,D,P,L,R,F 2/	1				
Input bias current	I_B	V_{CM} = 0 V	1,2,3	01, 03		370	nA
		V_{CM} = +V_S				370	
		V_{CM} = +V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = -V_S	1,2,3			650	
		V_{CM} = -V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = +V_S – 0.5 V	1,2,3			370	
		V_{CM} = -V_S + 0.5 V				650	
		V_{CM} = 0 V	1,2,3	02		500	
		V_{CM} = +V_S				500	
		V_{CM} = +V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = -V_S	1,2,3			650	
		V_{CM} = -V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = +V_S – 0.5 V	1,2,3			500	
		V_{CM} = -V_S + 0.5 V				650	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm18$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset current	I_{OS}	$V_{CM} = +V_S$ to $-V_S$	1	01, 02, 03	-30	+30	nA
			2,3		-50	+50	
		$V_{CM} = +V_S$ to $-V_S$, M,D,P,L,R,F 2/	1		-50	+50	
Common mode input voltage range	VCMIR		1,2,3	01, 02, 03	$-V_S$	$+V_S$	V
		M,D,P,L,R,F 2/	1				
Common mode rejection ratio	CMRR	$V_{CM} = -V_S$ to $+V_S$	1,2,3	01, 02, 03	70		dB
		$V_{CM} = -V_S$ to $+V_S$, M,D,P,L,R,F 2/	1				
		$V_{CM} = +V_S - 0.5$ V to $-V_S + 0.5$ V	1,2,3		80		
		$V_{CM} = +V_S - 0.5$ V to $-V_S + 0.5$ V, M,D,P,L,R,F 2/	1				
Power supply rejection ratio	PSRR	$-V_S = -18$ V, $+V_S = 0.5$ V to 18 V, $+V_S = 18$ V, $-V_S = -0.5$ V to -18 V	1,2,3	01, 02, 03	83		dB
		$-V_S = -18$ V, $+V_S = 0.5$ V to 18 V, $+V_S = 18$ V, $-V_S = -0.5$ V to -18 V, M,D,P,L,R,F 2/	1				
Open loop gain	A_{VOL}	$R_L = 10$ kΩ to ground	4,5,6	01, 03	96		dB
		$R_L = 10$ kΩ to ground, M,D,P,L,R,F 2/	4				
		$R_L = 10$ kΩ to ground	4,5,6	02	90		
		$R_L = 10$ kΩ to ground, M,D,P,L,R,F 2/	4				
Output voltage high (V_{OUT} to $+V_S$)	V_{OH}	R_L = no load	1,2,3	01, 02, 03		160	mV
		R_L = no load, M,D,P,L,R,F 2/	1				
		$R_L = 10$ kΩ	1,2,3			175	
		$R_L = 10$ kΩ, M,D,P,L,R,F 2/	1				

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_S = \pm18$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage low (V_{OUT} to $-V_S$)	V_{OL}	R_L = no load	1,2,3	01, 03		160	mV
		R_L = no load, M,D,P,L,R,F 2/	1			150	
		R_L = 10 kΩ	1,2,3			175	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1			165	
		R_L = no load	1,2,3	02		160	
		R_L = no load, M,D,P,L,R,F 2/	1			160	
		R_L = 10 kΩ	1,2,3			175	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1			175	
Output short circuit current	I_{SC}	Sourcing: V_{OUT} = -18 V, V_{IN} = 0 V	1,2,3	01, 02, 03		-10	mA
		Sourcing: V_{OUT} = -18 V, V_{IN} = 0 V, M,D,P,L,R,F 2/	1				
		Sinking: V_{OUT} = +18 V, V_{IN} = 0 V	1,2,3		10		
		Sinking: V_{OUT} = +18 V, V_{IN} = 0 V, M,D,P,L,R,F 2/	1				
Supply current/amplifier	I_S	Unity gain	1,2,3	01, 03		2.4	mA
		Unity gain, M,D,P,L,R,F 2/	1				
		Unity gain	1	02		2.4	
			2, 3			2.8	
		Unity gain, M,D,P,L,R,F 2/	1			2.4	
Large signal slew rate	SR	A_V = 1, R_L = 10 kΩ, V_O = 10 V_{PP}	4,5,6	01, 02, 03	60		V/µs
		A_V = 1, R_L = 10 kΩ, V_O = 10 V_{PP}, M,D,P,L,R,F 2/	4				

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_S = \pm 2.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage	V_{OS}	V_{CM} = 0 V	1	01, 02, 03		400	µV
		V_{CM} = +V_S to –V_S	1,2,3			500	
		V_{CM} = +V_S to –V_S , M,D,P,L,R,F 2/	1				
Input offset channel to channel match	ΔV_{OS}	V_{CM} = +V_S	1,2,3	01, 02		800	µV
		V_{CM} = +V_S , M,D,P,L,R,F 2/	1				
		V_{CM} = -V_S	1,2,3			800	
		V_{CM} = -V_S , M,D,P,L,R,F 2/	1				
Input bias current	I_B	V_{CM} = 0 V	1,2,3	01, 03		340	nA
		V_{CM} = +V_S				340	
		V_{CM} = +V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = -V_S	1,2,3			580	
		V_{CM} = -V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = +V_S – 0.5 V	1,2,3			340	
		V_{CM} = -V_S + 0.5 V				580	
		V_{CM} = 0 V	1,2,3	02		400	
		V_{CM} = +V_S				400	
		V_{CM} = +V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = -V_S	1,2,3			580	
		V_{CM} = -V_S , M,D,P,L,R,F 2/	1			650	
		V_{CM} = +V_S – 0.5 V	1,2,3			400	
		V_{CM} = -V_S + 0.5 V				580	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 2.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset current	I_{OS}	$V_{CM} = +V_S$ to $-V_S$	1	01, 02, 03	-30	+30	nA
			2,3		-50	+50	
		$V_{CM} = +V_S$ to $-V_S$, M,D,P,L,R,F 2/	1		-50	+50	
Common mode input voltage range	VCMIR		1,2,3	01, 02, 03	$-V_S$	$+V_S$	V
		M,D,P,L,R,F 2/	1				
Common mode rejection ratio	CMRR	$V_{CM} = -V_S$ to $+V_S$	1,2,3	01, 02, 03	70		dB
		$V_{CM} = -V_S$ to $+V_S$, M,D,P,L,R,F 2/	1				
		$V_{CM} = +V_S - 0.5$ V to $-V_S + 0.5$ V	1,2,3		74		
		$V_{CM} = +V_S - 0.5$ V to $-V_S + 0.5$ V, M,D,P,L,R,F 2/	1				
Power supply rejection ratio	PSRR	$-V_S = -2.5$ V, $+V_S = 2.5$ V to 4.5 V, $+V_S = 2.5$ V, $-V_S = -2.5$ V to -4.5 V	1,2	01,02, 03	80		dB
			3		70		
		$-V_S = -2.5$ V, $+V_S = 2.5$ V to 4.5 V, $+V_S = 2.5$ V, $-V_S = -2.5$ V to -4.5 V, M,D,P,L,R,F 2/	1		80		
Open loop gain	A_{VOL}	$R_L = 10$ kΩ to ground	4,5,6	01, 03	90		dB
		$R_L = 10$ kΩ to ground, M,D,P,L,R,F 2/	4				
		$R_L = 10$ kΩ to ground	4,6	02	90		
			5		80		
		$R_L = 10$ kΩ to ground, M,D,P,L,R,F 2/	4		90		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C V_S = ±2.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage high (V_{OUT} to $+V_S$)	V_{OH}	R_L = no load	1,2,3	01,02, 03		85	mV
		R_L = no load, M,D,P,L,R,F 2/	1				
		R_L = 10 kΩ	1,2,3			105	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1				
		R_L = 600 Ω	1,2,3			400	
		R_L = 600 Ω, M,D,P,L,R,F 2/	1				
Output voltage low (V_{OUT} to $-V_S$)	V_{OL}	R_L = no load	1,2,3	01,02, 03		85	mV
		R_L = no load, M,D,P,L,R,F 2/	1				
		R_L = 10 kΩ	1,2,3			105	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1				
		R_L = 600 Ω	1,2,3			400	
		R_L = 600 Ω, M,D,P,L,R,F 2/	1				
Supply current/amplifier	I_S	Unity gain	1	01, 03		1.25	mA
			2,3			1.8	
		Unity gain, M,D,P,L,R,F 2/	1			1.8	
		Unity gain	1	02		1.5	
			2,3			2	
		Unity gain, M,D,P,L,R,F 2/	1			1.8	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 1.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Offset voltage	V_{OS}	V_{CM} = 0 V	1	01,02, 03		400	μV
		V_{CM} = $+V_S$ to $-V_S$	1,2,3			500	
		V_{CM} = $+V_S$ to $-V_S$, M,D,P,L,R,F 2/	1				
Input offset channel to channel match	ΔV_{OS}	V_{CM} = $+V_S$	1,2,3	01,02, 03		800	μV
		V_{CM} = $+V_S$, M,D,P,L,R,F 2/	1				
		V_{CM} = $-V_S$	1,2,3			800	
		V_{CM} = $-V_S$, M,D,P,L,R,F 2/	1				
Input bias current	I_B	V_{CM} = 0 V	1,2,3	01, 03		330	nA
		V_{CM} = $+V_S$				330	
		V_{CM} = $+V_S$, M,D,P,L,R,F 2/	1			650	
		V_{CM} = $-V_S$	1,2,3			565	
		V_{CM} = $-V_S$, M,D,P,L,R,F 2/	1			650	
		V_{CM} = $+V_S$ – 0.5 V	1,2,3			330	
		V_{CM} = $-V_S$ + 0.5 V				565	
		V_{CM} = 0 V	1,2,3	02		375	
		V_{CM} = $+V_S$				375	
		V_{CM} = $+V_S$, M,D,P,L,R,F 2/	1			650	
		V_{CM} = $-V_S$	1,2,3			565	
		V_{CM} = $-V_S$, M,D,P,L,R,F 2/	1			650	
		V_{CM} = $+V_S$ – 0.5 V	1,2,3			375	
		V_{CM} = $-V_S$ + 0.5 V				565	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C V_S = ±1.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset current	I_{OS}	V_{CM} = $+V_S$ to $-V_S$	1	01,02, 03	-30	+30	nA
			2,3		-50	+50	
		V_{CM} = $+V_S$ to $-V_S$, M,D,P,L,R,F 2/	1		-50	+50	
Common mode input voltage range	V_{CMIR}		1,2,3	01,02, 03	$-V_S$	$+V_S$	V
		M,D,P,L,R,F 2/	1				
Output voltage high (V_{OUT} to $+V_S$)	V_{OH}	R_L = no load	1,2,3	01, 03		39	mV
		R_L = no load, M,D,P,L,R,F 2/	1			160	
		R_L = 10 kΩ	1,2,3			60	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1			175	
		R_L = no load	1,2,3	02		50	
		R_L = no load, M,D,P,L,R,F 2/	1			160	
		R_L = 10 kΩ	1,2,3			70	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1			175	
Output voltage low (V_{OUT} to $-V_S$)	V_{OL}	R_L = no load	1,2,3	01, 03		39	mV
		R_L = no load, M,D,P,L,R,F 2/	1			150	
		R_L = 10 kΩ	1,2,3			60	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1			165	
		R_L = no load	1,2,3	02		50	
		R_L = no load, M,D,P,L,R,F 2/	1			150	
		R_L = 10 kΩ	1,2,3			70	
		R_L = 10 kΩ, M,D,P,L,R,F 2/	1			165	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ $V_S = \pm 1.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current/amplifier	I_S	Unity gain	1	01, 03		1.24	mA
			2,3			1.8	
		Unity gain, M,D,P,L,R,F 2/	1			1.8	
		Unity gain	1	02		1.5	
			2,3			2.0	
		Unity gain, M,D,P,L,R,F 2/	1			1.8	

1/ Unless otherwise specified, $V_{CM} = V_O = 0$ V and R_L = open.

2/ RHA device types 01 and 02 supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation for condition A and M, D, P, and L of irradiation for condition D. However, device types 01 and 02 supplied to this drawing are only tested at the “F” level in accordance with MIL-STD-883, method 1019, condition A to TID level 300 krad(Si) and condition D to TID level 50 krad(Si) (see 1.5 herein). RHA device type 03 supplied to this drawing will meet all levels M, D, P, and L of irradiation for condition D. However, device type 03 is only tested at the “L” level in accordance with MIL-STD-883, method 1019, condition D to TID level 50 krad(Si) (see 1.5 herein).

Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device types	SEP	Temperature (T_A)	Surface Linear energy transfer (LET)
01, 02, 03	No SEL	125°C	LET ≤ 86.4 MeV/(mg/cm^2)
	No SEB	125°C	LET ≤ 86.4 MeV/(mg/cm^2)
	SET 4/	25°C	LET = 2.7 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract. See manufacturer’s SEE test report for more information.

4/ Single event transients (SET) observed at magnitude of ±10 mV with recovery time 2 μs at cross section 1.58 x 10^{-5}cm^2. and surface LET = 2.7 MeV/(mg/cm^2).

Case X

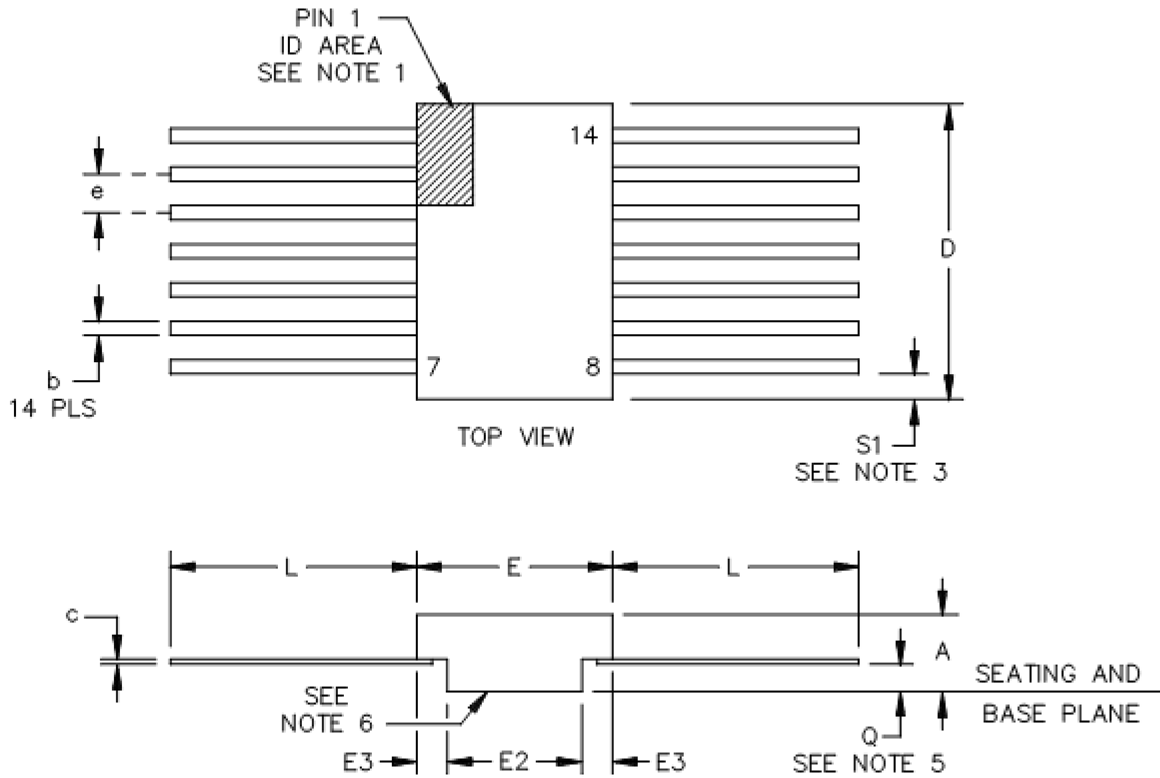


FIGURE 1. Case outline.

Case X

Symbol	Dimensions				Notes
	Inc hes		Millimeters		
	Min	Max	Min	Max	
A	0.085	0.115	2.16	2.92	
b	0.015	0.022	0.38	0.56	
c	0.004	0.009	0.10	0.23	
D	0.376	0.390	9.55	9.91	
e	0.050 BSC		1.27 BSC		
E	0.248	0.260	6.30	6.60	
E2	0.167	0.183	4.24	4.65	6
E3	0.03	---	0.76	---	
L	0.270	0.370	6.86	9.40	
Q	0.026	0.045	0.66	1.14	5
S1	0.005	---	0.13	---	3

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown.
2. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Measure dimension at all four corners.
4. For bottom brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
5. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body.
   Dimension minimum shall be reduced by 0.0015 inch (0.038 mm) maximum when solder dip lead finish is applied.
6. The bottom of the package is solderable metal surface.
7. Controlling dimensions are inch, millimeter dimensions are given for reference only.

FIGURE 1. Case outline - continued.

Device types	01, 02, 03	
Case outline	X	
Terminal number	Terminal symbol	Description
1	OUT_A	Amplifier A output
2	$-IN_A$	Amplifier A inverting input
3	$+IN_A$	Amplifier A non-inverting input
4	$+V_S$	Positive power supply
5	$+IN_B$	Amplifier B non-inverting input
6	$-IN_B$	Amplifier B inverting input
7	OUT_B	Amplifier B output
8	OUT_C	Amplifier C output
9	$-IN_C$	Amplifier C inverting input
10	$+IN_C$	Amplifier C non-inverting input
11	$-V_S$	Negative power supply
12	$+IN_D$	Amplifier D non-inverting input
13	$-IN_D$	Amplifier D inverting input
14	OUT_D	Amplifier D output
Bottom metal	NONE	Unbiased, tied to package lid. The bottom of the package is a solderable metal surface.
Metal lid	NONE	Unbiased, tied to package bottom metal.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4	1,4
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3, 1/ 2/ 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6 2/
Group D end-point electrical parameters (see 4.4)	1,4	1,4
Group E end-point electrical parameters (see 4.4)	1,4	1,4

1/ PDA applies to subgroup 1 for device class Q and subgroup 1 and Δ for device class V.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and life test delta parameters. (T_A = +25°C). 1/

Parameters	Symbol	Device types	Min	Max	Units
Offset voltage	V_{OS}	01, 02, 03	-125	125	μV
Input bias current	I_B	01, 02, 03	-75	75	nA
Supply current / amplifier	I_S	01, 02, 03	-500	500	μA

1/ Deltas are performed at room temperature.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and condition D and as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ±10% for SEB.

f. For SEB test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Number of burnouts (SEB).

c. Number of latch-up (SEL).

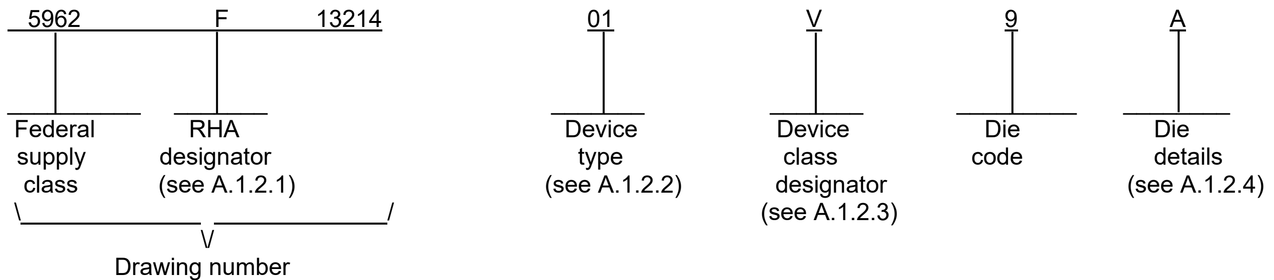
d. Number of transients (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-13214

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ISL70444SEH	Radiation hardened, 19 MHz, 40 V, low power, quad operational amplifier
02	ISL70444ASEH	Radiation hardened, 19 MHz, 40 V, low power, quad operational amplifier
03	ISL73444SEH	Radiation hardened, 19 MHz, 40 V, low power, quad operational amplifier

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-13214

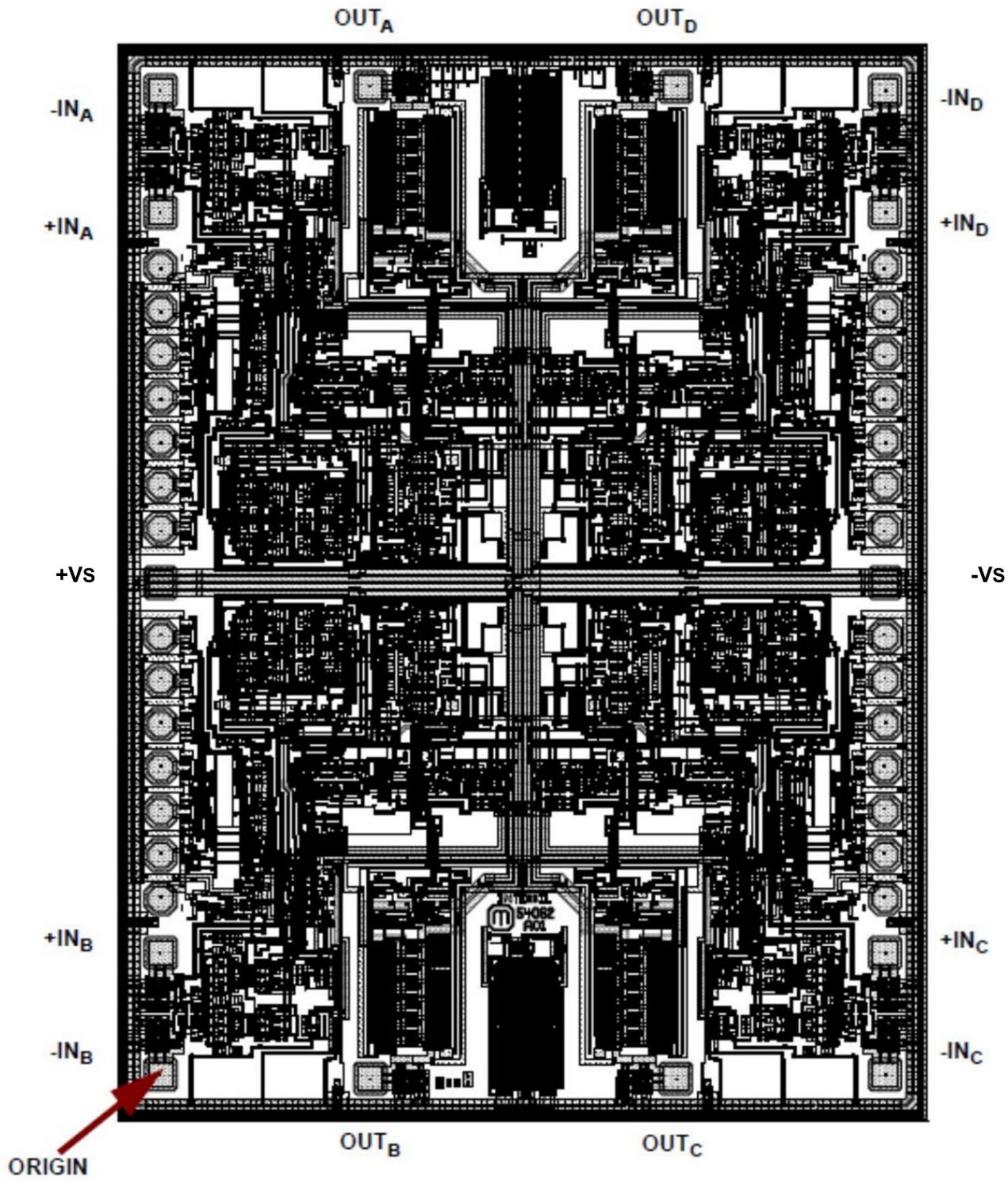


FIGURE A-1. Die bonding pad locations and electrical functions.

Pad name	Pad number	X (µm)	Y (µm)	dX (µm)	dY (µm)	Bond wires per pad
OUT_B	2	599.0	-11.5	70	70	1
OUT_C	3	1472.0	-11.5	70	70	1
$-IN_C$	4	2071.0	0.0	70	70	1
$+IN_C$	12	2071.0	347.5	70	70	1
$-V_S$	20	2071.0	1406.5	70	70	1
$+IN_D$	21	2071.0	2465.5	70	70	1
$-IN_D$	22	2071.0	2813.0	70	70	1
OUT_D	23	1472.0	2824.5	70	70	1
OUT_A	24	599.0	2824.5	70	70	1
$-IN_A$	25	0.0	2813.0	70	70	1
$+IN_A$	33	0.0	2465.5	70	70	1
$+V_S$	41	0.0	1406.5	70	70	1
$+IN_B$	42	0.0	347.5	70	70	1
$-IN_B$	1	0.0	0.0	70	70	1

Note: Origin of coordinates is the centroid of pad 1, $-IN_B$.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 2410 µm x 3175 µm (95 mils x 125 mils)
Die thickness: 483 µm ± 25 µm (19 mils ± 1 mil)

Interface materials.
Top metallization: AlCu (99.5%/0.5%)
Thickness: 15 kÅ
Backside metallization: Bare Silicon

Glassivation.
Type: Nitrox
Thickness: 15 kÅ

Substrate: PR40 process: Bonded wafer dielectrically isolated complementary bipolar.

Assembly related information.
Substrate potential: Floating
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-06-13

Approved sources of supply for SMD 5962-13214 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1321401VXC	34371	ISL70444SEHVF
5962F1321401V9A	34371	ISL70444SEHVX
5962F1321402VXC	34371	ISL70444ASEHVF
5962F1321402V9A	34371	ISL70444ASEHVX
5962L1321403VXC	34371	ISL73444SEHVF
5962L1321403V9A	34371	ISL73444SEHVX

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Renesas Electronics America 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.