REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Redrawn. Update the drawing to current MIL-PRF-38535 requirements. - drw	19-04-01	Charles F. Saffle
B	Make correction to the D2/E2 dimension limit by deleting 0.300 inch BSC and replacing with 0.500 inch BSC as specified under Figure 1. - ro	24-04-12	James R. Eschmeyer

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B							
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15							

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
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CHECKED BY
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Charles F. Saffle

DRAWING APPROVAL DATE
14-01-13

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

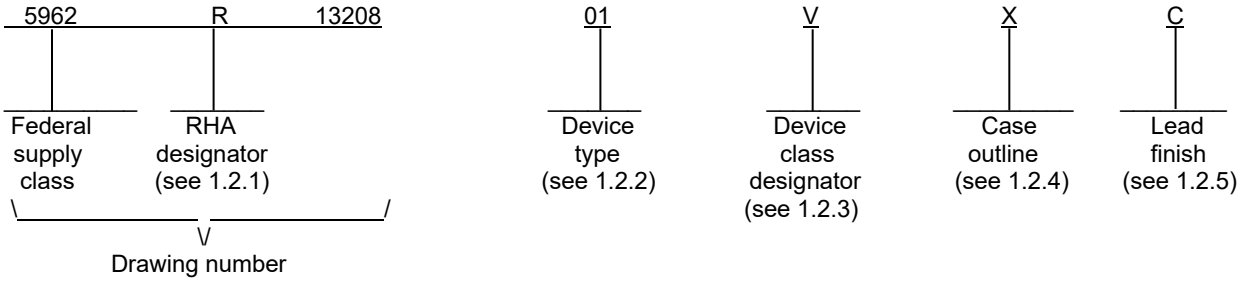
MICROCIRCUIT, DIGITAL-LINEAR, 14 BIT 400 MSPS, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL B	SIZE A	CAGE CODE **67268**	**5962-13208**
		SHEET 1 OF 15		

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADS5474-SP	A/D converter, 14-bit, 400 million samples per second (MSPS)

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	84	Quad flatpack with non-conductive tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage:
- AV_{DD5} to GND ..... 6 V
- DV_{DD3} to GND ..... 5 V
- AV_{DD3} to GND ..... 5 V

Analog input to GND ..... -0.3 V to AV_{DD5} + 0.3 V
Clock input to GND ..... -0.3 V to AV_{DD5} + 0.3 V
CLK to $\overline{CLK}$ ..... ±2.5 V
Digital data output to GND ..... -0.3 V to DV_{DD3} + 0.3 V
Maximum junction temperature (T_J) ..... +150°C
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 21.81°C/W 2/
Thermal resistance, junction-to-case (θ_{JC}) ..... 0.849°C/W 3/

1.4 Recommended operating conditions.

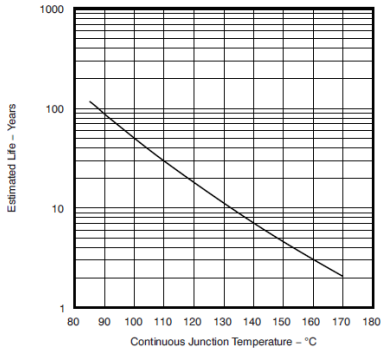
Supplies:
- Analog supply voltage (AV_{DD5}) ..... 4.75 V to 5.25 V
- Analog supply voltage (AV_{DD3}) ..... 3.1 V to 3.6 V
- Output driver supply voltage (DV_{DD3}) ..... 3 V to 3.6 V

Analog input:
- Differential input range ..... 2.2 V_{PP}
- Input common mode voltage (V_{CM}) ..... 3.1 V

Clock input:
- ADCLK input sample rate (sine wave) (1/t_C) ..... 20 to 400 MSPS 4/
- Clock amplitude, sine wave, differential ..... 0.5 V_{PP} to 5 V_{PP} 4/
- Clock duty cycle ..... 40% to 60% 4/

Digital differential output load ..... 10 pF
Operating case temperature range (T_C) ..... -55°C to +125°C

Estimated device life at elevated temperatures electromigration fail modes



1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Heat slug connected to PCB thermal plane. Airflow is at 0 LFM (no airflow).
3/ Specified with the thermal bond pad on the backside of the package soldered to a 2 ounce CU plate PCB thermal plane.
4/ Parameters are assured by characterization, but not production tested.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) ..... 100 krads(Si) 5/, 6/

The manufacturer supplying RHA device on this drawing has performed characterization test to demonstrate that the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) in accordance with MIL-STD-883, method 1019, paragraph 3.13.1.1. Therefore these parts may be considered ELDRS free at a dose level of 100 krads (Si).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

5/ The manufacturer supplying device type 01 (SiGe BiCom3x technology process) has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si).

6/ The BiCOM3X technology process uses both NPN and PNP SiGe transistors in its design. SiGe transistors do not have a base oxide layer that covers the emitter base junction like legacy HBT bipolars or even lateral bipolars. With no oxide layer there is no hole trapping or interface state generation charges. Because of this fact, SiGe transistors should be ELDRS free. However, manufacturer exposed and tested some devices at low dose rates test condition D, and observed these SiGe components do not exhibit ELDRS.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/, 2/, 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal reference voltages section							
Analog input common mode voltage reference output	V_{CM}	With internal VREF. Provided as an output via the VCM pin for dc-coupled applications	1, 2, 3	01	2.9	3.3	V
Dynamic accuracy section							
Differential linearity error	DNL	f_{IN} = 10 MHz	1, 2, 3	01	-0.99	2.5	LSB
Integral linearity error	INL	f_{IN} = 10 MHz	1, 2, 3	01	-7	7	LSB
Offset error			1, 2, 3	01	-16	16	mV
Gain error			1, 2, 3	01	-5	5	%FS
Power supply section							
Analog supply current	I_{AVDD5}	F_S = 400 MSPS, V_{IN} = full scale, f_{IN} = 70 MHz	1, 2, 3	01		380	mA
	I_{AVDD3}			01		210	
Digital supply current	I_{DVDD3}	F_S = 400 MSPS, V_{IN} = full scale, f_{IN} = 70 MHz	1, 2, 3	01		85	mA
Total power dissipation	P_D			01		2.835	W
Power-down power dissipation	P_{DWN}	PDWN pin = logic HIGH	1, 2, 3	01		350	mW
Dynamic AC characteristics section							
Signal-to-noise ratio	SNR	f_{IN} = 70 MHz	4, 5, 6	01	65		dBFS
		f_{IN} = 230 MHz			65		
Spurious free dynamic range	SFDR	f_{IN} = 70 MHz	4, 5, 6	01	69		dBc
		f_{IN} = 230 MHz			64.5		
Signal-to-noise and distortion	SINAD	f_{IN} = 70 MHz	4, 5, 6	01	62.5		dBc
		f_{IN} = 230 MHz			60.5		
Effective number of bits	ENOB	f_{IN} = 70 MHz	4, 5, 6	01	10.1		Bits
		f_{IN} = 230 MHz			9.77		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/, 2/, 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital characteristics – LVDS digital outputs							
Differential output voltage (±)	V_{OD}		1, 2, 3	01	247	454	mV
Common mode output voltage	V_{OC}		1, 2, 3	01	1.115	1.375	V
Digital characteristics – Digital inputs							
High level input voltage	V_{IH}	PWD (pin33)	1, 2, 3	01	2.0		V
Low level input voltage	V_{IL}		1, 2, 3	01		0.8	V
High level input current	I_{IH}		1, 2, 3	01		1	µA
Low level input current	I_{IL}		1, 2, 3	01	-1		µA
Timing characteristics 4/							
Clock period	t_{CLK}		9, 10, 11	01	2.5	50	ns
Clock pulse duration, high	t_{CLKH}		9, 10, 11	01	1		ns
Clock pulse duration, low	t_{CLKL}		9, 10, 11	01	1		ns
CLK to DRY delay 5/	t_{DRY}	Zero crossing, 10 pF to GND on each output pin	9, 10, 11	01	700	2500	ps
CLK to DATA/OVR delay 5/	t_{DATA}	Zero crossing, 10 pF to GND on each output pin	9, 10, 11	01	650	2600	ps
DATA to DRY skew	t_{SKEW}	t_{DATA} - t_{DRY}, 10 pF to GND on each output pin	9, 10, 11	01	-700	700	ps

1/ Unless otherwise specified, sampling rate = 400 MSPS, 50 % clock duty cycle, AV_{DD5} = 5 V, AV_{DD3} = 3.3 V, DV_{DD3} = 3.3 V, 3 V_{PP} differential clock.

2/ Devices supplied to this drawing have been characterized through all levels M, D, L, and R of irradiation. However, this device is only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein).

3/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krads (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si).

4/ Timing parameters are assured by characterization, but not production tested. See figure 4.

5/ DRY, DATA, and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the overall propagation delay.

Case X

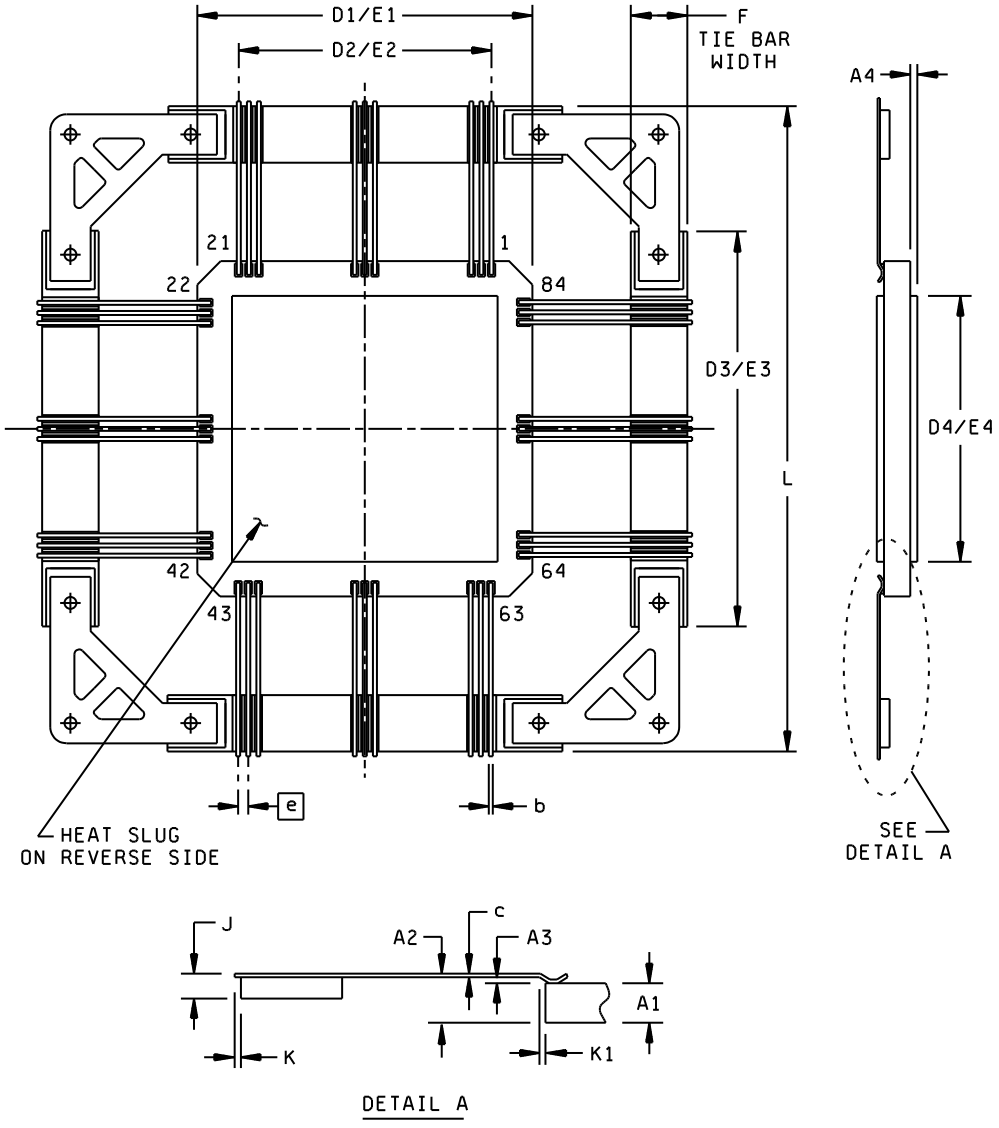


FIGURE 1. Case outline X.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-13208**
		REVISION LEVEL B	SHEET **8**

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	---	0.090	---	2.29
A2	---	0.115	---	2.92
A3	0.002	0.014	0.05	0.36
A4	0.03 BSC		0.762 BSC	
b	0.005	0.011	0.127	0.28
c	0.004	0.008	0.10	0.20
D1/E1	0.740	0.760	18.8	19.30
D2/E2	0.500 BSC		12.7 BSC	
D3/E3	1.198	1.222	30.43	31.04
D4/E4	0.630 BSC		16.0 BSC	
e	0.025 BSC		0.64 BSC	
F	0.175	0.225	4.44	5.72
J	0.029	0.042	0.75	1.05
K	---	0.020	---	0.51
K1	---	0.018	---	0.46
L	1.98	2.024	50.29	51.4
N	84			

NOTES:
1. Controlling dimensions are inches, millimeter dimensions are given for reference only.
2. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated and can be solder dipped.
5. All leads are not shown for clarity purposes.
6. Lid and heat sink are connected to GND leads.

FIGURE 1. Case outline X – continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AGND	22	AGND	43	AGND	64	AGND
2	DV_{DD3}	23	AV_{DD5}	44	$\overline{OVR}$	65	$\overline{D6}$
3	GND	24	GND	45	OVR	66	D6
4	AV_{DD5}	25	AV_{DD5}	46	NC	67	$\overline{D7}$
5	NC	26	GND	47	NC	68	D7
6	NC	27	AV_{DD5}	48	NC	69	GND
7	V_{REF}	28	GND	49	NC	70	DV_{DD3}
8	GND	29	AV_{DD5}	50	$\overline{D0}$	71	$\overline{D8}$
9	AV_{DD5}	30	GND	51	D0	72	D8
10	GND	31	VCM	52	$\overline{D1}$	73	$\overline{D9}$
11	CLK	32	GND	53	D1	74	D9
12	$\overline{CLK}$	33	AV_{DD5}	54	DV_{DD3}	75	$\overline{D10}$
13	GND	34	GND	55	GND	76	D10
14	AV_{DD5}	35	PWDN	56	$\overline{D2}$	77	$\overline{D11}$
15	AV_{DD5}	36	GND	57	D2	78	D11
16	GND	37	AV_{DD3}	58	$\overline{D3}$	79	$\overline{D12}$
17	AIN+	38	GND	59	D3	80	D12
18	AIN-	39	AV_{DD3}	60	$\overline{D4}$	81	$\overline{D13}$
19	GND	40	GND	61	D4	82	D13
20	AV_{DD5}	41	AV_{DD3}	62	$\overline{D5}$	83	$\overline{DRY}$
21	GND	42	GND	63	D5	84	DRY

FIGURE 2. Terminal connections.

Terminal symbol	Description
AIN	Differential input signal (positive)
$\overline{\text{AIN}}$	Differential input signal (negative)
AV_{DD5}	Analog power supply (5 V)
AV_{DD3}	Analog power supply (3.3 V)
DV_{DD3}	Digital and output driver power supply (3.3 V)
CLK	Differential input clock (positive). Conversion initiated on rising edge.
GND	Ground
$\overline{\text{CLK}}$	Differential input clock (negative)
D0, $\overline{\text{D0}}$	LVDS digital output pair, least significant bit (LSB)
D1-D12, $\overline{\text{D1}}$ - $\overline{\text{D12}}$	LVDS digital output pairs
D13, $\overline{\text{D13}}$	LVDS digital output pair, most significant bit (MSB)
DRY, $\overline{\text{DRY}}$	Data ready LVDS output pair
NC	No connect
OVR, $\overline{\text{OVR}}$	Over range indicator LVDS output. A logic high signals an analog input excess of full scale range.
VCM	Common-mode voltage output (3.1 V nominal). Commonly used in DC-coupled applications to set the correct common-mode voltage.
PDWN	Power-down (active high). Device is in sleep mode PDWN pin is logic HIGH. ADC converter is awake when PDWN is logic LOW (grounded)
V_{REF}	Reference voltage input/output

FIGURE 2. Terminal connections – continued.

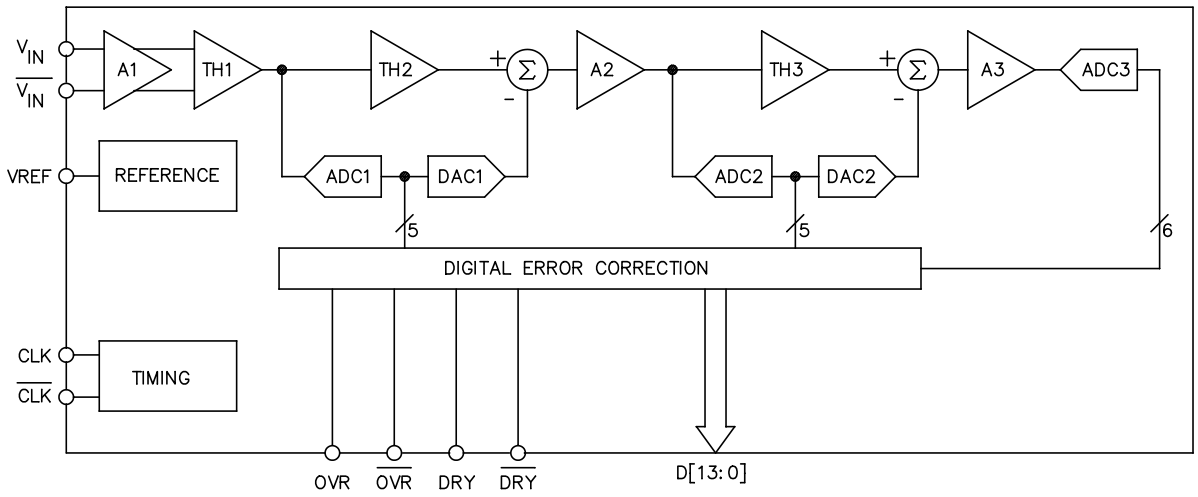


FIGURE 3. Block diagram.

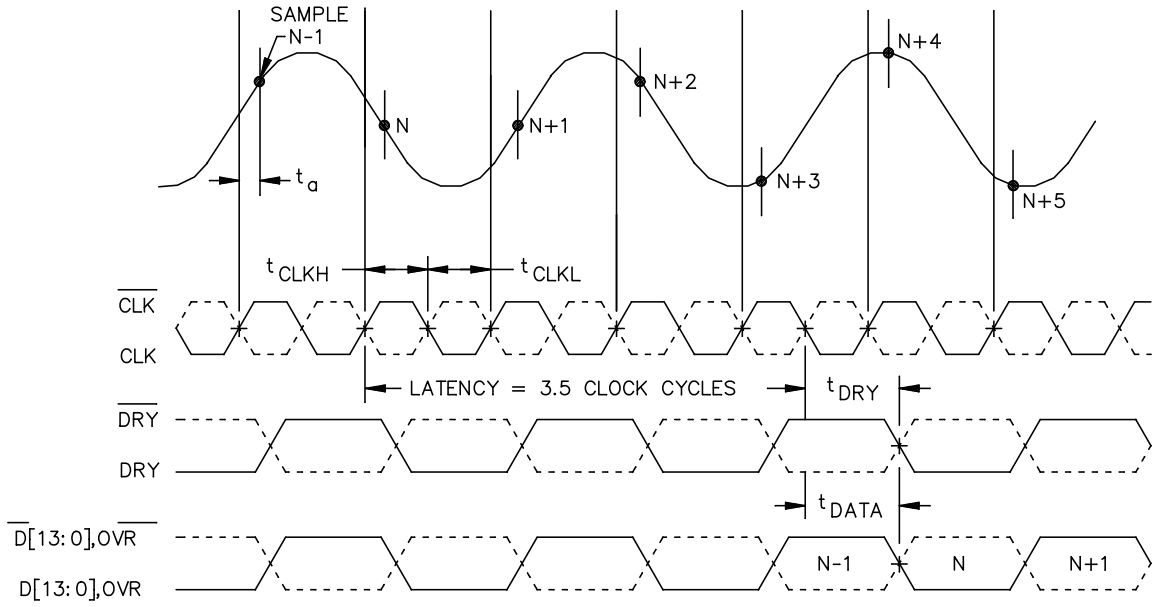


FIGURE 4. Timing waveforms.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-13208
		REVISION LEVEL B	SHEET 12

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 1/, 2/ 4, 5, 6, 9, 10, 11	1, 2, 3, 1/, 2/, 3/ 4, 5, 6, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 2/ 6, 9, 10, 11	1, 2, 3, 4 ,5, 2/ 6, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 2/ 6, 9, 10, 11	1, 2, 3, 2/, 3/ 4, 5, 6, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9
Group E end-point electrical parameters (see 4.4)	1, 4, 9	1, 4, 9

1/ PDA applies to subgroup 1.
2/ Subgroups 9, 10, 11, if not tested, are guaranteed to the limits in table I.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test. Delta parameters (+25°C).

Parameters 1/	Delta limits
Analog input common-mode voltage reference output (V_{CM})	+/-50 mV
3.3 V digital supply (I_{DVDD3})	+/-5 mA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A and condition D as specified herein for device type 01.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 24-04-12

Approved sources of supply for SMD 5962-13208 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1320801VXC	01295	ADS5474-RHA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243