

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add radiation hardness requirements to device type 01. -rrp	13-12-16	C. SAFFLE
B	Table IIB. Change feedback pin voltage (VFB) from -18 mV min and 18 mV max to read -9 mV min and 9 mV max. Update drawing to current MIL-PRF-38535 requirement. - jt	16-12-01	C. SAFFLE
C	Paragraph 1.3 absolute maximum ratings: change output voltage range from "-0.3 V to V _{IN} " to "-0.3V to 7.5 V". Paragraph 1.4 Recommended operating conditions. Add t _R EN Rise time (10% to 90%) for EN signal at 100 μs and add t _R V _{IN} Rise time (10% to 90%) for V _{IN} = EN at 1 ms. Table I. change max limit for output voltage range from "V _{IN} - 0.35" to read "V _{IN} ". - jt	17-03-24	C. SAFFLE
D	Add device type 02. - ro	17-06-22	C. SAFFLE
E	Add paragraph 3.1.1 and Appendix A for microcircuit die. - ro	18-01-23	C. SAFFLE
F	Make change to thermal resistance, junction-to-case and junction-to-ambient limits in section 1.3. In Table I, make change to the operating voltage range at CS, V _{CS} , minimum limit from 0.3 V to 0 V. In Table I, add footnote to the operating voltage range at CS test. -rrp	20-09-01	J. ESCHMEYER



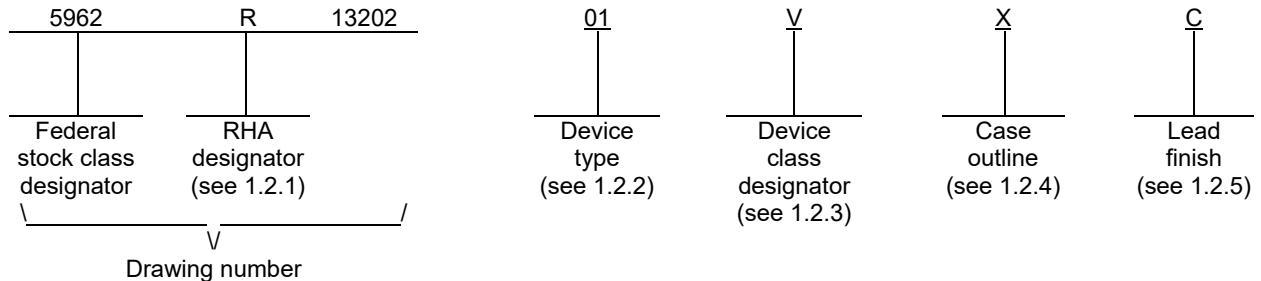
REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F											
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS OF SHEETS	REV			F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY RAJESH PITHADIA	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime																	
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY RAJESH PITHADIA																		
	APPROVED BY CHARLES F. SAFFLE	MICROCIRCUIT, LINEAR, VOLTAGE REGULATOR, MONOLITHIC SILICON																	
	DRAWING APPROVAL DATE 13-10-09																		
	REVISION LEVEL F	SIZE A	CAGE CODE 67268	5962-13202															
		SHEET 1 OF 23																	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	TPS7H1101	Low dropout, adjustable, voltage regulator
02	TPS7H1101A	Low dropout, adjustable, voltage regulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. ^{1/}

Input voltage range:

V _{IN} , PG pins	-0.3 V to +7.5 V
FB, COMP, PCL, CS, EN pins	-0.3 V to V _{IN} + 0.3 V
Output voltage range (V _{OUT} , SS)	-0.3 V to 7.5 V
Peak output current	Internally limited
Pin PG sink current	5 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T _J)	+150°C
Thermal resistance, junction-to-case (bottom) (θ _{JCbot})	0.4°C/W
Thermal resistance, junction-to-ambient (θ _{JA})	24.3°C/W

1.4 Recommended operating conditions.

Input voltage (V _{IN})	1.5 V to 7 V
Junction temperature range (T _J)	-55°C to +125°C
Ambient operating temperature range (T _A)	-55°C to +125°C
t _R EN Rise time (10% to 90%) for EN signal :	
Device type 01 only	100 μs
t _R V _{IN} Rise time (10% to 90%) for V _{IN} = EN :	
Device type 01 only	1 ms

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rads(Si)/s)	100 krad(Si) ^{2/}
Maximum total dose available (low dose rate ≤ 10m rad(Si)/s)	100 krad(Si) ^{2/}

The manufacturer supplying RHA device types 01 and 02 on this drawing has performed characterization test to demonstrate that the parts do not exhibit enhanced low dose rate sensitivity (ELDRS) in accordance with MIL-STD-883, method 1019, paragraph 3.13.1.1 to a TID level 100 krad (Si).

^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

^{2/} The manufacturer supplying device types 01 and 02 have performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krad (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krad(Si).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input voltage range	V _{IN}		1, 2, 3	01, 02	1.5	7	V
Feedback pin voltage	V _{FB}	1.5 V ≤ V _{IN} ≤ 7 V	1, 2, 3	01, 02	0.594	0.616	V
Output voltage range	V _{OUT}		1, 2, 3	01, 02	0.8	V _{IN}	V
Output voltage accuracy		0 A ≤ I _{OUT} ≤ 3 A, <u>3/ 4/</u> 1.5 V ≤ V _{IN} ≤ 7 V, 0.8 < V _{OUT} < 6.65 V	1, 2, 3	01, 02	-2	2	%
Line regulation	ΔV _{OUT} % / ΔV _{IN}	1.5 V ≤ V _{IN} ≤ 7 V	1,2,3	01, 02	-0.07	0.07	%/V
DC input line regulation	ΔV _{OUT}	1.5 V ≤ V _{IN} ≤ 7 V, <u>5/</u> V _{OUT} = 0.8 V, I _{OUT} = 10 mA	1	01, 02		3.0	mV
			2			0.6	
			3			1.0	
		1.5 V ≤ V _{IN} ≤ 7 V, <u>5/</u> V _{OUT} = 1.2 V, I _{OUT} = 10 mA	1			3.0	
			2			0.6	
			3			1.0	
		1.5 V ≤ V _{IN} ≤ 7 V, <u>5/</u> V _{OUT} = 1.8 V, I _{OUT} = 10 mA	1			3.0	
			2			0.6	
			3			1.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> <u>2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC output load regulation <u>6/</u>	ΔV _{OUT}	V _{OUT} = 0.8 V, 0 ≤ I _{LOAD} ≤ 1 A <u>5/</u>	1	01, 02		1.0	mV
			2			1.1	
			3			1.3	
		V _{OUT} = 0.8 V, 0 ≤ I _{LOAD} ≤ 2 A <u>5/</u>	1, 2			1.8	
			3			2.4	
		V _{OUT} = 0.8 V, 0 ≤ I _{LOAD} ≤ 3 A <u>5/</u>	1			1.9	
			2			2.6	
			3			3.4	
		V _{OUT} = 1.2 V, 0 ≤ I _{LOAD} ≤ 1 A <u>5/</u>	1			1.2	
			2, 3			1.3	
		V _{OUT} = 1.2 V, 0 ≤ I _{LOAD} ≤ 2 A <u>5/</u>	1			1.6	
			2, 3			2.1	
		V _{OUT} = 1.2 V, 0 ≤ I _{LOAD} ≤ 3 A <u>5/</u>	1			1.7	
2			2.4				
3			3.5				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC output load regulation <u>6/</u>	ΔV _{OUT}	V _{OUT} = 1.8 V, 0 ≤ I _{LOAD} ≤ 1 A <u>5/</u>	1, 2	01, 02		0.9	mV
			3			1.2	
			1			2.4	
		V _{OUT} = 1.8 V, 0 ≤ I _{LOAD} ≤ 2 A <u>5/</u>	2			1.4	
			3			1.9	
			1			3.9	
		V _{OUT} = 1.8 V, 0 ≤ I _{LOAD} ≤ 3 A <u>5/</u>	2			2.1	
			3			2.5	
			1			2.9	
		V _{OUT} = 6.65 V, 0 ≤ I _{LOAD} ≤ 1 A <u>5/</u>	2			2.6	
			3			3.5	
			1			5.9	
		V _{OUT} = 6.65 V, 0 ≤ I _{LOAD} ≤ 2 A <u>5/</u>	2			4.7	
			3			8.0	
			1			9.3	
V _{OUT} = 6.65 V, 0 ≤ I _{LOAD} ≤ 3 A <u>5/</u>	2		8.0				
	3		25.0				
Dropout voltage <u>6/</u>	V _{DO}	I _{OUT} = 3 A, V _{OUT} = 1.3 V	1, 2, 3	01, 02		335	mV
Programmable output current limit range	I _{CL}	V _{IN} = 1.5 V, V _{OUT} = 1.2 V, PCL resistance = 47 kΩ	1, 2, 3	01, 02	500	750	mA
		V _{IN} = 1.5 V, V _{OUT} = 1.2 V, PCL resistance varies			200	3500 <u>7/</u>	
Operating voltage range at CS <u>8/</u>	V _{CS}		1, 2, 3	01, 02	0	V _{IN}	V
Ground pin current	I _{GN}	V _{IN} = 1.5 V, V _{OUT} = 1.2 V, I _{OUT} = 2 A	1, 2, 3	01, 02		16	mA
Quiescent current (no load)	I _Q	V _{IN} = V _{OUT} + 0.5 V, I _{OUT} = 0 A	1, 2, 3	01, 02		10	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Shutdown current	I _{SHDN}	1.5 V ≤ V _{IN} ≤ 7 V	1, 2, 3	01, 02		230	μA
			M, D, P, L, R	1	01, 02		
FB/SNS pin current	I _{SNS} , I _{FB}	V _{IN} = 7 V, V _{OUT} = 6.65 V	1, 2, 3	01, 02		5	nA
EN pin input current	I _{EN}	V _{IN} = 7 V, V _{EN} = 7 V, V _{OUT} = 6.65 V	1, 2, 3	01, 02		150	nA
EN pin propagation delay	E _{prop Dly}	V _{IN} = 2.2 V, EN rise to I _{OUT} rise	9, 10, 11	01, 02		1000	μs
EN pin turn-on delay (delay to PG assertion)	t _{EN}	V _{IN} = 2.2 V, V _{OUT} = 1.8 V, I _{LOAD} = 1 A, C _{OUT} = 220 μF, C _{SS} = 2 nF	9, 10, 11	01, 02		1.6	ms
PG pin threshold	V _{THPG}	No load, 0.8 V ≤ V _{OUT} ≤ 6.65 V	1, 2, 3	01, 02	86		%
PG pin output low	V _{OLPG}	I _{PG} = -1 mA	1, 2, 3	01, 02		400	mV
PG pin leakage current	I _{LKPG}	V _{OUT} > V _{THPG} , V _{PG} = 7 V	1, 2, 3	01, 02		2.5	μA
SS pin current	I _{SS}	V _{SS} = 1.5 V to 7 V	1, 2, 3	01, 02		3.5	μA
V _{ILEN} EN terminal input low (disable)	V _{ILEN}	1.5 V < V _{IN} < 7 V	1,2,3	02		0.55	V
V _{IHEN} EN terminal input high (enable)	V _{IHEN}	1.5 V < V _{IN} < 7 V	1,2,3	02	V _{IN} - 0.7		V

- 1/ 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT(target)} = V_{IN} - 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 μF, PG pin pulled up to V_{IN} with 50 kΩ.
- 2/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see 1.5 herein). The manufacturer supplying device types 01 and 02 have performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krad (Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100 krad(Si).
- 3/ Based on using 0.1% resistors.
- 4/ The output voltage accuracy of condition at I_{OUT} = 2 A and I_{OUT} = 3 A is specified by characterization, but not production tested.
- 5/ Line and load regulations done under pulse condition for T < 10 ms.
- 6/ The parameter is guaranteed to the limit specified by characterization, but not production tested.
- 7/ The maximum limit of the I_{CL} parameter is guaranteed to the limit specified by characterization, but not production tested.
- 8/ To insure foldback is enabled, V_{CS} must be > 0.9 x V_{FB}.

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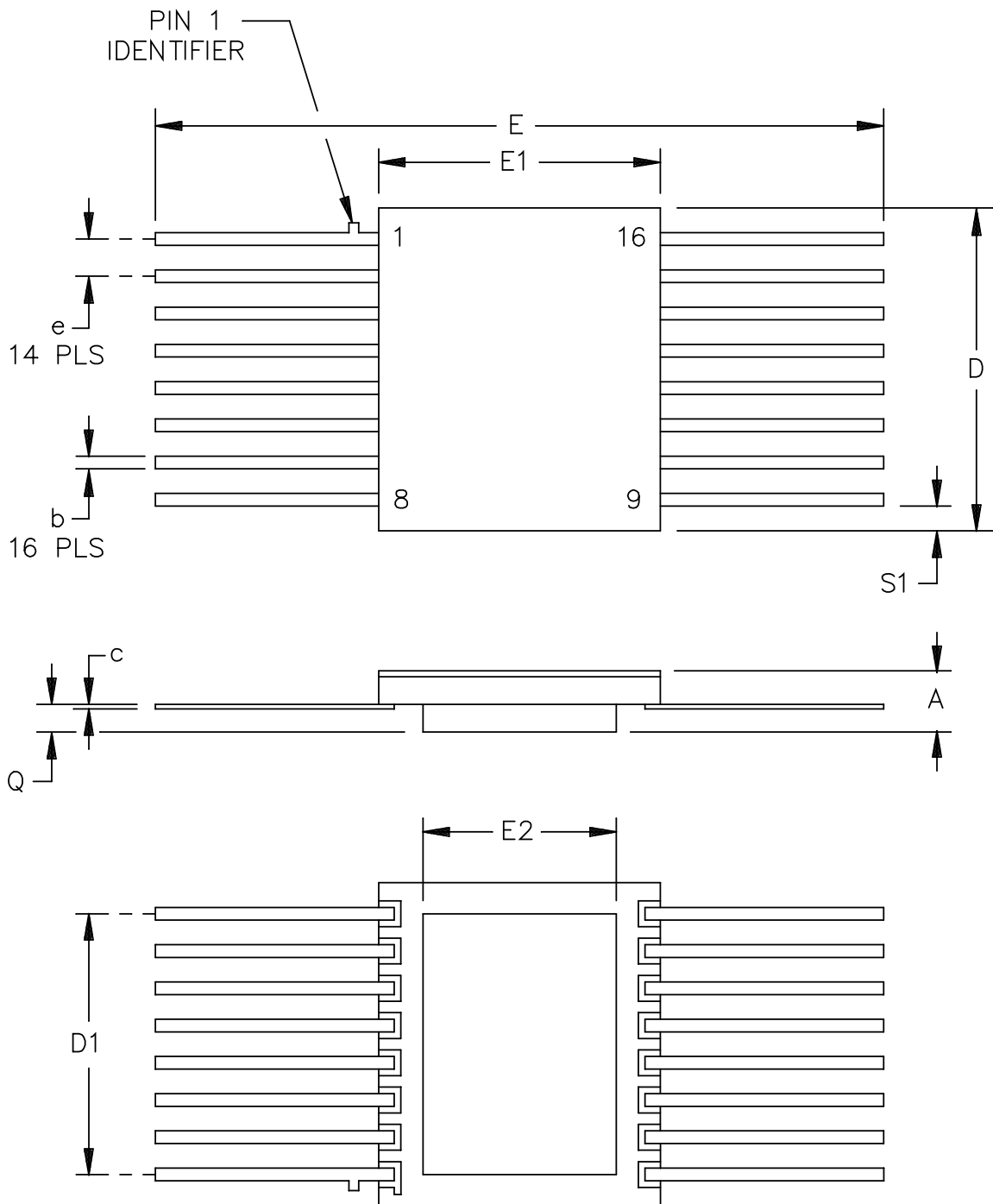


FIGURE 1. Case outline.

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Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.833	2.333	0.072	0.092
B	0.382	0.482	0.015	0.019
c	0.097	0.177	0.004	0.007
D	10.760	11.260	0.424	0.443
D1	8.550	9.050	0.337	0.356
E	24.642	25.142	0.970	0.990
E1	9.380	9.880	0.369	0.389
E2	6.340	6.840	0.250	0.269
e	1.190	1.350	0.047	0.053
Q	0.690	1.190	0.027	0.047
S1	0.844 REF		0.033 REF	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This package is hermetically sealed with a metal lid. Lid and heat sink are connected to pin 8 (GND).
3. The leads are gold plated.

FIGURE 1. Case outline – continued.

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Device types	01 and 02
Case outline	X
Terminal number	Terminal symbol
1	SS
2	EN
3	V _{IN}
4	V _{IN}
5	V _{IN}
6	V _{IN}
7	PCL
8	GND
9	PG/OC
10	CS
11	V _{OUT}
12	V _{OUT}
13	V _{OUT}
14	V _{OUT}
15	COMP
16	FB

FIGURE 2. Terminal connections.

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Terminal symbol	Description
VIN	Unregulated supply voltage. It is recommended to connect an input capacitor as a good analog circuit practice.
VOUT	Regulated output.
FB	The output voltage feedback input through voltage dividers.
GND	Ground/Thermal pad. Thermal pad must be connected to GND.
EN	Enable pin. Driving this pin to logic high enables the device. Driving the pin to logic low disables the device.
CS	Current sense pin. Resistor connected from CS to VIN. CS pin indicates voltage proportional to output current. CS pin low: Foldback current limit disabled. CS pin high: Foldback current limit enabled.
SS	SoftStart pin. Connecting an external capacitor slows down the output voltage ramp rate after enable event.
PG/OC	PowerGood pin. PG is open drain output to indicate the output voltage reaches to 90% of target. PG pin is also used as indicator when over current condition is activated.
PCL	Programmable current limit. A resistor to GND sets the current limit activation point. The range of resistor that can be used on the PCL pin to GND is 8.2 kΩ to 160 kΩ.
COMP	Output of error amplifier.

FIGURE 2. Terminal connections – continued.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 9	1, 9
Final electrical parameters (see 4.2)	1, 2, 3, 9, 10, 11 <u>1/</u>	1,2, 3, 9, 10, 11 <u>1/</u> <u>2/</u>
Group A test requirements (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11 <u>2/</u>
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	1, 9	1, 9

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters.

TABLE IIB. 240 burn-in and and group C life test delta parameters. (TA = +25°C). 1/

Parameters	Symbol	Min	Max	Units
Quiescent current (no load)	IQ	-0.8	+0.8	mA
Feedback pin voltage	VFB	-9	+9	mV
Shutdown current	ISHDN	-16	+16	μA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at TA = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and condition D as specified herein for device types 01 and 02.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

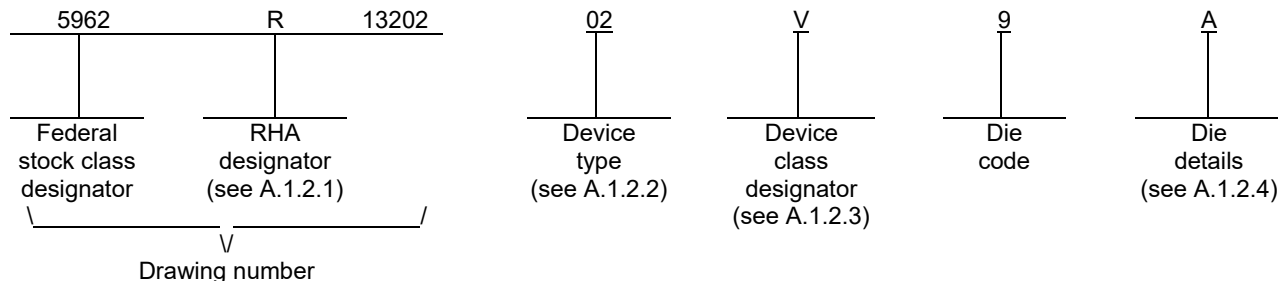
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A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
02	TPS7H1101A	Low dropout, adjustable, voltage regulator

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

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A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
02	A-1

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
02	A-1

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

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A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.3 herein.

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A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

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A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

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Bond pad coordinates in microns					
Description	Pad number	X min	Y min	X max	Y max
SS	1	109.89	4046.805	287.19	4224.105
EN	2	109.89	3493.35	287.19	3670.65
VIN	3	1359.99	3021.345	1537.29	3198.645
VIN	4	1359.99	2749.005	1537.29	2926.305
VIN	5	1359.99	2553.705	1537.29	2731.005
VIN	6	1359.99	2281.365	1537.29	2458.665
VIN	7	1359.99	2086.065	1537.29	2263.365
VIN	8	1359.99	1813.725	1537.29	1991.025
VIN	9	1359.99	1618.425	1537.29	1795.725
PCL	10	109.89	660.285	287.19	837.585
GND	11	109.89	319.455	287.19	496.755
GND	12	392.58	109.935	569.88	287.235
VIN	13	1359.00	1346.085	1537.29	1523.385
PG/OC	14	2898.945	379.62	3076.245	556.92
CS	15	2898.945	724.32	3076.245	901.62
VOUT	16	2829.105	1384.6095	3006.405	1561.995
VOUT	17	2829.105	1579.815	3006.405	1757.115
VOUT	18	2829.105	1852.335	3006.405	2029.63
VOUT	19	2829.105	2047.455	3006.405	2224.755
VOUT	20	2829.105	2319.975	3006.405	2497.275
VOUT	21	2829.105	2515.095	3006.405	2692.395
VOUT	22	2829.105	2787.615	3006.405	2964.915
VOUT	23	2829.105	2982.735	3006.405	3160.035
COMP	24	2898.945	3519.72	3076.245	3697.02
FB	25	2898.945	3956.535	3076.245	4133.835

FIGURE A-1. Die bonding pad locations and electrical functions.

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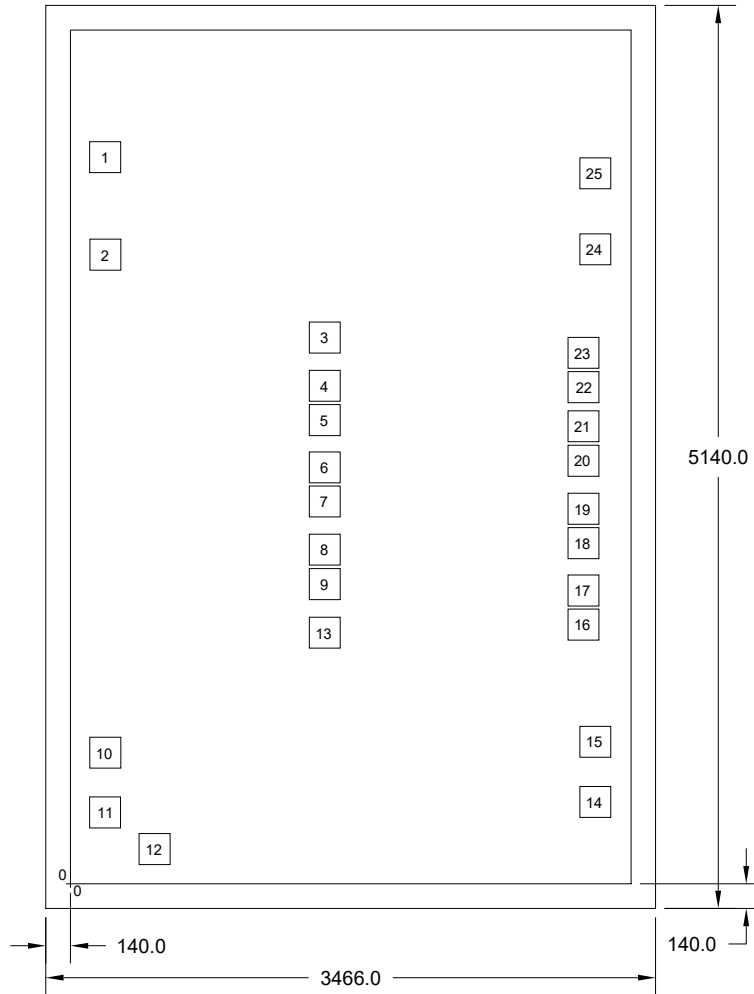


FIGURE A-1. Die bonding pad locations and electrical functions - continued.

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Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size: 3466.0 microns x 5140.0 microns

Die thickness: 15 mils

Backside finish: Silicon with backgrind

Backside potential: Ground

Bond pad metallization composition: AlCu

Bond pad thickness: 30 kÅ

Assembly related information.

Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-09-01

Approved sources of supply for SMD 5962-13202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-1320201VXC	01295	TPS7H1101-SP
5962R1320201VXC	01295	TPS7H1101-RHA
5962R1320202VXC	01295	TPS7H1101A-RHA
5962R1320202V9A	01295	TPS7H1101A-RHA

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments Incorporated
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.